NB7L111M

2.5V/3.3V, 6.125Gb/s 2:1:10 Differential Clock/Data Driver with CML Output

Description

The NB7L111M is a low skew 2:1:10 differential clock/data driver, designed with clock/data distribution in mind. It accepts two clock/data sources into multiplexer input and reproduces ten identical CML differential outputs. This device is ideal for clock/data distribution across the backplane or a board, and redundant clock switchover applications.

The input signals can be either differential or single–ended (if the external reference voltage is provided). Differential inputs incorporate internal 50 Ω termination resistors and accept Negative ECL (NECL), Positive ECL (PECL), LVCMOS, LVTTL, CML, or LVDS (using appropriate power supplies). The differential 16 mA CML output provides matching internal 50 Ω termination, and 400 mV output swing when externally terminated 50 Ω to V_{CC}.

The NB7L111M operates from a 2.5 V ±5% supply or a 3.3 V ±5% supply and is guaranteed over the full industrial temperature range of −40°C to +85°C. This device is packaged in a low profile 8x8 mm, QFN−52 package with 0.5 mm pitch (see package dimension on the back of the datasheet).

Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency > 5.5 GHz Typical
- Maximum Input Data Rate > 6.125 Gb/s Typical
- < 0.5 ps Maximum Clock RMS Jitter
- < 15 ps Maximum Data Dependent Jitter at 3.125 Gb/s
- 50 ps Typical Rise and Fall Times
- 240 ps Typical Propagation Delay
- 2 ps Typical Duty Cycle Skew
- 10 ps Typical Within Device Skew
- 15 ps Typical Device–to–Device Skew
- Operating Range: V_{CC} = 2.5 V ±5 and 3.3 V ±5
- 400 mV Differential CML Output Swing
- 50 Ω Internal Input and Output Termination Resistors
- These Devices are Pb−Free and are RoHS Compliant*

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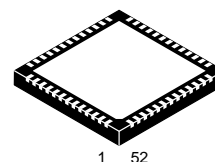
QFN−52
MN SUFFIX
CASE 485M

MARKING DIAGRAM*

```
        52
  1
         NB7L
         111M
         AWLYYWWG
```

A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
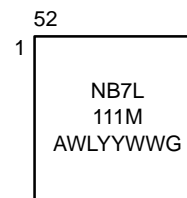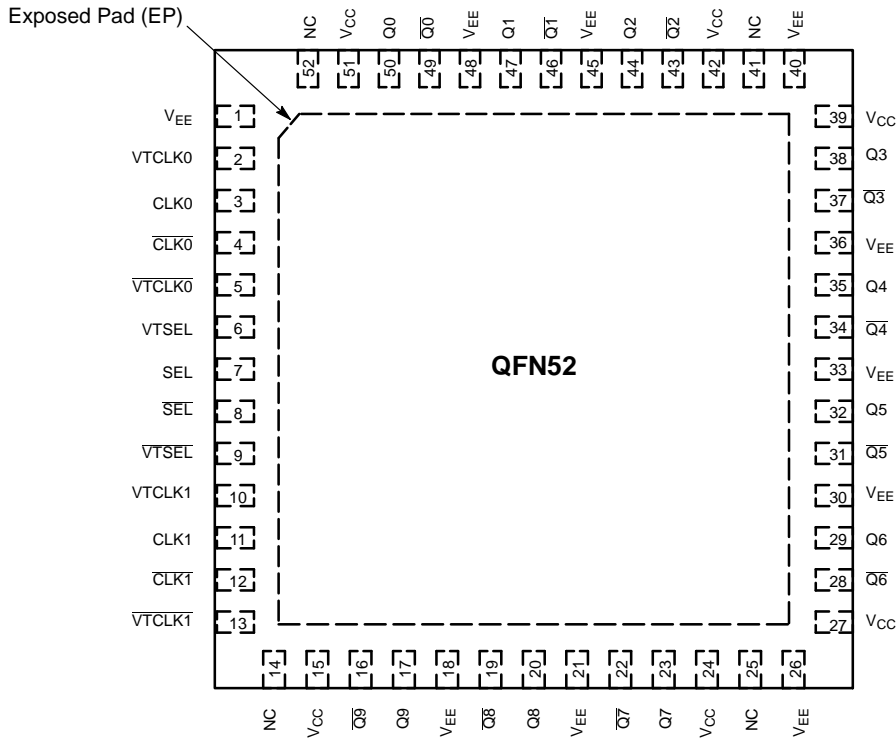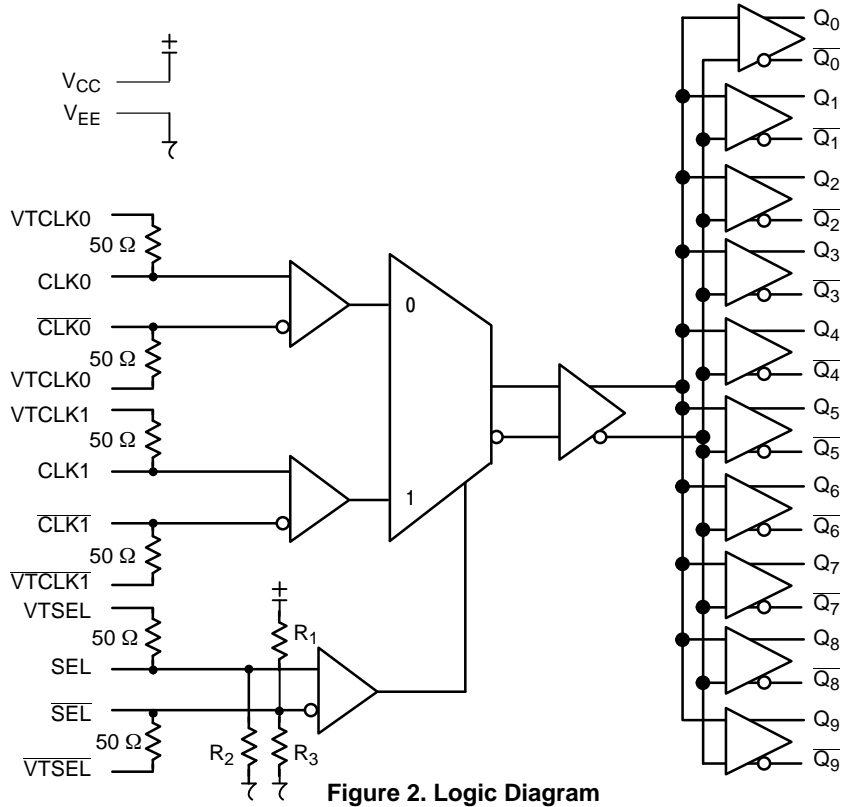
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Figure 1. Pinout (Top View)

Figure 2. Logic Diagram

Table 1. FUNCTION TABLE

SEL	$\overline{SEL}$	CLK0/$\overline{CLK0}$	CLK1/$\overline{CLK1}$
LOW	HIGH	ON	OFF
HIGH	LOW	OFF	ON

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
15, 24, 27, 39, 42, 51	V_{CC}	–	Positive supply voltage. All V_{CC} pins must be externally connected to power supply to guarantee proper operation.
1, 18, 21, 26, 30, 33, 36, 40, 45, 48	V_{EE}	–	Negative supply voltage. All V_{EE} pins must be externally connected to power supply to guarantee proper operation.
2	VTCLK0	–	Internal 50 Ω termination pin for CLK0. (Note 2)
3	CLK0	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Non−inverted differential clock/data input 0 (Note 2).
4	$\overline{\text{CLK0}}$	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Inverted differential clock/data input 0 (Note 2).
5	$\overline{\text{VTCLK0}}$	–	Internal 50 Ω termination pin for $\overline{\text{CLK0}}$. (Note 2)
6	VTSEL		Internal 50 Ω termination pin for SEL. (Note 2)
7	SEL	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Non−inverted differential clock/data select input. Internal 75 kΩ to V_{EE}.
8	$\overline{\text{SEL}}$	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Inverted differential clock/data select input. Internal 56 KΩ to V_{CC} and 56 kΩ to V_{EE} bias this pin to $(V_{CC}-V_{EE})/2$.
9	$\overline{\text{VTSEL}}$	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Internal 50 Ω termination pin for $\overline{\text{SEL}}$. (Note 2)
10	VTCLK1	–	Internal 50 Ω termination pin for CLK1. (Note 2)
11	CLK1	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Non−inverted differential clock/data input 1 (Note 2).
12	$\overline{\text{CLK1}}$	LVPECL, CML, LVCMOS, LVTTL, LVDS Input	Inverted differential clock/data input 1 (Note 2).
13	$\overline{\text{VTCLK1}}$	–	Internal 50 Ω termination pin for $\overline{\text{CLK1}}$. (Note 2)
14, 25, 41, 52	NC	–	
17, 20, 23, 29, 32, 35, 38, 44, 47, 50	Q[0−9]	CML Outputs	Non−inverted CML outputs [0−9] with internal 50 Ω source termination resistor (Note 1).
16, 19, 22, 28, 31, 34, 37, 43, 46, 49	$\overline{\text{Q[0−9]}}$	CML Outputs	Inverted CML outputs [0−9] with internal 50 Ω source termination resistor (Note 1).
EP	–	–	Exposed Pad (EP). The thermally exposed pad on package bottom (see case drawing) must be attached to a heat−sinking conduit on the printed circuit board.

1. CML output requires 50 Ω receiver termination resistor to V_{CC} for proper operation.
2. In the differential configuration when the input termination pin (VTCLK, $\overline{\text{VTCLK}}$) are connected to a common termination voltage or left open, and if no signal is applied on CLK and $\overline{\text{CLK}}$ then the device will be susceptible to self−oscillation.

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Table 3. ATTRIBUTES

Characteristics		Value	
Input Default State Resistors	R1, R3 R2	56 kΩ 75 kΩ	
ESD Protection	Human Body Model Machine Model	> 1400 V > 80 V	
Moisture Sensitivity (Note 3)		Pb Pkg	Pb−Free Pkg
	QFN−52	Level 2	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		339	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	$V_{EE} = 0$ V		3.6	V
V_I	Input Voltage	$V_{EE} = 0$ V	$V_{EE} \leq V_I \leq V_{CC}$	3.6	V
V_{INPP}	Differential Input Voltage |CLK − $\overline{CLK}$|	$V_{CC} - V_{EE} \geq 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\|V_{CC} - V_{EE}\|$	V V
I_{in}	Input Current Through R_T (50 Ω Resistor)	Continuous Surge		25 50	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	QFN52		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 5)	0 lfpm 500 lfpm	QFN52	25 19.6	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 8)	QFN52	21	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
4. Maximum Ratings are those values beyond which device damage may occur.
5. JEDEC standard multilayer board – 1S2P (1 signal, 2 power).

Table 5. DC CHARACTERISTICS V_{CC} = 2.375 V 2.625 V and 3.135 V to 3.465 V, V_{EE} = 0 V, T_A = −40°C to +85°C (Notes 6 and 7)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open) V_{CC} = 2.375 V to 2.625 V V_{CC} = 3.135 V to 3.465 V	255 270	290 305	325 340	mA
V_{OH}	Output HIGH Voltage (Notes 6 and 7)	V_{CC} − 40	V_{CC} − 20	V_{CC}	mV
V_{OL}	Output LOW Voltage (Notes 6 and 7) V_{CC} = 2.375 V to 2.625 V V_{CC} = 3.135 V to 3.465 V	V_{CC} − 440 V_{CC} − 490	V_{CC} − 350 V_{CC} − 400	V_{CC} − 290 V_{CC} − 340	mV

DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (See Figures 13 and 15)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1125		V_{CC} − 75	mV
V_{IH}	Single−ended Input HIGH Voltage (Note 7)	V_{th} + 75		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage (Note 7)	V_{EE}		V_{CC} − 150	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (See Figures 14 and 16)

Symbol	Characteristic		Min	Typ	Max	Unit
V_{IHD}	Differential Input HIGH Voltage		1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		V_{EE}		V_{CC} − 75	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 9)		1163		V_{CC} − 37	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})		75		2500	mV
I_{IH}	Input HIGH Current (Termination Pins Open)	CLK[0−1]/$\overline{CLK[0−1]}$ SEL/$\overline{SEL}$	−100 −150	5	100 150	µA
I_{IL}	Input LOW Current (Termination Pins Open)	CLK[0−1]/$\overline{CLK[0−1]}$ SEL/$\overline{SEL}$	−100 −150	5	100 150	µA
R_{TIN}	Internal Input Termination Resistor		45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor		45	50	55	Ω
$R_{Temp\ Coef}$	Internal I/O Termination Resistor Temperature Coefficient			−3.75		mΩ/C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. CML outputs require 50 Ω receiver termination resistors to V_{CC} for proper operation.
7. Input and output parameters vary 1:1 with V_{CC}.
8. V_{th} is applied to the complementary input when operating in single−ended mode.
9. V_{CMR}(MIN) varies 1:1 with V_{EE}, V_{CMR}(MAX) varies 1:1 with V_{CC}.

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Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 2.625 V and 3.135 V to 3.465 V, V_{EE} = 0 V; (Note 10)

Symbol	Characteristic	−40°C Min	−40°C Typ	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{inppmin}$) (See Figures 3, 4, 5, and 6) V_{CC} = 2.375 V to 2.625 V $f_{in} \leq 3$ GHz $f_{in} \leq 5.5$ GHz V_{CC} = 3.135 V to 3.465 V $f_{in} \leq 3$ GHz $f_{in} \leq 5.5$ GHz	240 115 250 130	330 220 350 250		240 115 250 130	330 220 350 250		240 115 250 130	330 220 350 250		mV
f_{DATA}	Maximum Operating Data Rate	5	6		5	6		5	6		Gb/s
t_{PLH}, t_{PHL}	Differential Input−to−Output Propagation Delay @ 1 GHz (See Figures 7 and 11) CLK−Q SEL−Q	200 290	240 340	280 390	200 290	240 340	280 390	200 290	240 340	280 390	ps
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew Device−to−Device Skew (Note 15)		2 10 15	15 20 80		2 10 15	15 20 80		2 10 15	15 20 80	ps
t_{JITTER}	RMS Random Clock Jitter (Note 13) f_{in} = 3 GHz f_{in} = 5.5 GHz Peak−to−Peak Data Dependent Jitter (Note 14) f_{DATA} = 3.125 Gb/s f_{DATA} = 5 Gb/s f_{DATA} = 6.125 Gb/s		0.2 0.2 6 15 15	0.5 0.5 15 25 25		0.2 0.2 6 15 15	0.5 0.5 15 25 25		0.2 0.2 6 15 15	0.5 0.5 15 25 25	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12 and Figures 3, 4, 5, and 6)	75	400	2500	75	400	2500	75	400	2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%)		50	75		50	75		50	75	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Measured by forcing V_{INPP}(MIN) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 1 GHz.
12. V_{INPP}(MAX) cannot exceed V_{CC} − V_{EE}. Input voltage swing is a single−ended measurement operating in differential mode.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS 2^{23}−1.
15. Device−to−device skew is measured between outputs under identical transition and conditions @ 1 GHz.
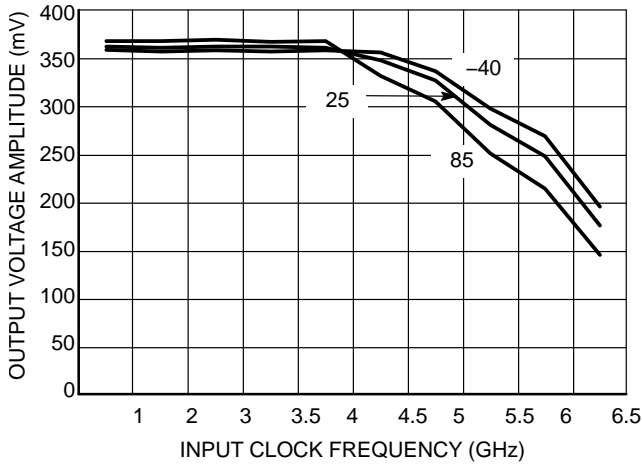
**Figure 3. Output Voltage Amplitude vs. Input
Clock Frequency and Temperature
(V$_{inpp}$ = 400 mV; V$_{CC}$ = 3.3 V)**
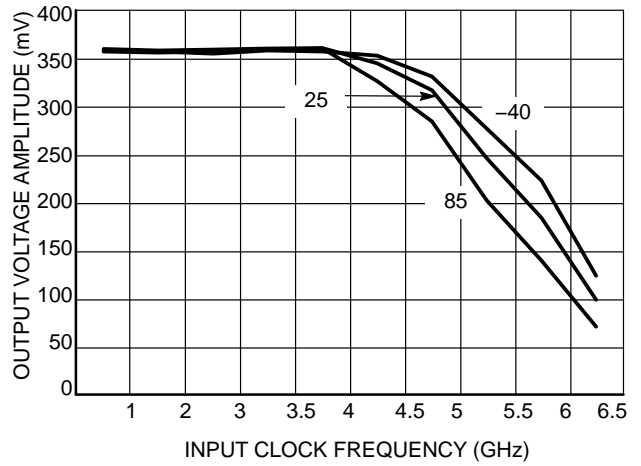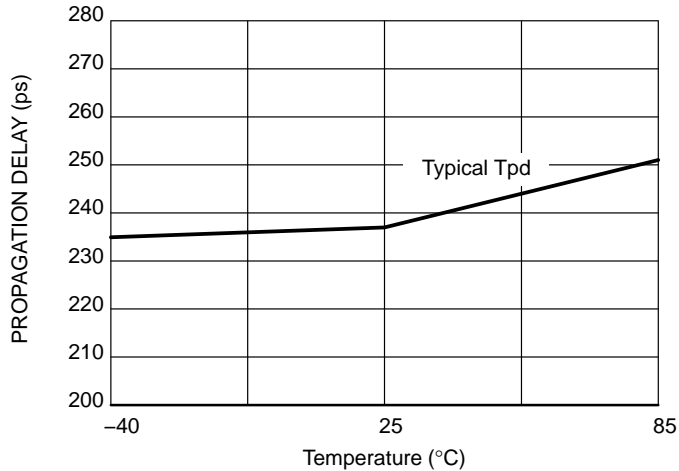
**Figure 4. Output Voltage Amplitude vs. Input
Clock Frequency and Temperature
(V$_{inpp}$ = 75 mV; V$_{CC}$ = 3.3 V)**
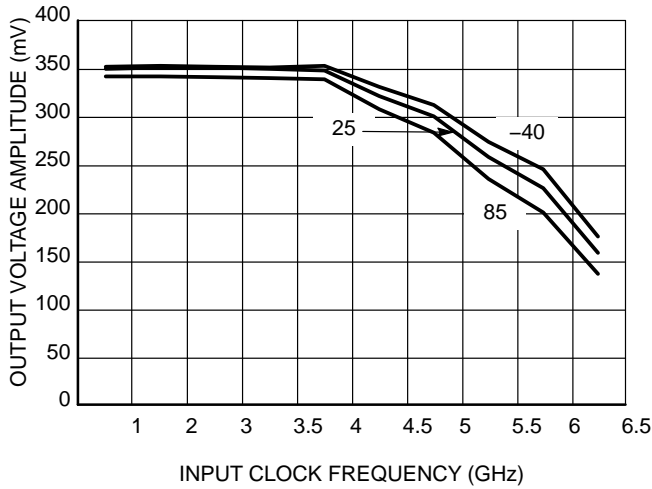
**Figure 5. Output Voltage Amplitude vs. Input
Clock Frequency and Temperature
(V$_{inpp}$ = 400 mV; V$_{CC}$ = 2.5 V)**
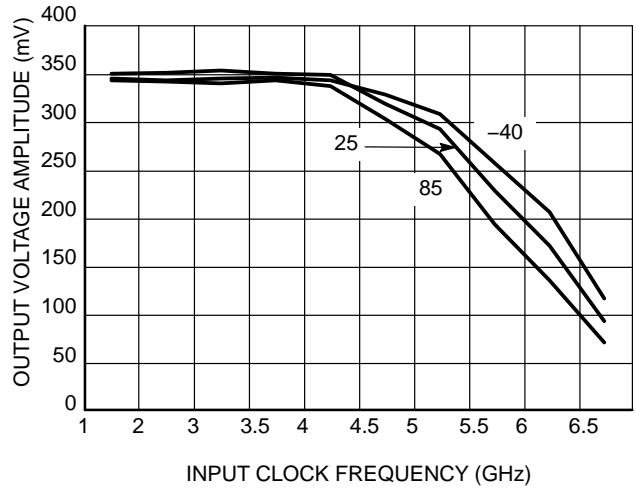
**Figure 6. Output Voltage Amplitude vs. Input
Clock Frequency and Temperature
(V$_{inpp}$ = 75 mV; V$_{CC}$ = 2.5 V)**

Figure 7. Propagation Delay versus Temperature
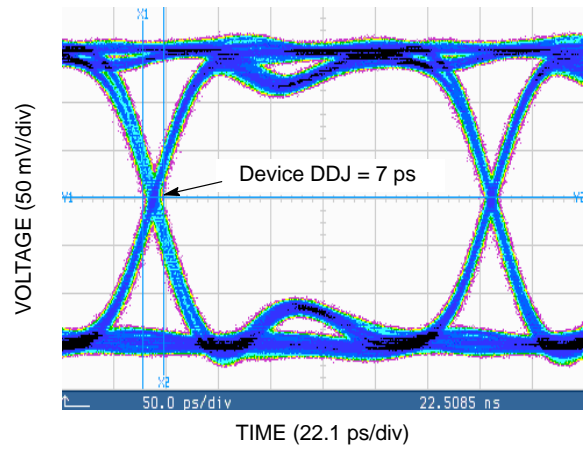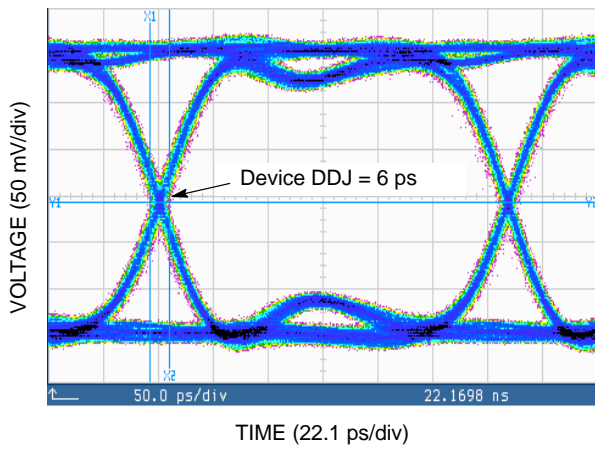
Figure 8. Typical Output Waveform at 3.125 Gb/s with PRBS $2^{23}-1$ (V_{inpp} = 75 mV−left and 400 mV−right)
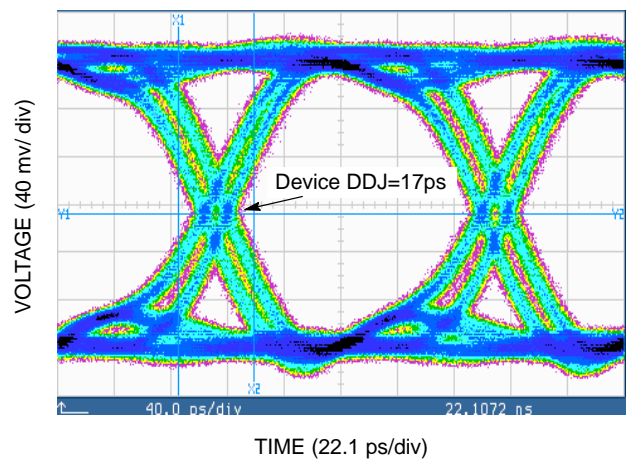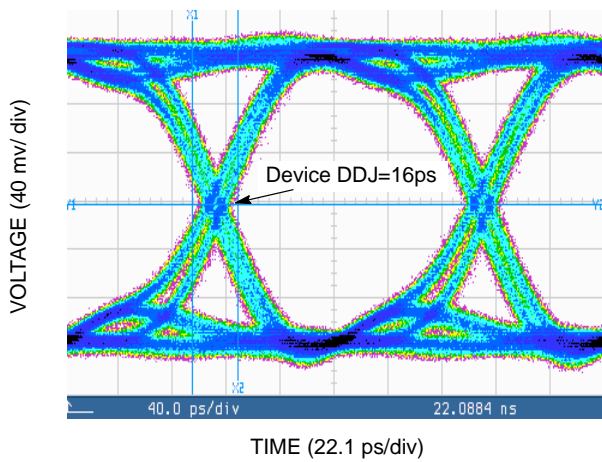
Figure 9. Typical Output Waveform at 5 Gb/s with PRBS $2^{23}-1$ (V_{inpp}=75 mV−left and 400 mV−right)
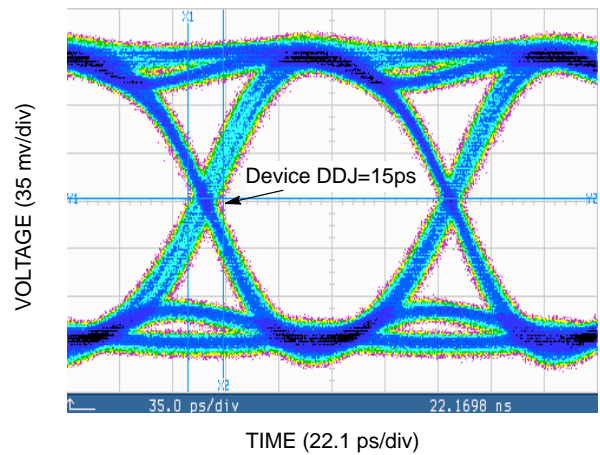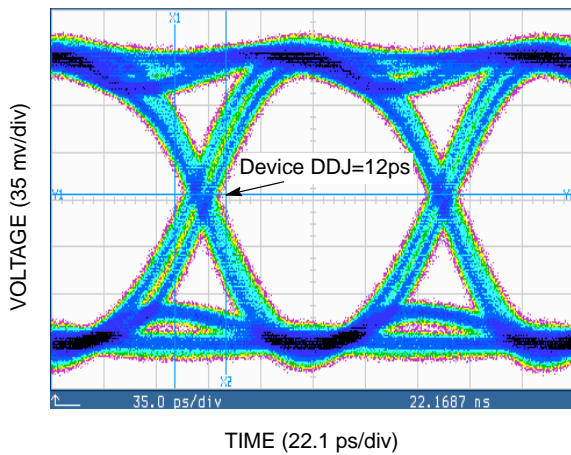
Figure 10. Typical Output Waveform at 6.125 Gb/s with PRBS $2^{23}-1$ (V_{inpp} = 75 mV−left and 400 mV−right)

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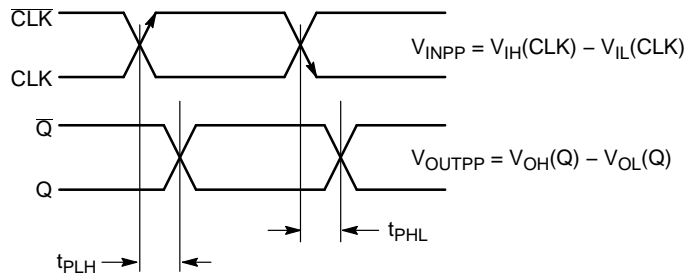
Figure 11. AC Reference Measurement

$V_{INPP} = V_{IH}(CLK) - V_{IL}(CLK)$

$V_{OUTPP} = V_{OH}(Q) - V_{OL}(Q)$
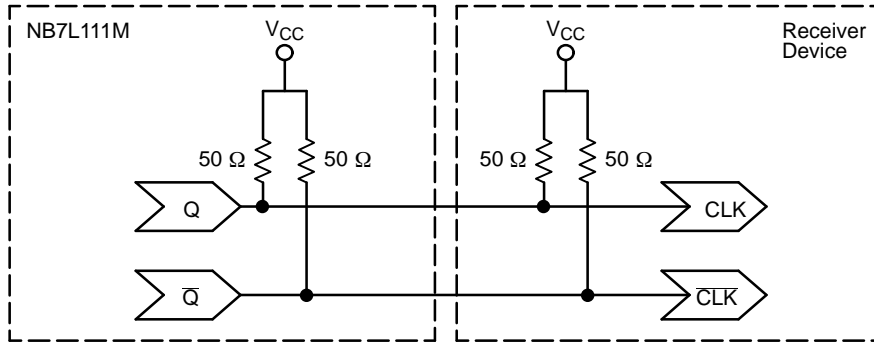
Figure 12. Typical Termination for 16 mA Output Drive and Device Evaluation
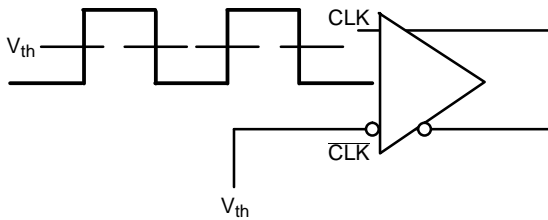
Figure 13. Differential Input Driven Single−Ended
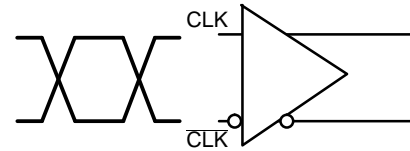
Figure 14. Differential Inputs Driven Differentially
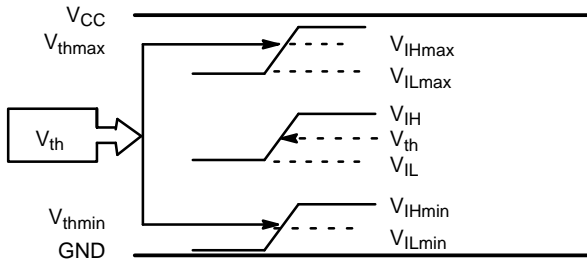
Figure 15. V$_{th}$ Diagram
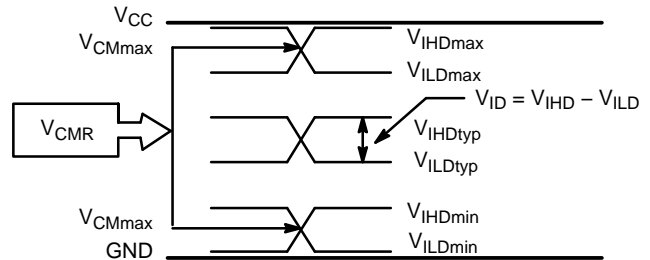
Figure 16. V$_{CMR}$ Diagram

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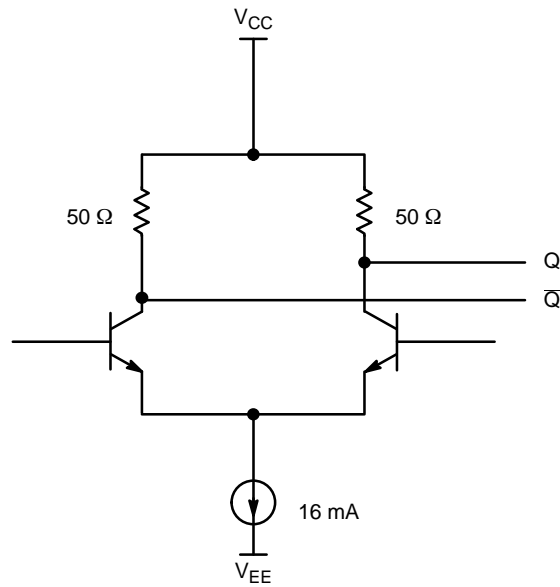
Figure 17. CML Output Structure

Table 7. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK0, $\overline{\text{VTCLK0}}$, VTCLK1, $\overline{\text{VTCLK1}}$, VTSEL, $\overline{\text{VTSEL}}$ to V_{CC}
LVDS	Connect VTCLK0, $\overline{\text{VTCLK0}}$ together for CLK0 input; Connect VTCLK1, $\overline{\text{VTCLK1}}$ together for CLK1 input; Connect VTSEL, $\overline{\text{VTSEL}}$ together for SEL control input.
AC–COUPLED	Bias VTCLK0, $\overline{\text{VTCLK0}}$, VTSEL, $\overline{\text{VTSEL}}$ and VTCLK1, $\overline{\text{VTCLK1}}$ inputs within (VCMR) Common Mode Range.
RSECL, LVPECL	Standard ECL termination techniques. See AND8020.
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs.

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Application Information

All NB7L111M inputs can accept LVPECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV$_{PP}$ and the maximum input swing of 2500 mV$_{PP}$. Within these differential conditions, the input HIGH voltage can range from V$_{CC}$ to 1.2 V. Examples of interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω).
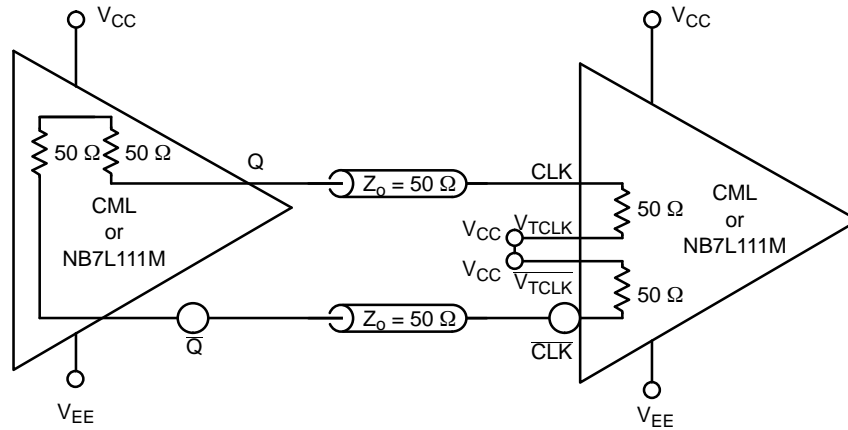
Figure 18. CML to CML Interface

Recommended R$_T$ Values	
V$_{CC}$	R$_T$
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

*V$_{BIAS}$ is within V$_{CMR}$ Range.
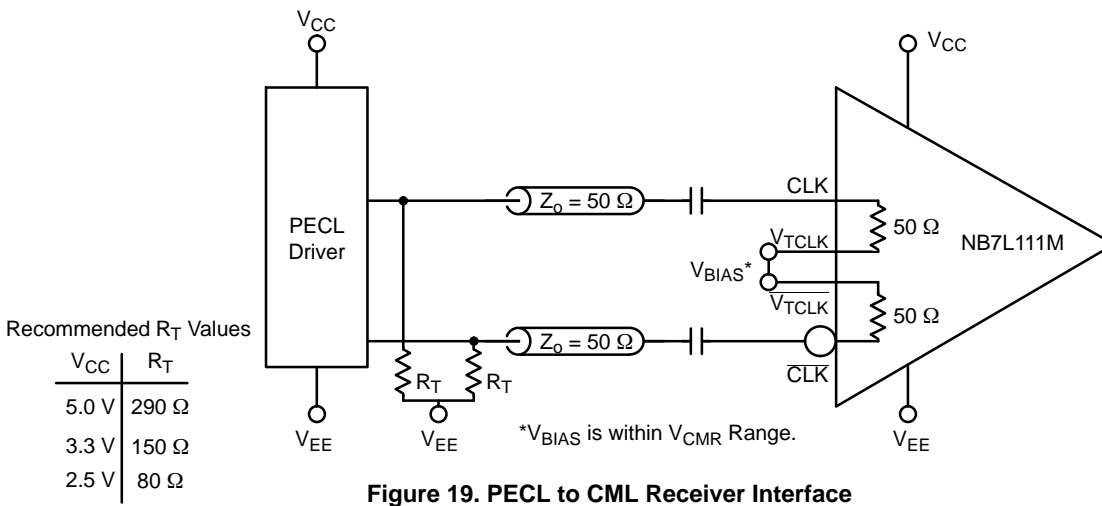
Figure 19. PECL to CML Receiver Interface
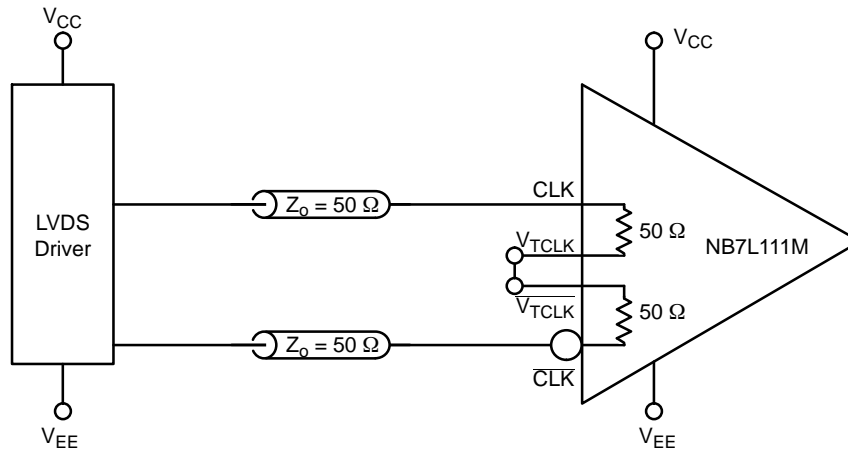
Figure 20. LVDS to CML Receiver Interface

Figure 21. LVCMOS/LVTTL to CML Receiver Interface

Recommended V_{REF} Values

	V_{REF}
LVCMOS	$\dfrac{V_{CC} - V_{EE}}{2}$
LVTTL	1.5 V
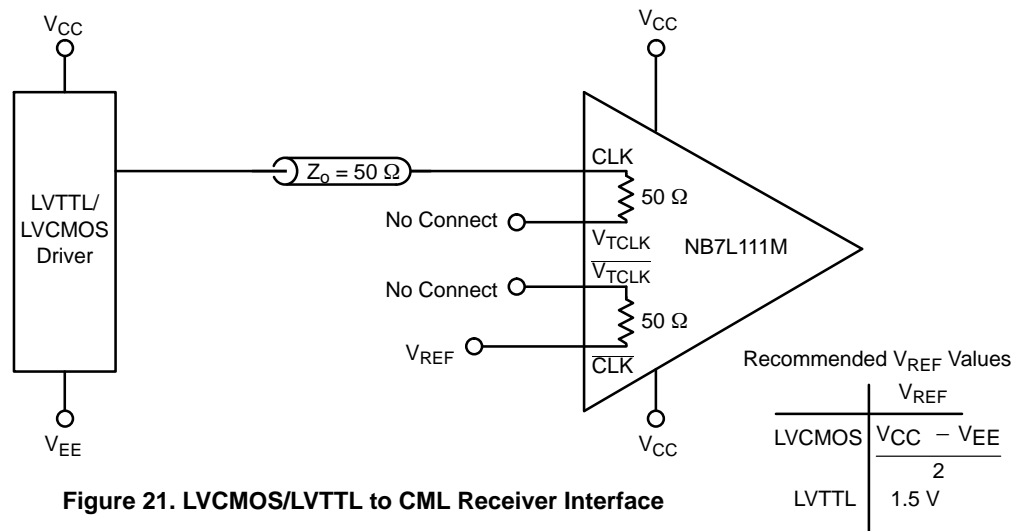
ORDERING INFORMATION

Device	Package	Shipping†
NB7L111MMNG	QFN–52 (Pb–Free)	260 Units / Tray
NB7L111MMNR2G	QFN–52 (Pb–Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

QFN52 8x8, 0.5P
CASE 485M
ISSUE C

PIN ONE REFERENCE

2X △ 0.15 C

2X △ 0.15 C

∥ 0.10 C

△ 0.08 C

SEATING PLANE

A2
A
A1
A3 REF

D2

14 26
13 27
52 X L
E2
1 39
52 X K
52 40
52 X b NOTE 3
e

⊕ 0.10 C A B
0.05 C
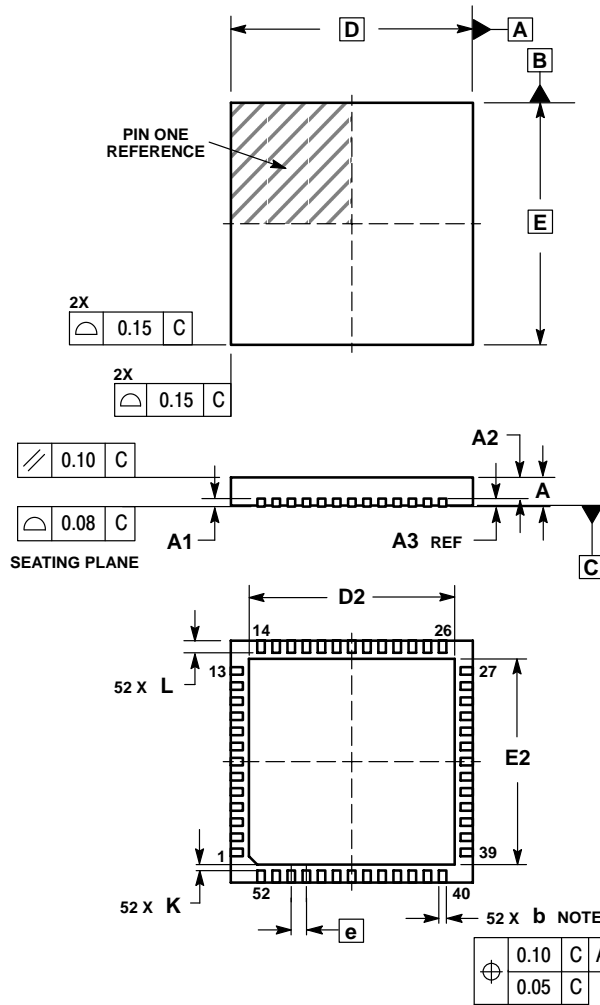
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

RECOMMENDED SOLDERING FOOTPRINT*
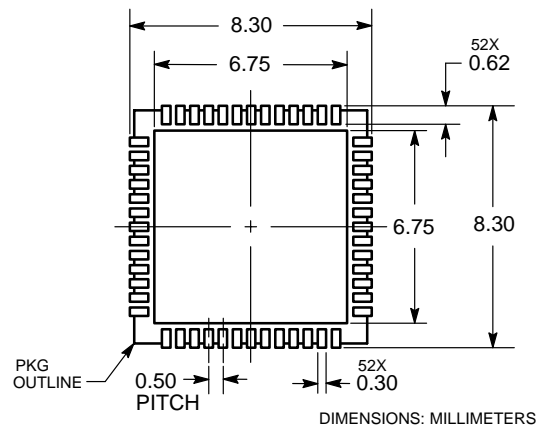
8.30
6.75
52X 0.62
6.75
8.30
PKG OUTLINE
0.50 PITCH
52X 0.30

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Components Industries, LLC (SCILLC).

pubnumber/D