Wide Input Voltage, Synchronous USB Buck Regulator with Remote Load Regulation

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Cable and wiring drop compensation
- Dynamic voltage correction with controller
- Integrated high-side and low-side switching MOSFETs
- Programmable load-side current limit
- Maximized duty cycle for low dropout operation
- Operating input voltage range: 4 V to 36 V
- UVLO STOP threshold is at 2.6 V_{TYP}
- Withstands surge voltages up to 40 V
- Continuous loading: 2.6 A for A8653; 1 A for A8652
- Adjustable switching frequency (f_{SW}): 100 kHz to 2.2 MHz
- Synchronization to external clock: 100 kHz to 2.2 MHz
- Frequency dithering for lower EMI signature
- External adjustable compensation network
- Stable with ceramic output capacitors

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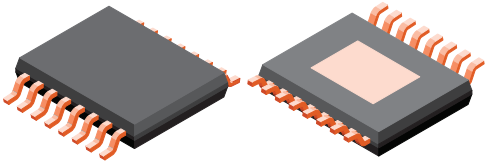
PACKAGES:

16-Pin eTSSOP (suffix LP) with exposed thermal pad



Not to scale

DESCRIPTION

The A8652/53 is a high output current synchronous buck regulator that provides tight load regulation over a wiring harness without the need for remote sense lines. This remote load regulation is achieved with an integrated open-loop correction scheme that, given a known wiring harness resistance, adjusts the output voltage based on the measured load current and a user-programmable gain, achieving ±2% accuracy at 500 mV of correction. The Remote Load Regulation control includes a 115% regulated voltage clamp in conjunction with a dynamic overvoltage protection, with OVP threshold changing with the correction voltage. The A8652/53 includes a user-configurable load-side current limit to fold back the output voltage during an output overcurrent condition. The A8652/53 regulates nominal input voltages from 4 to 36 V and remains operational when V_{IN} drops as low as 2.6 V. When the input voltage approaches the output voltage, the duty cycle is maximized to maintain the output voltage.

The A8652/53 features include externally set soft-start time, external compensation network, an EN input to enable V_{OUT}, a SYNC/FSET input to synchronize or set the PWM switching

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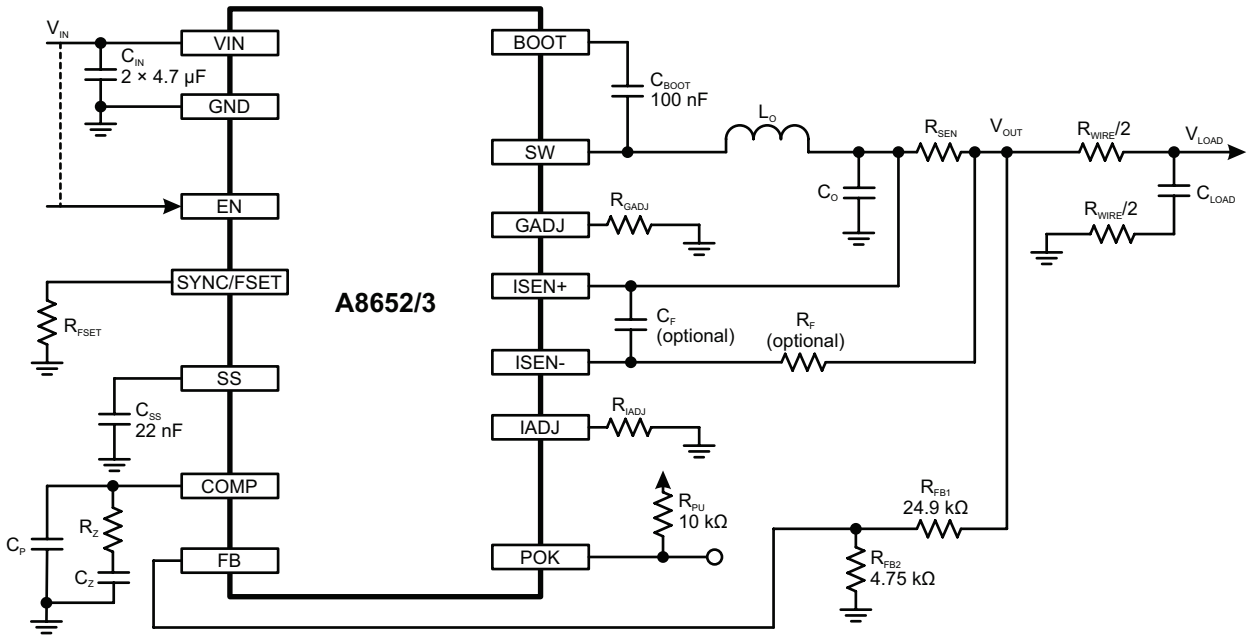
APPLICATIONS

- Automotive USB Power Ports
- Rear Seat Entertainment
- Navigation Systems
- Motorcycle Clusters



Typical Application Diagram 1

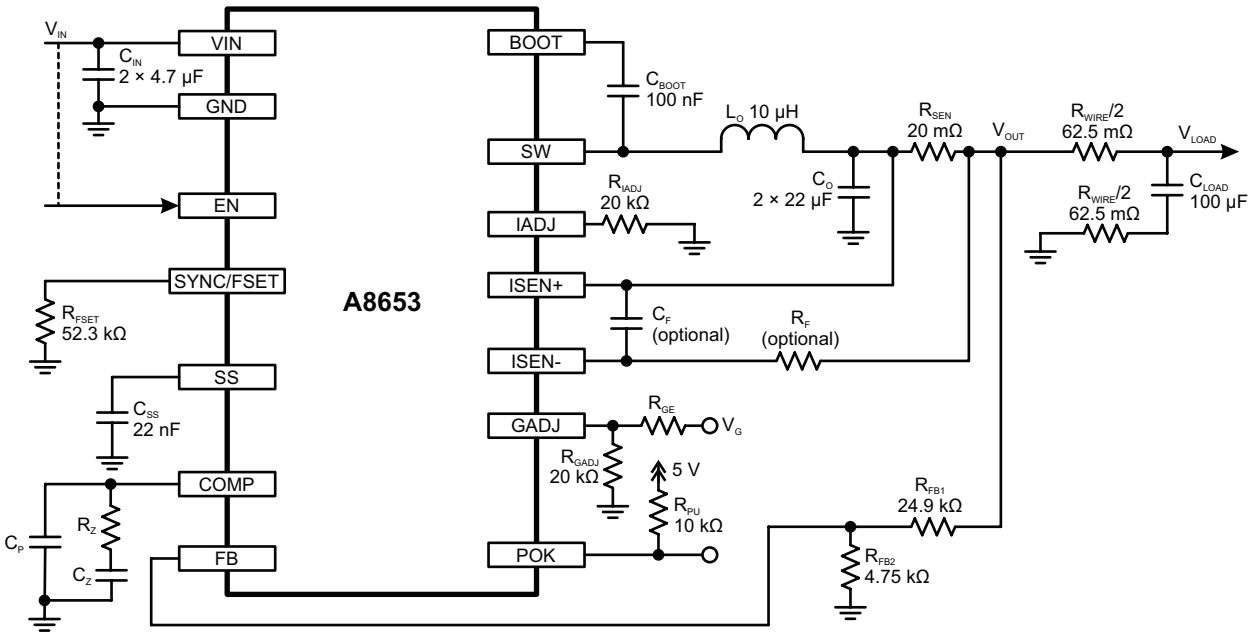
FEATURES AND BENEFITS (continued)

- Pre-bias startup compatible
- Power OK (POK) output
- Dynamic overvoltage protection, pulse-by-pulse current limit, hiccup mode short-circuit, and thermal protections
- Open-circuit and adjacent pin short-circuit tolerant
- Short-to-ground tolerant at every pin
- USB3 charging capability: 2.6 A (A8653)
- USB2 capability: 1 A (A8652)

DESCRIPTION (continued)

frequency, and a Power OK output to indicate when V_{OUT} is within regulation and there is no load-side current limit condition. Protection features include V_{IN} undervoltage lockout, pulse-by-pulse current limit, hiccup mode short-circuit protection, dynamic overvoltage protection, and thermal shutdown. The A8652/53 provides open-circuited, adjacent pin short-circuit, and short-to-ground protection at every pin to satisfy the most demanding automotive and non-automotive applications.

The A8652/53 device is available in a 16-pin eTSSOP package with exposed pads for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte-tin lead frame plating. The maximum junction temperature ($T_{J(max)}$) is 150ºC.



Typical Application Diagram 2 with Dynamic Voltage Correction Control at Pin GADJ

Selection Guide

Part Number	Packing	Package
A8652KLPTR-T	4000 pieces per 13-inch reel	4.4 mm × 5 mm, 1.2 mm nominal height 16-pin eTSSOP with exposed thermal pad
A8653KLPTR-T		

SPECIFICATIONS

Absolute Maximum Ratings[1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN, SS			–0.3 to 40	V
SW to GND [2]	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		V_{IN} ≤ 36 V, t < 50 ns	–1 to V_{IN} + 2	V
BOOT Pin Above SW Pin	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		< 1 ms	V_{SW} – 0.3 to V_{SW} + 7	V
ISEN+ and ISEN– Pins		ISEN+ and ISEN– Pins	–0.3 to 6.5	V
ISEN+ to ISEN– Differential Voltage			–0.3 to 0.3	V
All other pins			–0.3 to 5.5	V
Maximum Junction Temperature	$T_{J(max)}$		150	ºC
Storage Temperature Range	T_{stg}		–55 to 150	ºC

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

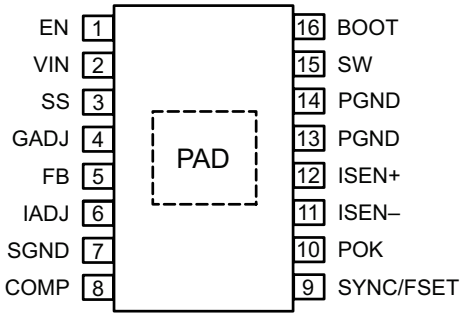
[2] SW has internal clamp diodes to GND and VIN. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limits.

Thermal Characteristics

Characteristic	Symbol	Test Conditions[3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP Package, 4-layer PCB based on JEDEC standard	34	ºC/W

[3] Additional thermal information available on the Allegro website.

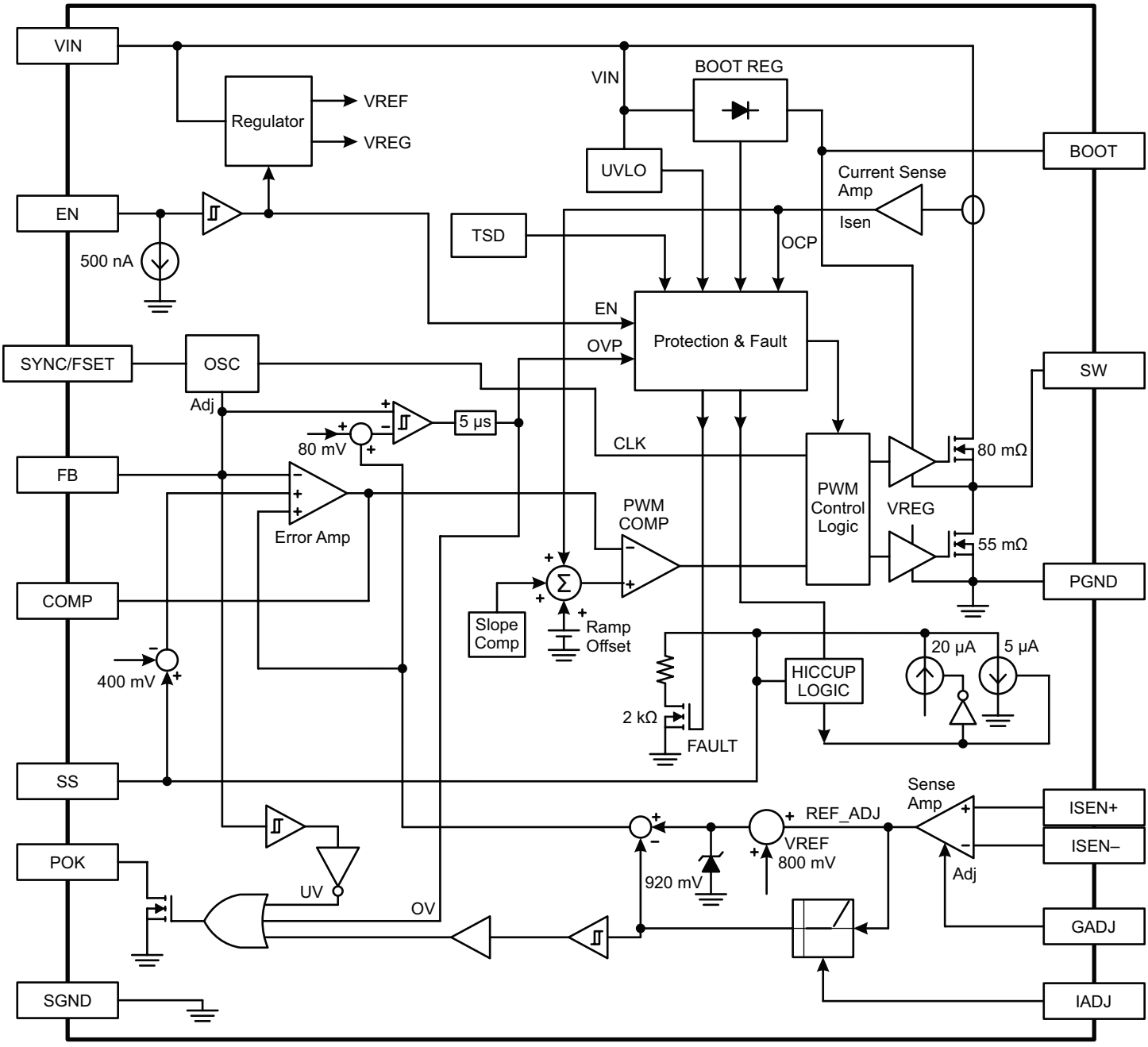
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 16-Pin eTSSOP Pinout Diagram

Terminal List Table

Symbol	Number	Function
EN	1	Enable input. This pin is used to turn the converter on or off: set this pin high to turn the converter on or set this pin low to turn the converter off. May be connected to VIN.
VIN	2	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. A high quality ceramic capacitor should be placed very close to this pin.
SS	3	Soft-Start pin. Connect a capacitor, C_{SS}, from this pin to GND to set the soft-start time. This capacitor also determines the hiccup period during overcurrent.
GADJ	4	This pin is used to set the gain of the differential current sense amplifier with ISEN+/ISEN– pins. A resistor from this pin to GND set the amplifier gain. Together with load sense resistor, it sets the desired voltage correction at the specified load condition. Grounding GADJ disables Remote Load Regulation function.
FB	5	Feedback (negative) input to the error amplifier. Connect a resistor divider from the converter output node (V_{OUT}) to this pin to program the output voltage.
IADJ	6	Active current limit adjust pin. A resistor from this pin to GND sets the current limit. When the load current exceeds this limit, the output voltage will decrease at the predefined slope.
SGND	7	Signal (quiet) GND.
COMP	8	Output of the error amplifier and compensation node for the control loop. Connect a series RC network from this pin to GND for loop compensation.
SYNC/FSET	9	Frequency setting and synchronization pin. A resistor, R_{FSET}, from this pin to GND sets the PWM switching frequency.
POK	10	Power OK output signal. This pin is an open-drain output that transitions from low impedance to high impedance when the output is within the final regulation voltage and no load side current limit exists.
ISEN–	11	Negative current-sensing pin to the internal current sense amplifier, connected to the load side of the external current sensing resistor.
ISEN+	12	Positive current-sensing pin to the internal current sense amplifier, connected to the inductor side of the external current sensing resistor.
PGND	13, 14	Power GND.
SW	115	The source of the high-side N-channel MOSFET. The output inductor (L_O) should be connected to this pin. L_O should be placed as close as possible to this pin and connected with relatively wide traces.
BOOT	16	High-side gate drive boost input. Connect a 100 nF ceramic capacitor from BOOT to SW.
PAD	–	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.



Functional Block Diagram

ELECTRICAL CHARACTERISTICS: Valid at 4 V ≤ V_{IN} ≤ 36 V; T_A = 25ºC; • indicates specifications guaranteed –40°C ≤ T_A = T_J ≤ 150°C (unless noted otherwise).

Characteristics	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS								
Operating Input Voltage Range [2]	V_{IN}			•	4	–	36	V
UVLO Start Threshold	$V_{UVLO(START)}$	V_{IN} rising			–	3.4	3.7	V
UVLO Stop Threshold	$V_{UVLO(STOP)}$	V_{IN} falling			–	2.6	2.9	V
UVLO Hysteresis	$V_{UVLO(HYS)}$				–	800	–	mV
INPUT CURRENTS								
Input Quiescent Current [1]	I_Q	V_{EN} = 5 V, V_{FB} = 1 V, no PWM switching		•	–	3	6.5	mA
Input Sleep Supply Current [1]	I_{QSLEEP}	V_{IN} = 12 V, V_{EN} ≤ 0.4 V, –40°C < T_A = T_J < 85°C			–	1	240	µA
		V_{IN} = 12 V, V_{EN} ≤ 0.4 V, T_A = T_J = 125°C			–	40	900	µA
VOLTAGE REGULATION								
Feedback Voltage Accuracy [3]	V_{FB}	V_{FB} = V_{COMP}, V_{GADJ} = 0 V, –40°C < T_A = T_J < 125°C			792	800	808	mV
		V_{FB} = V_{COMP}, V_{GADJ} = 0 V		•	788	800	812	mV
Feedback Voltage Accuracy with Cable Compensation [3]	$V_{FB(ACC)}$	V_{FB} = V_{COMP}, V_{ISEN+} – $V_{ISEN–}$ = 25 mV, V_{OUT} = 5 V, R_{GADJ} = 20 kΩ, R_{IADJ} = 20 kΩ		•	808	825	842	mV
Error Amp Clamp Voltage [3]	$V_{FB(CLAMP)}$	V_{FB} = V_{COMP}, V_{ISEN+} – $V_{ISEN–}$ = 55 mV, V_{OUT} =5 V, R_{GADJ} = 7.5 kΩ, R_{IADJ} = 20 kΩ			900	920	940	mV
Output Voltage Setting Range [3]	V_{OUT}				3.3	–	5.75	V
Output Dropout Voltage [3]	$V_{O(PWM)}$	V_{IN} = 5.7 V, I_O = 2.6 A, f_{SW} = 500 kHz	A8653	•	4.9	–	–	V
		V_{IN} = 7.3 V, I_O = 2.6 A, f_{SW} = 2 MHz		•	4.9	–	–	V
		V_{IN} = 5.5 V, I_O = 1 A, f_{SW} = 500 kHz	A8652	•	4.9	–	–	V
		V_{IN} = 6.8 V, I_O = 1 A, f_{SW} = 2 MHz		•	4.9	–	–	V
ERROR AMPLIFIER								
Feedback Input Bias Current [1]	I_{FB}				–100	–	–8	nA
Open-Loop Voltage Gain	A_{VOL}	V_{COMP} = 1.2 V			–	65	–	dB
Transconductance	gm_{EA}	400 mV < V_{FB}			550	750	950	µA/V
		0 V < V_{FB} < 400 mV			275	375	475	
Output Current	I_{EA}	V_{COMP} = 1.2 V			–	±75	–	µA
INTERNAL MOSFET PARAMETERS								
High-Side MOSFET On-Resistance [3]	$R_{DSON(HS)}$	T_A = 25°C, I_{DS} = 100 mA			–	80	–	mΩ
SW Node Rising Slew Rate	dV/dt	12 V < V_{IN} < 16 V			–	0.75	–	V/ns
SW Leakage [1]	$I_{SW(LEAK)}$	V_{EN} ≤ 0.4 V, V_{SW} = 5 V, V_{IN} = 12 V, T_J = 25°C			–10	0	10	µA
Low-Side MOSFET On-Resistance [3]	$R_{DSON(LS)}$	T_A = 25°C, I_{DS} = 100 mA			–	55	–	mΩ

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ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 36 V; T_A = 25ºC; • indicates specifications guaranteed –40°C ≤ T_A = T_J ≤ 150°C (unless noted otherwise).

Characteristics	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
OSCILLATOR								
PWM Switching Frequency	f_{SW}	R_{FSET} = 261 kΩ			–	100	–	kHz
		R_{FSET} = 61.9 kΩ			375	415	457	kHz
		R_{FSET} = 10.5 kΩ			–	2000	–	kHz
PWM Frequency Dithering	f_{DITHER}	No dithering with FSET synchronization			–	±13	–	%
Minimum Controllable On-Time	$t_{ON(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A			–	95	135	ns
Minimum Switch Off-Time	$t_{OFF(MIN)}$	V_{IN} = 12 V, I_{OUT} = 1 A			–	100	135	ns
FSET SYNCHRONIZATION TIMING								
Synchronization Frequency Range	f_{SW_MULT}				100	–	2200	kHz
Synchronization Input Off-Time	t_{SYNC_OFF}				0.2	–	1.3	µs
Synchronization Input Rise Time[3]	$t_{r(SYNC)}$				–	10	15	ns
Synchronization Input Fall Time[3]	$t_{f(SYNC)}$				–	10	15	ns
Synchronization Rising Threshold	$V_{SYNC(HI)}$	V_{SYNC} rising			–	–	2	V
Synchronization Falling Threshold	$V_{SYNC(LO)}$	V_{SYNC} falling			0.5	–	0.7	V
CURRENT LOOP								
Peak Inductor (Pulse-by-Pulse) Current Limit	$I_{PK\_LIM(MINON)}$	t_{ON} = $t_{ON(MIN)}$	A8653	•	3.3	4	4.62	A
			A8652	•	1.5	1.8	2.1	A
	$I_{PK\_LIM(MINOFF)}$	t_{ON} = 1/f_{SW} – $t_{OFF(MIN)}$, No Sync	A8653	•	2.4	3.2	4	A
			A8652	•	0.9	1	1.5	A
Load-Side Current Limit	I_{OUT_LIM}	R_{IADJ} = 20 kΩ, R_{SEN} = 20 mΩ, V_{OUT} = 5 V	A8653		2.5	3	3.3	A
			A8652		1	1.2	1.4	A
COMP to SW Current Gain	gm_{POWER}		A8653		–	6.3	–	A/V
			A8652		–	3.2	–	A/V
Slope Compensation	S_E	R_{FSET} = 261 kΩ, 100 kHz	A8653		–	0.056	–	A/µs
		R_{FSET} = 61.9 kΩ, 415 kHz			0.09	0.24	0.43	A/µs
		R_{FSET} = 10.5 kΩ, 2 MHz			–	1.3	–	A/µs
		R_{FSET} = 261 kΩ, 100 kHz	A8652		–	0.035	–	A/µs
		R_{FSET} = 61.9 kΩ, 415 kHz			0.07	0.15	0.23	A/µs
		R_{FSET} = 10.5 kΩ, 2 MHz			–	0.8	–	A/µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 36 V; T_A = 25ºC; • indicates specifications guaranteed –40°C ≤ T_A = T_J ≤ 150°C (unless noted otherwise).

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SOFT-START							
SS FAULT/HICCUP Reset Voltage	$V_{SS(RST)}$	V_{SS} falling due to $R_{SS(FLT)}$		–	200	275	mV
SS Maximum Charge Voltage	$V_{SS(MAX)}$			–	3.3	–	V
SS Startup (Source) Current [1]	$I_{SS(SU)}$	HICCUP = FAULT = 0		–30	–20	–10	µA
SS Hiccup (Sink) Current [1]	$I_{SS(HIC)}$	HICCUP = 1		1	2.2	5	µA
SS Pull-Down Resistance	$R_{SS(FLT)}$	FAULT = 1 or EN = 0		–	2	–	kΩ
SS Switching Frequency	f_{SS}	0 V < V_{FB} < 200 mV		–	f_{SW}/4	–	–
		200 mV < V_{FB} < 400 mV		–	f_{SW}/2	–	–
		400 mV < V_{FB}		–	f_{SW}	–	–
HICCUP MODE							
Hiccup OCP Enable Threshold	$V_{HIC(EN)}$	V_{SS} rising		–	2.3	–	V
Hiccup, OCP Count	OCP_{LIM}	V_{SS} > 2.3 V, OCP pulses		–	240	–	counts
Hiccup, BOOT Shorted Count	$BOOT_{UV}$			–	64	–	counts
Hiccup, BOOT Open Count	$BOOT_{OPEN}$			–	7	–	counts
POWER OK (POK) OUTPUT							
POK Output Voltage	V_{POK}	I_{POK} = 4 mA		–	–	0.4	V
POK Leakage [1]	$I_{POK(LEAK)}$	V_{POK} = 5 V	•	–	–	5	µA
POK UV Threshold	$V_{POK(UV)}$	V_{FB} falling	•	715	740	760	mV
POK UV Hysteresis	$V_{POK(UV,HYS)}$			–	10	–	mV
POK OV Threshold	$V_{POK(OV)}$	V_{FB} rising, V_{GADJ} = 0 V		840	880	920	mV
		V_{FB} rising, V_{ISEN+} – $V_{ISEN–}$ = 25 mV, V_{OUT} = 5 V, R_{GADJ} = 20 kΩ, R_{IADJ} = 20 kΩ		865	905	950	mV
		V_{FB} rising, V_{ISEN+} – $V_{ISEN–}$ = 55 mV, V_{OUT} = 5 V, R_{GADJ} = 7.5 kΩ, R_{IADJ} = 20 kΩ		–	1	–	V
POK OV Hysteresis	$V_{POK(OV,HYS)}$			–	10	–	mV
ISEN+ OV Threshold	$V_{ISEN(OV)}$	I_{SEN+} rising, V_{GADJ} = 0 V		5.4	5.65	6	V
		I_{SEN+} rising, V_{ISEN+} – $V_{ISEN–}$ = 25 mV, V_{OUT} = 5 V, R_{GADJ} = 20 kΩ, R_{IADJ} = 20 kΩ		5.6	5.8	6.1	V
		I_{SEN+} rising, V_{ISEN+} – $V_{ISEN–}$ = 55 mV, V_{OUT} = 5 V, R_{GADJ} = 7.5 kΩ, R_{IADJ} = 20 kΩ		–	6.45	–	V
ISEN+ OV Hysteresis	$V_{ISEN(OV,HYS)}$			–	60	–	mV
POK Delay	$t_{d(POK)}$	V_{FB} rising only		–	7	–	PWM cycles
THERMAL PROTECTION							
TSD Rising Threshold	TSD	PWM stops immediately and COMP is pulled low and SS is reset		155	170	185	ºC
TSD Hysteresis [3]	TSD_{HYS}			–	20	–	ºC

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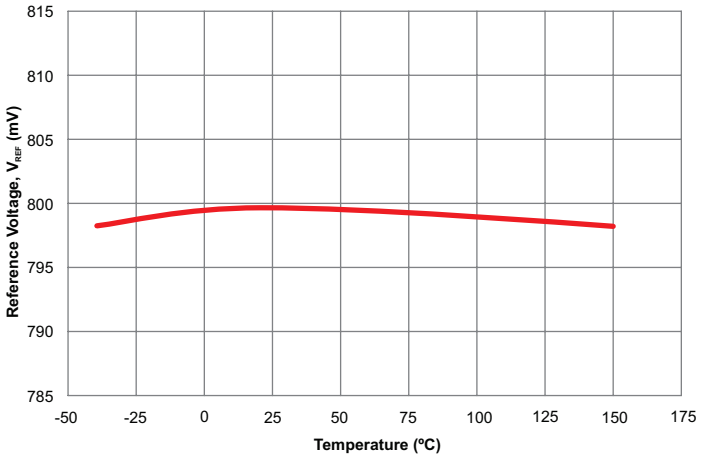
ELECTRICAL CHARACTERISTICS (continued): Valid at 4 V ≤ V_{IN} ≤ 36 V; T_A = 25ºC; • indicates specifications guaranteed –40°C ≤ T_A = T_J ≤ 150°C (unless noted otherwise).

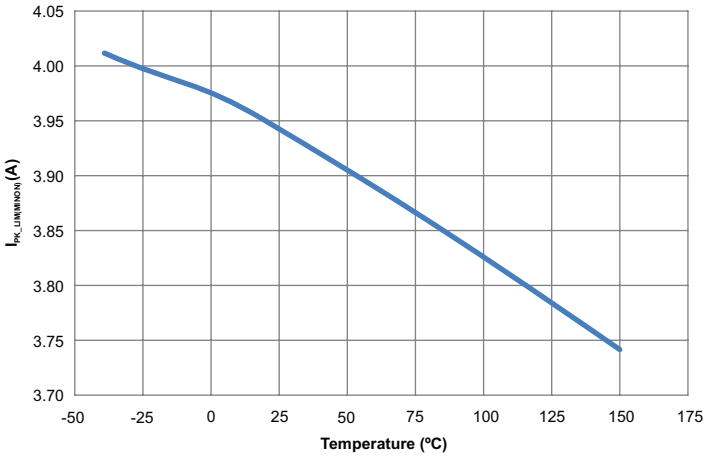
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
EN INPUT THRESHOLDS							
EN High Threshold	$V_{EN(H)}$	EN rising		–	1.41	2	V
EN Low Threshold	$V_{EN(L)}$	EN falling		0.7	1.36	–	V
EN Delay	$t_{d(EN)}$	EN transitioning low, V_{OUT} < 25%		–	60	–	PWM cycles
EN Input Bias Current [1]	I_{EN_BIAS}	EN = 5 V		–	500	–	nA

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin or node.
[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[3] Ensured by design and characterization, not production tested.

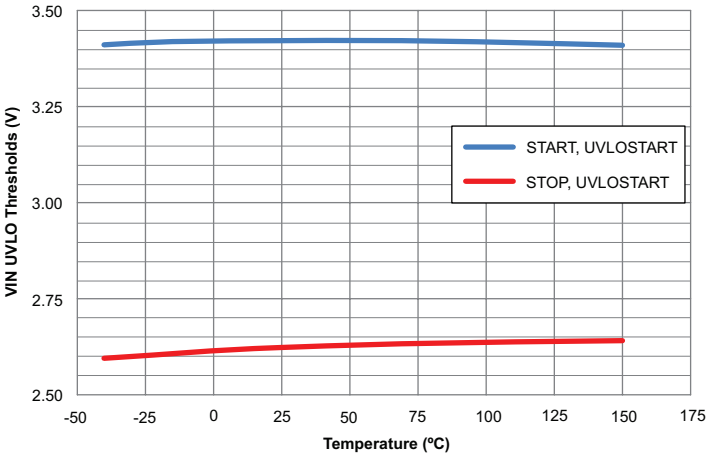
TYPICAL PERFORMANCE CHARACTERISTICS



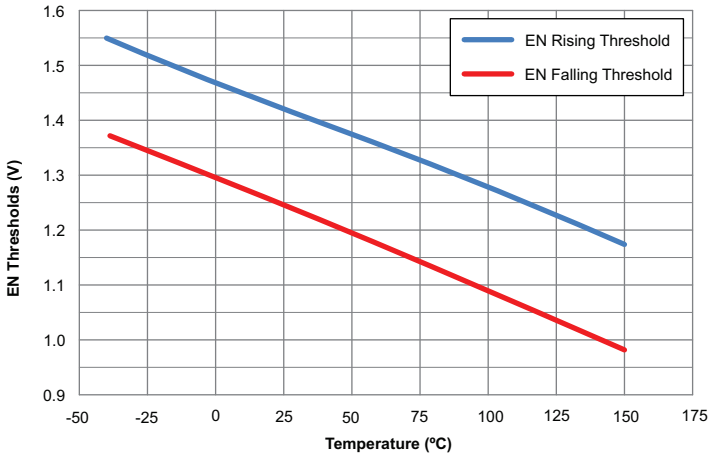
Reference Voltage versus Temperature



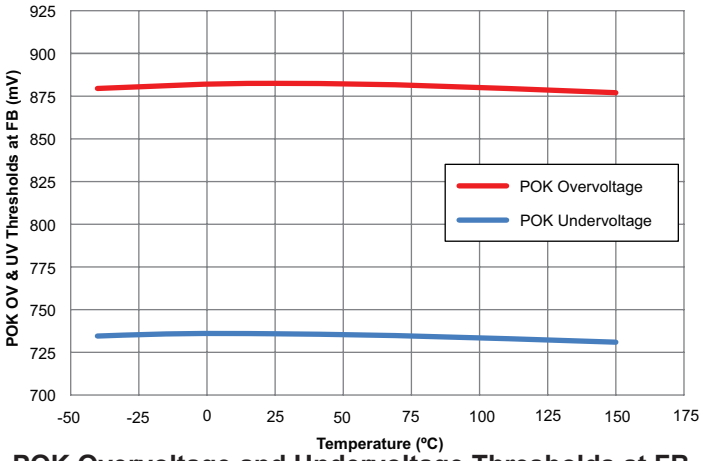
Pulse-by-Pulse Current Limit at $t_{ON(MIN)}$ ($I_{PK\_LIM(MINON)}$) versus Temperature



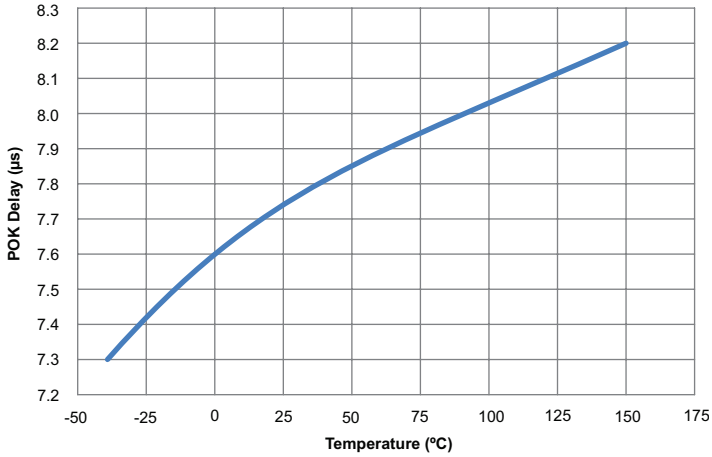
VIN UVLO START and STOP Thresholds versus Temperature



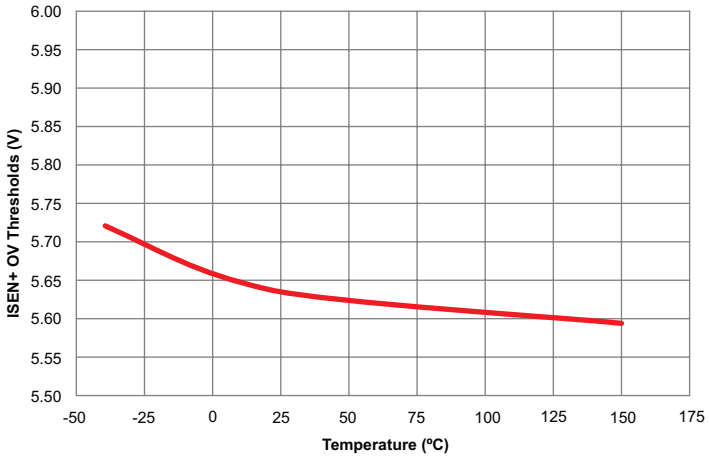
EN Rising and Falling Thresholds versus Temperature



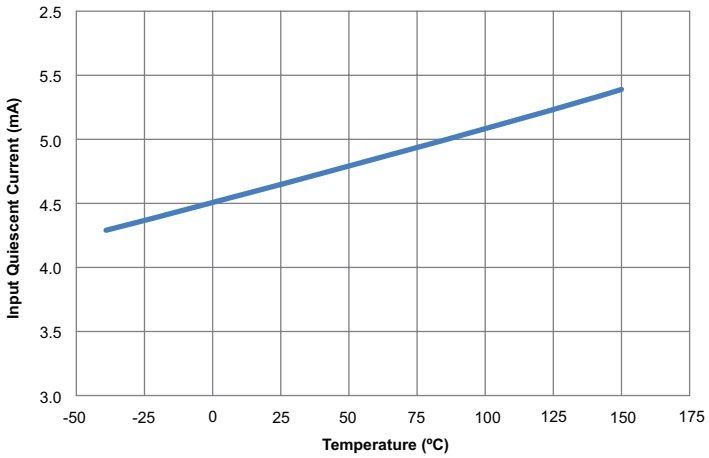
POK Overvoltage and Undervoltage Thresholds at FB versus Temperature (POK OV test with V_{GADJ} = 0 V)



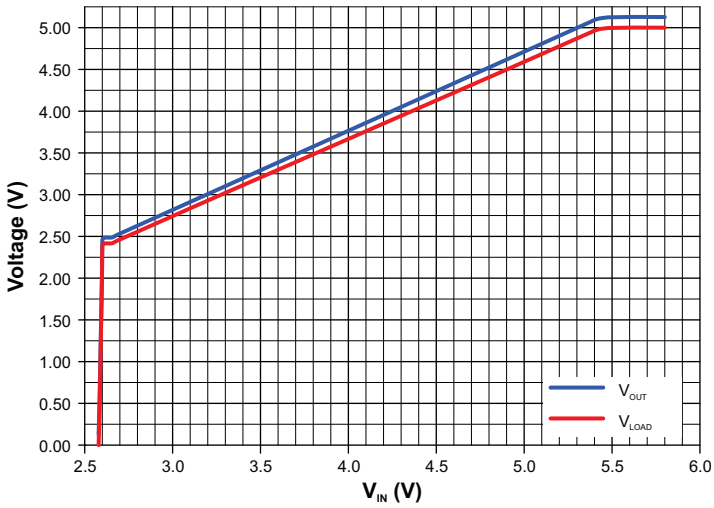
POK Delay Time versus Temperature



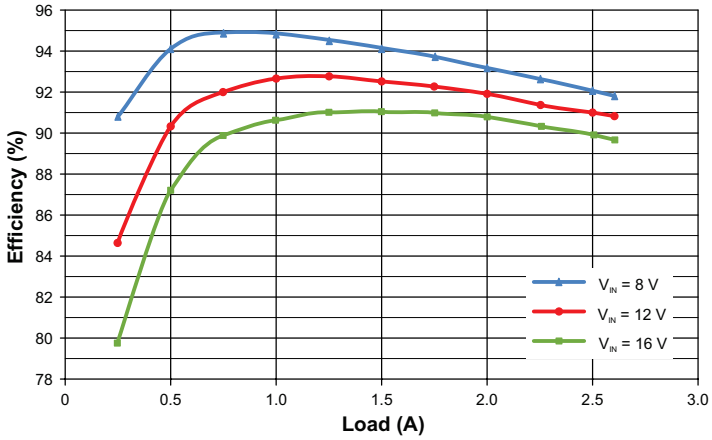
ISEN+ Overvoltage Thresholds versus Temperature (test with V_{GADJ} = 0 V)



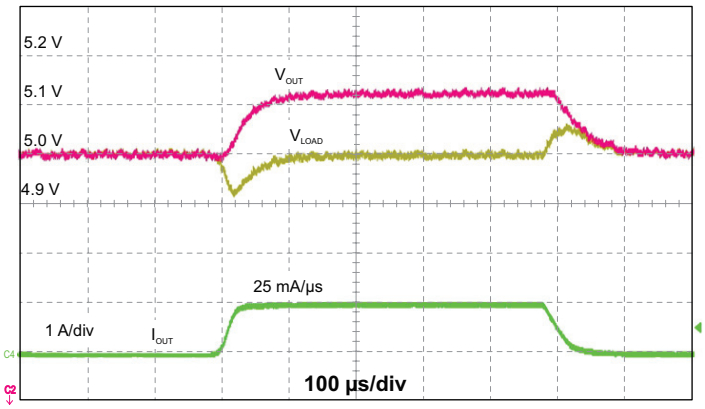
Quiescent Current I_Q versus Temperature



Low V_{IN} Dropout Operation at 5 Ω Load

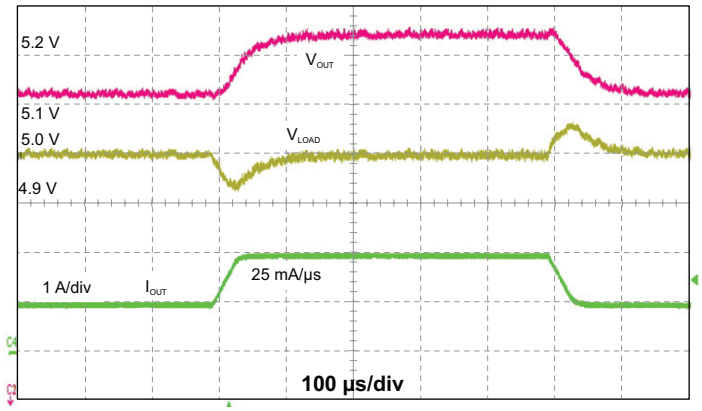


Efficiency versus Output Current (Typical Design A in Table 3)



Transient Response 0 to 1 A Load Step

(Typical Design A in Table 3)



Transient Response 1 to 2 A Load Step

(Typical Design A in Table 3)

FUNCTIONAL DESCRIPTION

Overview

The A8652/53 is a synchronous PWM buck regulator that integrates low $R_{DS(on)}$ high-side and low-side N-channel MOSFETs. It is designed to remain operational when input voltage falls as low as 2.6 V. The A8652/53 employs peak current mode control to provide superior line and load regulation, pulse-by-pulse current limit, fast transient response and simple compensation. The A8652/53 incorporates a Cable Drop Compensation (Remote Load Regulation) function in its current mode control architecture to adjust the output voltage according to the load current, offsetting the voltage drop introduced by the wiring harness. The reference voltage in the feedback loop is adjusted relative to the voltage across the sensing resistor at the load side. When the load current increases, it causes the reference voltage at the error amplifier to increase and the output voltage to follow. The gain of the voltage correction is configurable using the GADJ and IADJ pins. Such features provide flexibility in setting the amount of output voltage correction and the load current limit.

The features of the A8652/53 include Remote Load Regulation, an internal precision reference, an adjustable switching frequency, a transconductance error amplifier, an enable input, integrated top and bottom switching MOSFETs, adjustable soft-start time, pre-bias startup, and a Power OK output. Protection features of A8652/53 include V_{IN} undervoltage lockout, pulse-by-pulse overcurrent protection, BOOT overvoltage and undervoltage protection, hiccup mode short-circuit protection, dynamic overvoltage protection, and thermal shutdown. In addition, the A8652/53 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short-circuit protection.

Reference Voltage

The A8652/53 incorporates an internal precision reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is ±1% from –40°C to 125°C and ±1.5% across from –40°C to 150°C when the Remote Load Regulation is disabled. The output voltage of the regulator is programmed with a resistor divider between V_{OUT} and the FB pin of the A8652/53.

Oscillator/Switching Frequency and Synchronization

The PWM switching frequency of the A8652/53 is adjustable from 100 kHz to 2.2 MHz and has an accuracy of about ±10% over the operating temperature range. Connecting a resistor from the FSET/SYNC pin to GND, as shown in the Applications Schematic, sets the switching frequency. An FSET resistor with ±1% tolerance is recommended. A graph of switching frequency versus FSET resistor value is shown in the Component Selection section of this datasheet. The A8652/53 will suspend operation if the FSET pin is shorted to GND or left open.

FSET/SYNC pin also can be used as a synchronization input that accepts an external clock to switch the A8652/53 from 100 kHz to 2.2 MHz and scales the slope compensation according to the synchronization frequency. When being used as a synchronization input, the applied clock pulses must satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics shown in this datasheet.

Remote Load Regulation Control and Transconductance Error Amplifier

The Remote Load Regulation control in the A8652/53 provides improved load regulation at the remote load by increasing the voltage reference of the error amplifier to correct for the voltage drop introduced by wiring harness to the load. The amount of voltage correction is user-programmable with external configuration resistors, allowing the A8652/53 to be applied to wiring harnesses that have up to 750 mV IR drops at full load. The Remote Load Regulation controller has a variety of protection features, including a load-side current limit, a maximum regulation voltage, and protection in the event of open pin or shorted pin conditions.

The Remote Load Regulation voltage correction and protection features interface with the error amplifier, which is a four-terminal input device with three positive inputs and one negative input, as shown in Figure 1. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The error amplifier performs an “analog OR” selection between its positive inputs, operating according to the positive input with the lowest potential. The three positive inputs are used for soft-start, steady-state regulation, and the 15% maximum regulation voltage. The error amplifier regulates to the soft-start pin voltage minus 400 mV during startup, the sum of A8652/53 internal reference (VREF) and the Remote Load Regulation correction (REF_ADJ) during normal operation, or the 920 mV maximum.

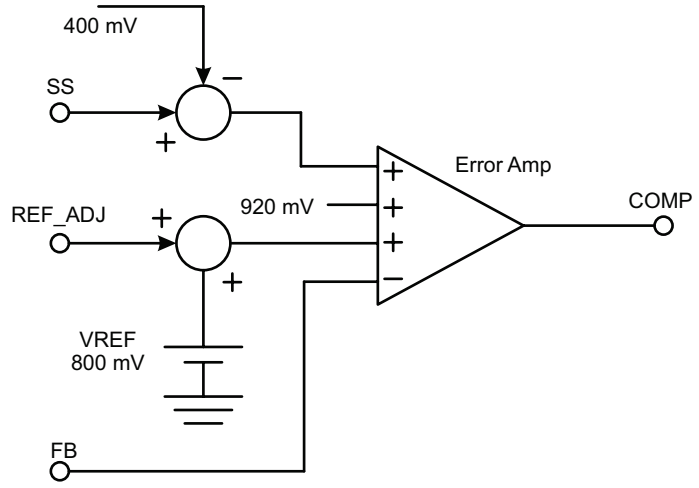


Figure 1: A8652/53 Error Amplifier

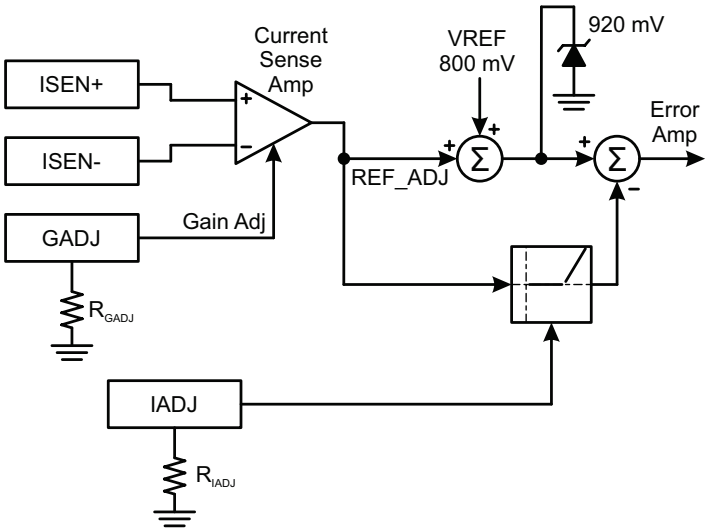


Figure 2: Remote Load Regulation Control

The amount of the voltage correction for the wiring harness is generated by the Remote Load Regulation control circuit and fed to the error amplifier via the REF_ADJ signal, as shown in Figures 1 and 2. The Remote Load Regulation controller generates REF_ADJ according to the load current sensed by ISEN+ and ISEN– and the gain set by the configuration resistors. The current sense resistor (R_{sen}) is connected on the load side between the regulator output capacitor and the load terminal and can have a value between 20 and 50 mΩ.

The gain of the current sense to the REF_ADJ (G_{ADJ}) signal is set by the ratio of resistance to GND on the GADJ pin and the IADJ pin in conjunction with R_{sen}:

$$G_{ADJ} = \frac{REF\_ADJ}{I_{OUT}} = \frac{R_{sen} \times R_{IADJ}}{R_{GADJ}} \quad (1)$$

This allows the user to calibrate the voltage correction to the IR drop of the wiring harness, as shown in Figure 3. This calibration results in improved load regulation at the end of the wiring harness.

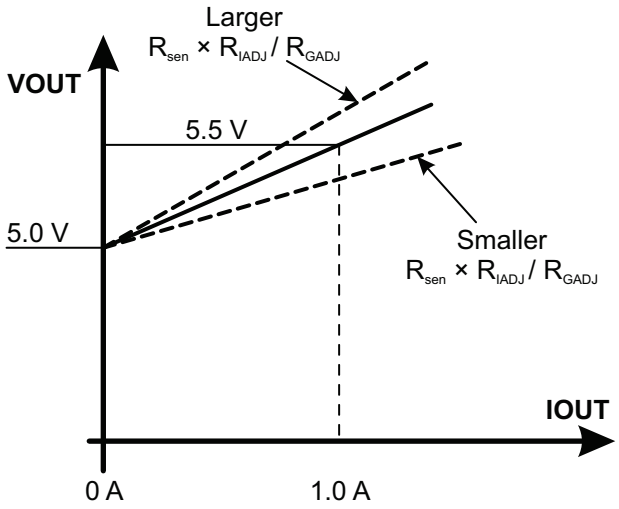


Figure 3: Voltage Correction Gain Adjustment

To configure the voltage correction gain, the load-side current limit (I_{OUT_LIM}) must first be set by the following equation (also referring to Table 1):

$$R_{IADJ} = \frac{1200}{I_{OUT\_LIM} \times R_{sen}} \quad (2)$$

The voltage correction gain is based on R_{WIRE}, which is the sum of the wiring harness supply and return resistive paths as detailed in the typical application diagram. Given the gain of the FB pin voltage divider ($A_{FB} = V_{OUT}/V_{FB}$), R_{WIRE} and R_{IADJ} the desired voltage correction gain is set by the following equation (referring to Figure 4):

$$R_{GADJ} = \frac{R_{sen}}{R_{WIRE}} \times A_{FB} \times R_{IADJ} \quad (3)$$

For example, for a 5 V application with a 20 mΩ current sense resistor and a 3 A load side current limit the IADJ configuration resistor would be 20 kΩ. To correct for a 125 mV wire harness drop at 1 A (R_{WIRE} =125 mΩ) given R_{IADJ} = 20 kΩ, the GADJ configuration resistor should be 20 kΩ.

Table 1: R_{IADJ} Resistor Selection vs. I_{OUT_LIM}

R_{IADJ} (kΩ)	R_{sen} = 20 mΩ	R_{sen} = 50 mΩ
15.8	3.80	1.52
16.9	3.55	1.42
17.4	3.45	1.38
17.8	3.37	1.35
18.2	3.30	1.32
18.7	3.21	1.28
19.1	3.14	1.26
19.6	3.06	1.22
20.0	3.00	1.20
20.5	2.93	1.17
21.0	2.86	1.14
21.5	2.79	1.12
22.1	2.71	1.09
22.6	2.65	1.06
23.2	2.59	1.03
23.7	2.53	1.01
24.3	2.47	0.99
26.7	2.25	0.90
30.1	1.99	0.80
34.8	1.72	0.69
40.2	1.49	0.60

As will be discussed in further detail below, altering the GADJ resistance with an external voltage proportionally adjusts the voltage correction gain (Method 1, refer to Typical Application Diagram 2). On the other hand, altering the IADJ resistance with an external voltage proportionally adjusts the load-side current limit, and inversely proportionally adjusts the voltage correction gain (Method 2).

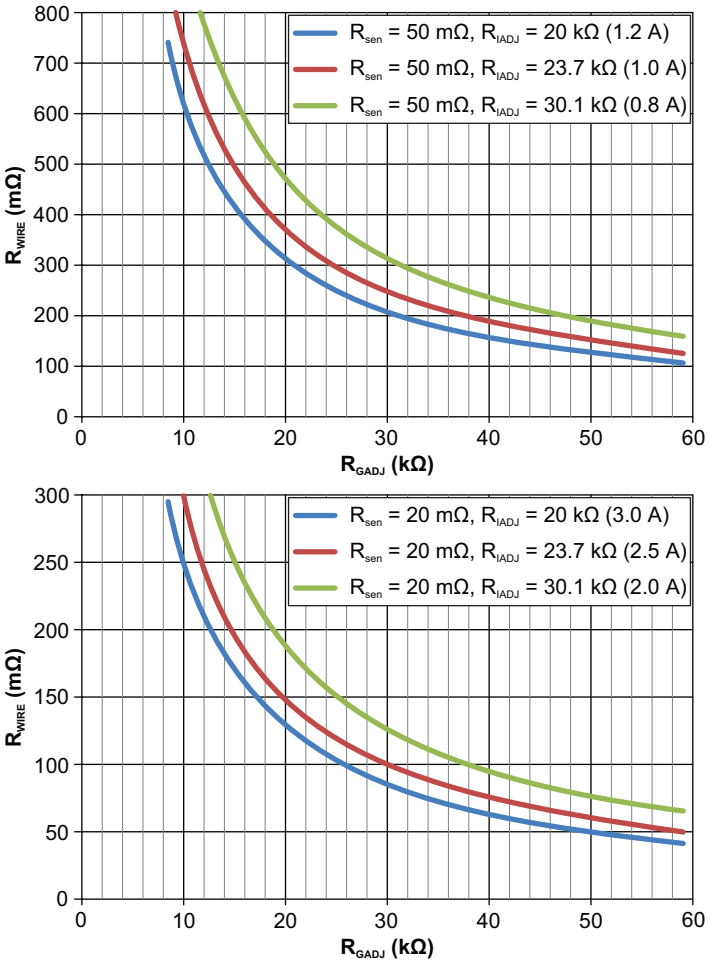


Figure 4: R_{GADJ} Selection vs R_{WIRE} for Given R_{sen}, R_{IADJ}

This can be very useful, for instance when one "universal" design is created for multiple platforms, where the expected wiring resistance can vary widely. The design can use this method in conjunction with the system controller such that the degree of voltage correction can be set via software.

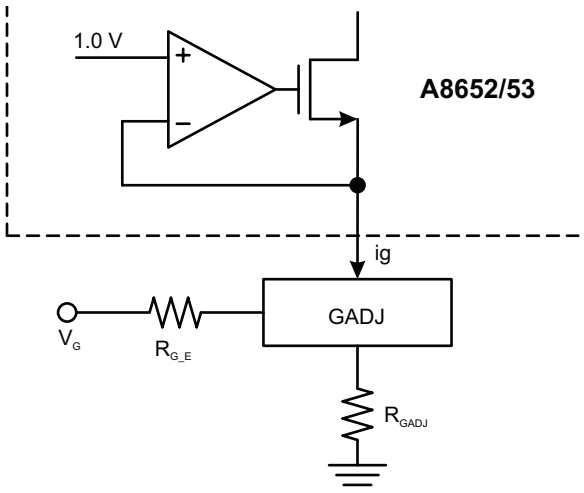


Figure 5: Dynamic Voltage Correction Adjustment at Pin GADJ

Figure 5 above illustrates how to adjust the amount of voltage correction by controlling V_G. The equivalent resistance R_{G_eqv} at pin GADJ with respect to GND now becomes:

$$R_{G\_eqv} = \frac{1}{\left(\frac{1}{R_{GADJ}} - \frac{V_G - 1}{R_{G\_E}}\right)} \quad (4)$$

The voltage correction gain (G_{ADJ}) then varies linearly with the applied V_G for given R_{GADJ} and R_{G_E}. Normalizing this gain to the case with only R_{GADJ} connecting to pin GADJ results in:

$$G_{norm} = 1 + \frac{R_{GADJ}}{R_{G\_E}} - \frac{R_{GADJ}}{R_{G\_E}} V_G \quad (5)$$

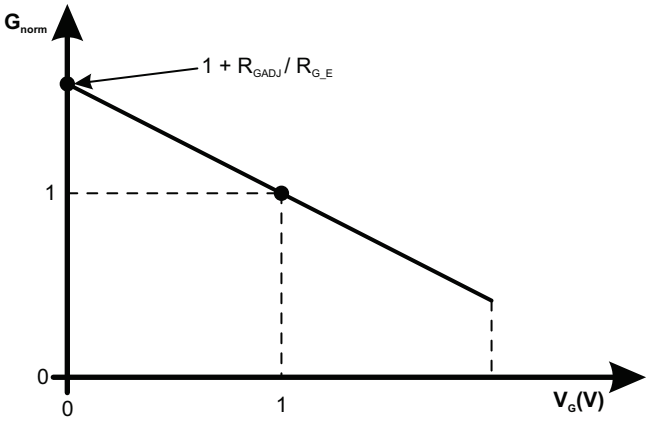


Figure 6: Normalized Gain G_{norm} vs. V_G

The minimum and maximum voltage correction can be adjusted with the ratio of R_{GADJ} and R_{G_E} for a given controlling voltage (V_G) range.

Similarly, as shown in Figure 7, Method 2 can inversely proportionally adjust the voltage correction gain for a fixed GADJ resistance, at the same time proportionally adjusts the load side current limit (I_{OUT_LIM}) by applying the control voltage (V_I) to the IADJ pin. The equivalent resistance RIADJ at pin IADJ is:

$$R_{I\_eqv} = \frac{1}{\left(\frac{1}{R_{IADJ}} - \frac{V_I - 1}{R_{I\_E}}\right)} \quad (6)$$

Thus the voltage correction gain can be kept the same by applying a separate control voltage to the GADJ pin to keep the GADJ and IADJ resistor ratio the same if only load-side current limit needs to be adjusted.

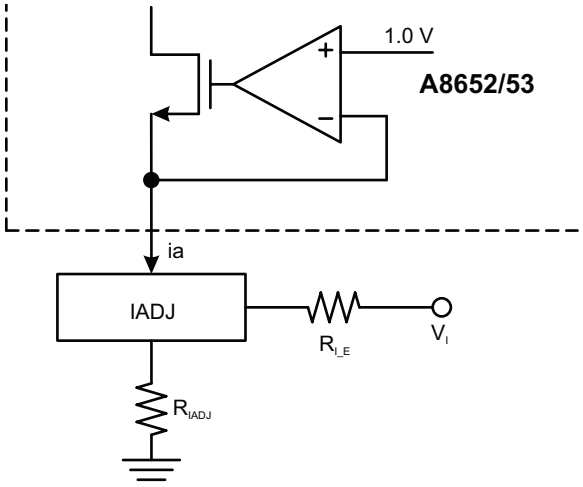


Figure 7: Simultaneous Voltage Correction and Load-Side Current Limit Adjustment at Pin IADJ

If a fixed load-side current limit is desired it is simpler to use GADJ pin to dynamically control the amount of voltage correction because of linear control and only altering the voltage correction gain.

The GADJ and IADJ pins are designed for a resistance range of 10 to 34 kΩ, and therefore the controlling voltage V_G and V_I must be limited as follows:

$$10\ k\Omega < R_{G\_eqv} < 34\ k\Omega \quad (7)$$

and

$$10\ k\Omega < R_{I\_eqv} < 34\ k\Omega \quad (8)$$

In addition to the voltage correction circuitry, Figure 2 also details the load-side current limit (I_{OUT_LIM}), which is configured independently by the resistance to GND on the IADJ pin. As shown by Figure 8 and 9, when the load current exceeds I_{OUT_LIM}, POK is pulled low to flag the condition, and the output voltage is decreased at the same rate as the voltage correction (set by Rsen, R_{GADJ} and R_{IADJ}) to protect against unstable behavior. Figure 8 and 9 also details the operation of peak inductor current limit (I_{PK_LIM}), which monitors the inductor current and will enter into hiccup mode after 240 counts of exceeding I_{PK_LIM} for robust protection and against the output voltage shorted to GND.

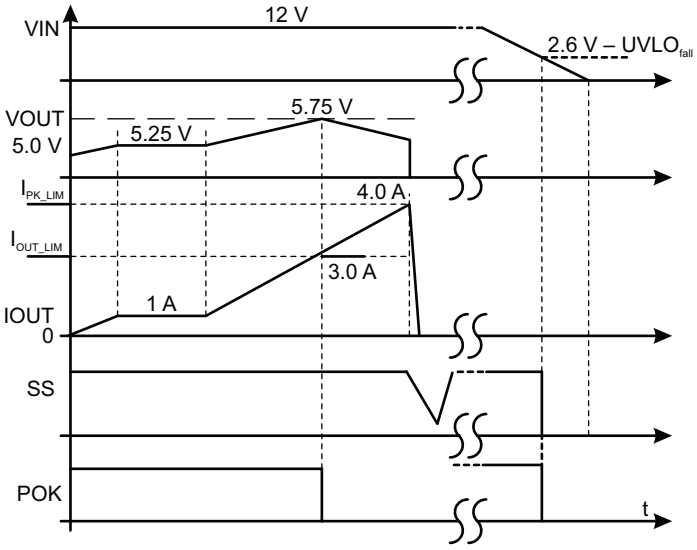


Figure 8: POK and Load-Side Current Limit Timing

In addition to current protection, the A8652/53 also includes a 115% (5.75 V) regulation voltage limit on the error amplifier. This protection feature prevents the excessive output voltages during fault conditions, and is therefore set above the operating range of the Remote Load Regulation. However, if the voltage correction gain is too high, the 115% voltage limit will impede the Remote Load Regulation operation, as shown in Figure 9. The VOUT waveform shows the operation point of the Remote Load Regulation controller set by REF_ADJ, but as illustrated, the 115% voltage regulation limit at the error amplifier clips the output voltage to 5.75 V.

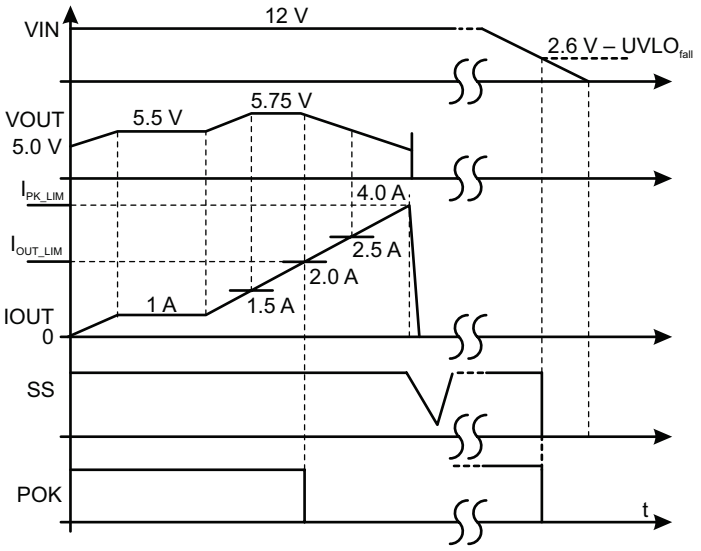


Figure 9: Excessive Voltage Correction Gain

The Remote Load Regulation controller is also robust against pin faults, such as adjacent pins shorting, shorting pins to GND, or pin open faults. When a pin fault is detected, either the IADJ or GADJ pin, the A8652/53 will default to the 800 mV reference, not applying any voltage correction to the output voltage. Given this, the GADJ pin can be connected to GND to disable the Remote Load Regulation function.

Compensation Components

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier output (COMP pin) to GND as shown in the applications schematic. In most instances, an additional low-value capacitor (C_P) should be connected in parallel with the R_Z-C_Z compensation network to reduce the loop gain at very high frequencies. However, if the C_P capacitor is too large, the phase margin of the converter may be reduced. How to calculate R_Z, C_Z and C_P is covered in the Component Selection section of this datasheet. When selecting the compensation components, the load decoupling capacitance and the wiring resistance must be taken into consideration.

If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via the approximately 1 kΩ internal resistor and PWM switching is inhibited.

Slope Compensation

The A8652/53 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the functional block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset. The amount of slope compensation is scaled with the switching frequency when programming the frequency with a resistor or with an external clock.

The value of the output inductor should be chosen such that slope compensation rate S_E is between 0.5× and 1× the falling slope of the inductor current (S_F).

Current Sense Amplifier

The A8652/53 incorporates a high-bandwidth current sense amplifier to monitor the current through the top MOSFET. This current signal is used to regulate the peak current when the top MOSFET is turned on. The current signal is also used by the protection circuitry for the pulse-by-pulse current limit (I_{PK_LIM}) and hiccup mode short-circuit protection.

Low Dropout Operation and Undervoltage Lockout

The Undervoltage Lockout behavior is described in the following Protection Features section.

The A8652/53 is designed to allow operation when input voltage drops as low as 2.6 V, which is the UVLO STOP threshold. When the input voltage falls towards the nominal output voltage, the high-side switch can remain on for maximum on-time to keep regulating the output. This is accomplished by decreasing the f_{SW} switching frequency. In this way, the dropout from the input to output voltage is minimized.

Sleep Mode with Enable input

The A8652/53 provides a shutdown function via the EN pin. When this pin is low, the A8652/53 is shut down and the A8652/53 will enter a “sleep mode” where the internal control circuits will be shut off and draw less current from VIN. If EN goes high, the A8652/53 will turn on and provided there are no fault conditions, soft-start will be initiated and V_{OUT} will ramp to its final voltage in a time set by the soft-start capacitor (C_{SS}). To automatically enable the A8652/53, the EN pin may be connected directly to VIN.

Power MOSFETs

The A8652/53 includes an 80 mΩ, high-side N-channel MOSFET capable of delivering up to 4 A typical. The A8652/53 also includes a 55 mΩ, low-side N-channel MOSFET to provide synchronous rectification.

When the A8652/53 is disabled via the EN input being low or a Fault condition, the A8652/53 output stage is tri-stated by turning off both the upper and lower MOSFETs.

Pulse-Width Modulation (PWM) Mode

The A8652/53 employs fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and simple compensation.

A high-speed comparator and control logic is included in A8652/53. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation signal, and a DC PWM Ramp offset voltage ($V_{PWM(OFFSET)}$).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop, the bottom MOSFET is turned off, the top MOSFET is turned on, and the inductor current increases. When the voltage at the non-inverting of PWM comparator rises above the error amplifier output COMP, the PWM flip-flop is reset and the top MOSFET is turned off, the bottom MOSFET is turned on and the inductor current decreases.

The PWM flip-flop is reset-dominant, so the error amplifier may override the CLK signal in certain situations.

BOOT Regulator

The A8652/53 includes a regulator to charge its boot capacitor. The voltage across the boot capacitor is typically 5 V. If the boot capacitor is missing, the A8652/53 will detect a boot overvoltage. Similarly, if the boot capacitor is shorted, the A8652/53 will detect a boot undervoltage. Also, the boot regulator has a current limit to protect itself during a short-circuit condition.

Soft-Start (Startup) and Inrush Current Control

The soft-start function controls the inrush current at startup. The soft-start pin, SS, is connected to GND via a capacitor. When the A8652/53 is enabled and all faults are cleared, the soft-start pin will source the charging current $I_{SS(SU)}$, and the voltage on the

soft-start capacitor, C_{SS}, will ramp upward from 0 V. When the voltage at the soft-start pin exceeds the Soft-Start COMP Release Threshold ($V_{SS(RELEASE)}$, typically 400 mV) the error amplifier will ramp up its output voltage above the PWM Ramp Offset. At that instant, the top and bottom MOSFETs will begin switching. There is a small delay ($t_{d(SS)}$) between the moments of EN pin transitioning high and the soft-start voltage reaching 400mV to initiate PWM switching.

Once the A8652/53 begins PWM switching, the error amplifier will regulate the voltage at the FB pin to the soft-start pin voltage minus approximately 400 mV. During the active portion of soft-start, the voltage at the SS pin will rise from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin will rise from 0 V to 800 mV, and the regulator output voltage will rise from 0 V to the setpoint determined by the feedback resistor divider.

During startup, the PWM switching frequency is reduced to 25% of f_{SW} while V_{FB} is below 200 mV. If V_{FB} is above 200 mV but below 400 mV, the switching frequency is 50% of f_{SW}. At the same time, the transconductance of the error amplifier, gm_{EA}, is reduced to 1/2 of nominal value when V_{FB} is below 400 mV. When V_{FB} is above 400 mV, the switching frequency will be f_{SW} and the error amplifier gain will be the nominal value. The reduced switching frequencies and error amplifier gain are necessary to help improve output regulation and stability when V_{OUT} is at very low voltage. When V_{OUT} is very low, the PWM control loop requires on-time near the minimum controllable on-time and extra low duty cycles that are not possible at the nominal switching frequency.

When the voltage at the soft-start pin reaches approximately 1.2 V, the error amplifier will “switch over” and begin regulating the voltage at the FB pin to the A8652/53 adjusted reference voltage. The voltage at the soft-start pin will continue to rise to the internal LDO regulator output voltage.

If the A8652/53 is disabled or a fault occurs, the internal fault latch is set and the capacitor at the SS pin is discharged to ground very quickly through a 2 kΩ pull-down resistor. The A8652/53 will clear the internal fault latch when the voltage at the SS pin decays to approximately 200 mV. However, if the A8652/53 enters hiccup mode, the capacitor at the SS pin is slowly discharged through a current sink, $I_{SS(HIC)}$. Therefore, the soft-start capacitor C_{SS} not only controls the startup time but also the time between soft-start attempts in hiccup mode.

Pre-Biased Startup

If the output of the buck regulator is pre-biased at certain output voltage level, the A8652/53 will modify the normal startup routine to prevent discharging the output capacitors. As described in the Soft-Start (Startup) and Inrush Current Control section, the error amplifier usually becomes active when the voltage at the soft-start pin exceeds 400 mV. If the output is pre-biased, the voltage at the FB pin will be non-zero. The A8652/53 will not start switching until the voltage at SS pin rises to approximately V_{FB} + 400 mV. From then on, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and V_{OUT} will ramp upward from the pre-bias level.

Power OK (POK) Output

The Power OK (POK) output is an open-drain output, so an external pull-up resistor must be connected. POK remains high when the voltage at the FB pin is within regulation and the load-side current limit I_{out_LIM} is not triggered. The POK output is pulled low under the conditions below:

1. $V_{FB(RISING)}$ < 92.5% of the reference voltage V_{REF}
2. $V_{FB(RISING)}$ is larger than the sum of the adjusted reference voltage (i.e. V_{REF} + V_{REF_ADJ} or 920 mV, whichever is lower) and 80 mV
3. Load current exceeds the load-side current limit I_{out_LIM}
4. EN is low for more than 32 PWM cycles
5. V_{IN} UVLO event occurs
6. Thermal shutdown event occurs

Once the load-side current limit is triggered, POK will go low even if the output voltage has not yet dropped due to the current limit. If the A8652/53 is running and EN is kept low for more than 32 PWM cycles, POK will fall low and remain low only as long as the internal circuitry is able to enhance the open-drain output device. Once V_{IN} fully collapses, POK will return to the high-impedance state. Hysteresis is included in POK comparators to prevent chattering due to the ripple effects on comparators’ input terminals.

PROTECTION FEATURES

The A8652/53 was designed to satisfy the most demanding automotive and nonautomotive applications. In this section, a description of each protection feature is described and Table 2 summarizes the protections and their operation.

Undervoltage Lockout Protection (UVLO)

An Undervoltage Lockout (UVLO) comparator in the A8652/53 monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the START threshold ($V_{UVLO(START)}$, V_{IN} rising) or the STOP threshold ($V_{UVLO(STOP)}$, V_{IN} falling). The UVLO comparator incorporates some hysteresis, $V_{UVLO(HYS)}$, to help reduce ON/OFF cycling of the regulator due to the resistive or inductive drops in the VIN path during heavy loading or during startup.

Pulse-by-Pulse Overcurrent Protection (OCP)

The A8652/53 monitors the current in the upper MOSFET, and if this current exceeds the pulse-by-pulse overcurrent threshold (I_{PK_LIM}), then the upper MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The A8652/53 includes leading-edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the upper MOSFET is turned on.

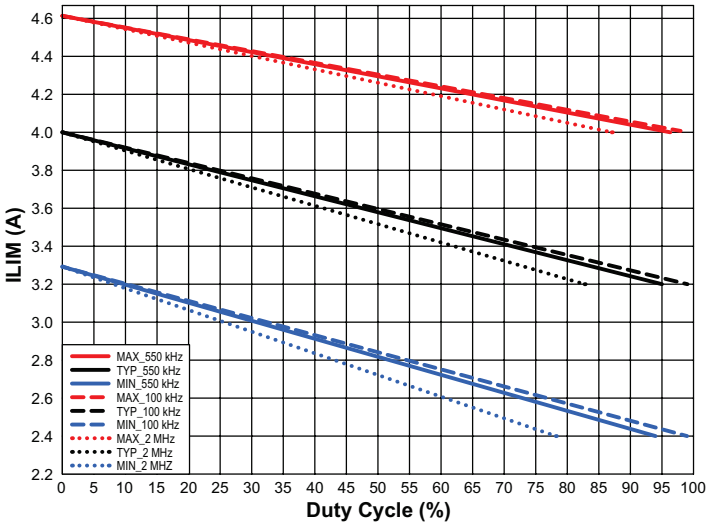


Figure 10: Pulse-by-Pulse Current Limit vs. Duty Cycle

at 100 kHz (long dashed lines), 550 kHz (solid lines) and 2 MHz (short dashed lines)

Because of the addition of the slope compensation ramp to the inductor current, the A8652/53 can deliver more current at lower duty cycles than at higher duty cycles to activate pulse-by-pulse overcurrent protection. Also the slope compensation is not a perfectly linear function of switching frequency, so the current limit at lower switching frequency is larger compared with the limit at higher switching frequency for a given duty cycle.

Figure 10 shows the typical and worst case pulse-by-pulse current limits versus duty cycles at 2 MHz, 550 kHz, and 100 kHz.

The exact current the buck regulators can support is heavily dependent on duty cycle (V_{IN}, V_{OUT}), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

Overcurrent Protection (OCP) and Hiccup Mode

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load current is too high. When the voltage at the SS pin is below the Hiccup OCP Threshold, the hiccup mode counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

1. $V_{SS} > V_{HIC(EN)}$ (2.3 V) and
2. V_{COMP} clamped at its maximum voltage (OCL = 1)

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP voltage decreases (OCL = 0) the OCP counter is cleared. If the OCP counter reaches OCP_{LIM} counts (240), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ).

The hiccup latch also enables a small current sink connected to the SS pin ($I_{SS(HIC)}$). This causes the voltage at the soft start pin to slowly ramp downward. When the voltage at the soft-start pin decays to a low-enough level ($V_{SS(RST)}$, 200 mV_{TYP}), the hiccup latch is cleared and the small current sink turned off. At that instant, the SS pin will begin to source current ($I_{SS(SU)}$) and the voltage at the SS pin will ramp upward. This marks the beginning of a new, normal soft-start cycle as described earlier. When the voltage at the soft-start pin exceeds the error amp voltage by approximately 400 mV, the error amp will force the voltage at the COMP pin to quickly slew upward and PWM switching will resume. If the short circuit at the regulator's output remains,

another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the converter is disabled. If the short circuit is removed, the A8652/53 will soft-start normally and the output voltage will automatically recover to the desired level.

Thus Hiccup mode is a very effective protection for the overload condition. It can avoid false trigger for a short-term overload. On the other hand, for the extended overload, the average power dissipation during Hiccup operation is very low to keep the controller cool and enhance the reliability.

Note that OCP is the only fault that results in Hiccup mode being ignored while $V_{SS} < 2.3$ V.

BOOT Capacitor Protection

The A8652/53 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator will enter Hiccup mode after 7 PWM cycles. If the BOOT capacitor is short-circuited, the regulator will enter Hiccup mode after 64 PWM cycles.

For a BOOT fault, Hiccup mode will operate virtually the same as described previously for an output short-circuit fault (OCP), with SS ramping up and down as a timer to initiate repeated soft-start attempts. BOOT faults are nonlatched condition, so the A8652/53 will automatically recover when the fault is corrected.

Dynamic Overvoltage Protection (OVP)

In addition to the error amp regulation voltage clamp ($V_{EA(CLAMP)}$) at 115%, the A8652/53 includes a dynamic overvoltage protection feature where the overvoltage threshold changes with the correction voltage. As shown in Figure 11 below, the A8652/53 also includes an overvoltage comparator that monitors the FB pin and the sum of the adjusted reference voltage (i.e. $V_{REF} + V_{REF\_ADJ}$ or 920 mV, whichever is lower) and 80 mV. In this way, the overvoltage threshold will dynamically change with the amount of the correction voltage and the threshold is always 0.5 V above the output voltage. For example, OVP threshold is 5.5 V when $V_{OUT} = 5$ V at $I_{OUT} = 0$ A; the OVP threshold will be 5.75 V when $V_{OUT} = 5.25$ V at $I_{OUT} = 1$ A; if $V_{OUT} = 5.75$ V at certain load, the OVP threshold will become 6.25 V. When the Remote Load Regulation function is disabled due to some reason (e.g., IADJ or GADJ pin fault or general non-

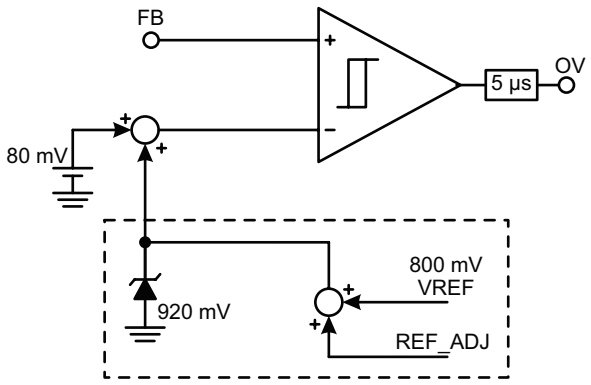


Figure 11: Dynamic Overvoltage Protection

USB buck application), the OVP threshold will be 5.5 V; when the output voltage reaches the 115% regulation limit, the OVP threshold will reach the maximum value of 6.25 V.

When the voltage at the FB pin exceeds the overvoltage threshold ($V_{POK(OV)}$), A8652/53 will stop PWM switching, i.e. both high and side switches will be turned off, and POK will be pulled low. In most cases, the error amplifier will be able to maintain regulation since the synchronous output stage has excellent sink and source capability. However the error amplifier and its regulation voltage clamp are not effective when the FB pin is disconnected or when the output is shorted to the input supply. When the FB pin is disconnected from the feedback resistor divider, a tiny internal current source will force the voltage at the FB pin to rise above $V_{POK(OV)}$ and disable the regulator, preventing the load from being significantly overvoltage. If a higher external voltage is accidently shorted to the A8652/53's output, V_{FB} will rise above the overvoltage threshold, triggering an OVP event and thus protecting the low-side switch. In either case, if the conditions causing the overvoltage are corrected, the regulator will automatically recover.

To provide additional protection when the battery is shorted to the load terminal, a 40 V Schottky diode (D) can be inserted after sensing resistor R_{sen} to block the high voltage entering into IC, and a Zener diode is placed at FB pin, as shown in Figure 12. The test result was shown in Figure 12b when Battery = 36 V was shorted to V_{OUT}.

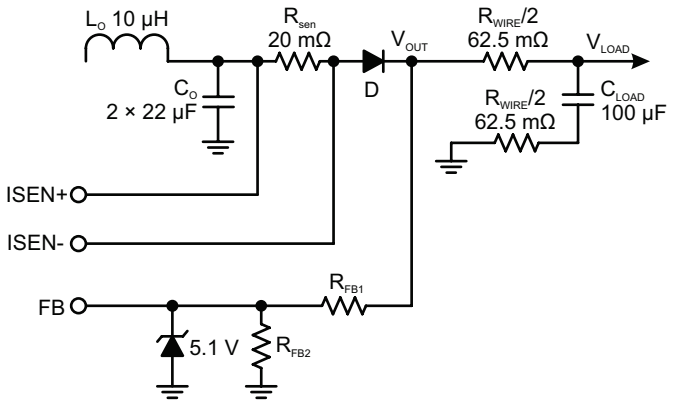


Figure 12a: Protection Circuitry for Load Short-to-Battery

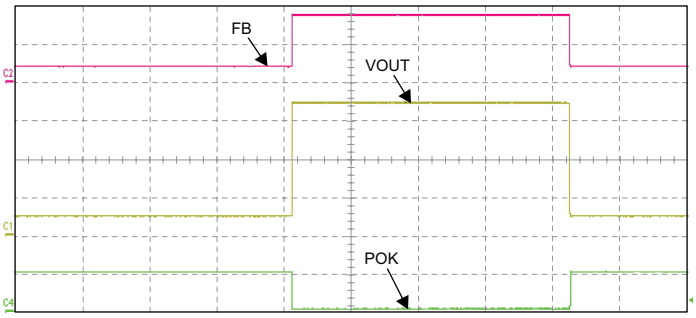


Figure 12b: Test Results when Battery = 36 V is Shorted to V_{OUT}

Ch1: V_{OUT} (10 V/div); Ch2: V_{FB} (2 V/div); Ch4: V_{POK} (5 V/div); 50 ms/div

Thermal Shutdown (TSD)

The A8652/53 monitors its junction temperature and will stop PWM switching and pull POK low if it becomes too hot. Also, to prepare for a restart, the SS and COMP pins will be pulled low until $V_{SS} < V_{SS(RST)}$. TSD is a non-latched fault so the A8652/53 will automatically recover if the junction temperature decreases by approximately 20°C.

Pin-to-Ground and Pin-to-Pin Short Protections

The A8652/53 was designed to satisfy the most demanding automotive and nonautomotive applications. For example, the A8652/53 was carefully designed "up front" to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the A8652/53's pinouts to optimize protection against pin-to-pin adjacent short-circuits. For example, logic pins and high-voltage pins were separated as much as possible. Inevitably, some low-voltage pins were located adjacent to high-voltage pins. In these instances, the low-voltage pins were designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the A8652/53.

Table 2: Summary of A8652/53 Fault Modes and Operation

Fault Mode	Fault Cases	V_{SS}	During Fault Count, before Hiccup			Dropout Foldback	POK	BOOT Charging	LATCH	RESET
			V_{COMP}	High-Side Switch	Low-Side Switch					
Positive Overcurrent Protection	1. Excessive I_{OUT} 2. V_{OUT} Shorted to GND 3. SW Soft Short To GND	Hiccup, after 240 faults of OCL	Clamped to achieve I_{LIM}, and pulled low only by hiccup	CCM according to COMP	CCM according to COMP	$f_{SW}/4$ or $f_{SW}/2$ based on V_{FB}	Depends on V_{OUT} and ISEN	Not affected	No	Auto, remove short
Load-Side Current Limit	Excessive I_{OUT}	Not affected	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Pulled Low immediately	Not affected	No	Auto
Negative Overcurrent Protection	1. Excessive Negative I_{OUT} 2. Inductor Short	Hiccup, after 1 fault of LSOC	Pulled low only by hiccup	Forced off Immediately	Forced off Immediately	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Not affected	No	Auto, remove short
SW Hard Short to GND	SW to GND hard Short	Hiccup at the end of blankOn	Pulled low only by hiccup	Forced off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Not affected	No (option avail able)	Auto, remove short
Thermal Shutdown	Die is too hot	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Forced off Immediately	Forced off Immediately	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto, Cool Down
Boot Capacitor Greater than 7 V	BOOT capacitor Open	Hiccup, after 7 latched faults	Pulled low by hiccup	CCM according to COMP	CCM according to COMP	Dropout Foldback Disabled by Hiccup	Depends on V_{OUT} and ISEN	Off for rest of period	–	–
Boot Capacitor On Fault	BOOT Capacitor Open	Hiccup, after 7 latched faults	Pulled low by hiccup	CCM according to COMP	CCM according to COMP	Dropout Foldback Disabled by Hiccup	Depends on V_{OUT} and ISEN	Off only during hiccup	No	Auto, replace capacitor
Boot Capacitor Overcurrent	BOOT to GND Short	Not affected	Not affected	Not affected	Pulsed at minOff	Not affected	Depends on V_{OUT} and ISEN	Off until fault clears	–	–
Boot Capacitor Low Voltage	Normal Low V_{IN} Operation	Not affected	Not affected	Not affected	Active during minOff period	Not affected	Depends on V_{OUT} and ISEN	On	–	–
Boot Capacitor Undervoltage	BOOT Capacitor Short	Not affected	Not affected	Forced Off Immediately	Active during minOff period	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	On	–	–
Low-Side Switch Undervoltage	Low V_{IN}	Not affected	Not affected	Forced Off Immediately	Forced Off Immediately	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Not affected	–	–
V_{REG} Undervoltage	Low V_{IN}	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Forced Off Immediately	Forced Off Immediately	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto
V_{IN} Undervoltage	Low V_{IN}	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Pulled Low Immediately & latched until V_{SS} < $V_{SS(RST)}$	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Off	No	Auto

Continued on next page...

Table 2: Summary of A8652/53 Fault Modes and Operation (continued)

Fault Mode	Fault Cases	V_{SS}	During Fault Count, before Hiccup			Dropout Foldback	POK	BOOT Charging	LATCH	RESET
			V_{COMP}	High-Side Switch	Low-Side Switch					
Hiccup Delay (after fault count is reached)	Hiccup	Discharged with $I_{SS(HIC)}$ until $V_{SS} < V_{SS(RST)}$	Pulled Low until $V_{SS} < V_{SS(RST)}$	Forced Off at Start of Period	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Not affected, (off only for boot capacitor faults) (sleep opt available)	–	–
Hiccup Restart or Startup (after V_{SS} returns to $V_{SS(RST)}$)	Startup Hiccup	Charged with $I_{SS(SU)}$	Released from 0 V, then responds to V_{SS}↑	CCM after V_{COMP} > 400 mV	CCM after V_{COMP} > 400 mV (pulsed at minOff)	Dropout Foldback Reset	Depends on V_{OUT} and ISEN	Not affected	–	–
FB Overvoltage	1. V_{OUT} to VIN Short 2. FB pin Open	Not affected	Not affected	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto, V_{FB} to normal range
ISENP Overvoltage	1. V_{OUT} to VIN short 2. FB to GND short	Not affected	Not affected	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto, V_{FB} to normal range
FB Undervoltage	Startup	Not affected	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Pulled Low Immediately	Not affected	No	Auto, V_{FB} to normal range
Feedback Less Than 400 mV	Startup	Not affected	Not affected	$f_{SW}/2$	CCM according to COMP	Not affected	Pulled Low	Not affected	–	–
Feedback Less Than 200 mV	Startup V_{OUT} to GND Short	Not affected	Not affected	$f_{SW}/4$	CCM according to COMP	f_{SW} already at 1/4	Pulled Low	Not affected	–	–
FSET Resistor Fault	1.FSET to GND short 2.FSET pulled high 3.Low R 4.High R	Pulled Low Immediately & latched until $V_{SS} < V_{SS(RST)}$	Pulled Low Immediately & latched until $V_{SS} < V_{SS(RST)}$	Forced Off Immediately	One Shot Diode Emulation	Not affected	Depends on V_{OUT} and ISEN	Off	–	–
GADJ or IADJ Resistor Fault	ADJ to GND short ADJ pulled high Low R High R	Not affected	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Depends on V_{OUT} and ISEN	Not affected	–	–
SS shorted to VIN	SS to VIN short	Clamped to Zener voltage internally	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Depends on V_{OUT} and ISEN	Not affected	–	–
SS shorted to GND	SS to GND short	At GND	Loop response only	CCM according to COMP	CCM according to COMP	Not affected	Depends on V_{OUT} and ISEN	Not affected	–	–
COMP shorted to GND	COMP to GND short	Not affected	At GND	CCM according to COMP	CCM according to COMP	Not affected	Depends on V_{OUT} and ISEN	Not affected	–	–

DESIGN AND COMPONENT SELECTION

Setting the Output Voltage

The output voltage of the regulator is determined by connecting a resistor divider from the output node (V_{OUT}) to the FB pin as shown in Figure 13. There are tradeoffs when choosing the value of the feedback resistors. If the series combination ($R_{FB1} + R_{FB2}$) is too low, then the light load efficiency of the regulator will be reduced. To maximize the efficiency, it is best to choose higher values of resistors. On the other hand, if the parallel combination (R_{FB1}//R_{FB2}) is too high, then the regulator may be susceptible to noise coupling onto the FB pin. 1% resistors are recommended to maintain the output voltage accuracy.

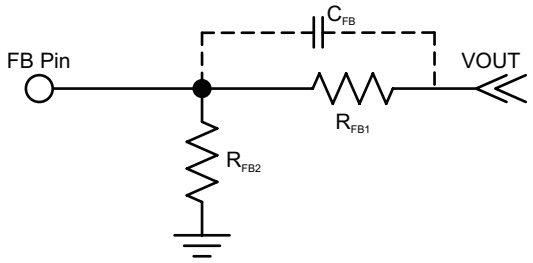


Figure 13: Connecting a Feedback Divider to Set the Output Voltage

The feedback resistors must satisfy the ratio shown in equation below to produce a desired output voltage, V_{OUT}.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8\ V} - 1 \qquad (9)$$

A phase lead capacitor (C_{FB}) can be connected in parallel with R_{FB1} to increase the phase and gain margins. It adds a zero and pole to the compensation network and boosts the loop phase at the crossover frequency. In general, C_{FB} should be less than 25 pF. If C_{FB} is too large, it will have no effect.

If C_{FB} is used, C_{FB} can be calculated from equation 10:

$$C_{FB} = \frac{1}{2\pi R_{FB1} f_c} \qquad (10)$$

where f_c is crossover frequency.

PWM Switching Frequency (f_{SW}, R_{FSET})

The PWM switching frequency is set by connecting a resistor from the FSET pin to ground. Figure 14 is a graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor, R_{FSET} (x-axis).

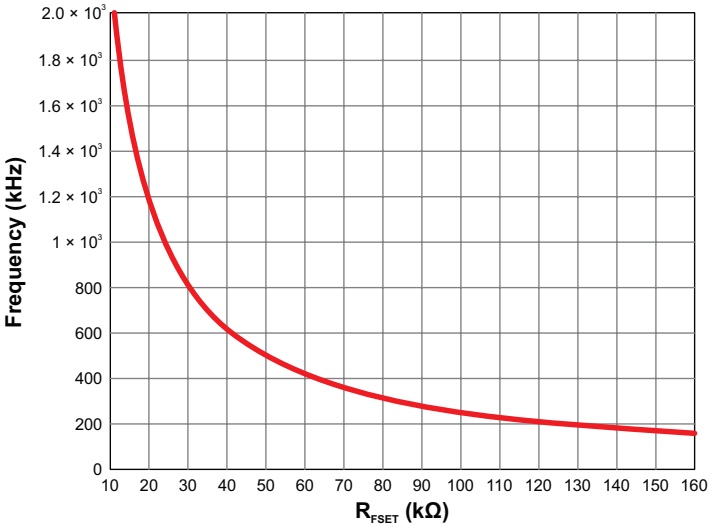


Figure 14: PWM Switching Frequency versus R_{FSET}

For a desired switching frequency (f_{SW}), the FSET resistor can be calculated using equation 11, where f_{SW} is in kHz and R_{FSET} is in kΩ.

$$R_{FSET} = \frac{26000}{f_{SW}} - 2.2 \qquad (11)$$

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A8652/53. If the system's required on-time is less than the minimum controllable on-time, pulse skipping will occur and the output voltage will have increased ripple or oscillations. The PWM switching frequency should be calculated using equation 12, where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the A8652/53 (See EC table), and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \qquad (12)$$

If the A8652/53 synchronization function is employed, the base switching frequency should be chosen such that pulse skipping will not occur at the maximum synchronized switching frequency according to equation 12 (i.e. 1.5 × f_{SW} is less than the result from equation 12).

Output Inductor (L_O)

For a peak current mode regulator, it is common knowledge that without adequate slope compensation, the system will become unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8652/53 is a fixed value (S_E). Therefore, it is important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the A8652/53 slope compensation. Equations 13 and 14 can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the down slope of the inductor current. In equation 13, use the slope compensation (S_E), which is a function of switching frequency according to equation 14.

$$\frac{V_{OUT}}{2 \times S_E} \leq L_O \leq \frac{V_{OUT}}{S_E} \qquad (13)$$

$$S_E = 0.0445 \times f_{SW}^2 + 0.5612 \times f_{SW} \qquad (14a \text{ for A8653})$$

$$S_E = 0.0237 \times f_{SW}^2 + 0.3529 \times f_{SW} \qquad (14b \text{ for A8652})$$

S_E is in A/µs, f_{SW} is in MHz, and L_O will be in µH.

If equations 13 or 14 yield an inductor value that is not a standard value, then the next highest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8652/53. Ideally, for output short-circuit conditions, the inductor should not saturate at the highest pulse-by-pulse current limit at minimum duty cycle. This may be too costly. At the very least, the inductor should not saturate at the peak operating current according to equation 15. In equation 15, $V_{IN(MAX)}$ is the maximum continuous input voltage.

$$I_{PEAK} = 4.62 - \frac{S_E \times V_{OUT}}{1.15 \times f_{SW} \times V_{IN(MAX)}} \qquad (15a \text{ for A8653})$$

$$I_{PEAK} = 2.1 - \frac{S_E \times V_{OUT}}{1.15 \times f_{SW} \times V_{IN(MAX)}} \qquad (15b \text{ for A8652})$$

Subtracting half of the inductor ripple current from equation 15 gives an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D),

$$I_{OUT(DC)} \leq 4.62 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O} \qquad (16a \text{ for A8653})$$

$$I_{OUT(DC)} \leq 2.1 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O} \qquad (16b \text{ for A8652})$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin. The output voltage ripple (ΔV_{OUT}) is a function of the output capacitors parameters: C_O, ESR_{CO}, ESL_{CO}.

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_L}{8 f_{SW} C_O} \qquad (17)$$

The type of output capacitors will determine which terms of equation 17 are dominant.

For ceramic output capacitors, the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 17.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 f_{SW} C_O} \qquad (18)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in equation 17 will be very small and the output voltage ripple will be determined primarily by the first two terms of equation 17.

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} \qquad (19)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent ESR_{CO} and ESL_{CO} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (i.e. increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and in most cases reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} ESL_{CO} \qquad (20)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint mainly depends on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system, it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Input Capacitors

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the

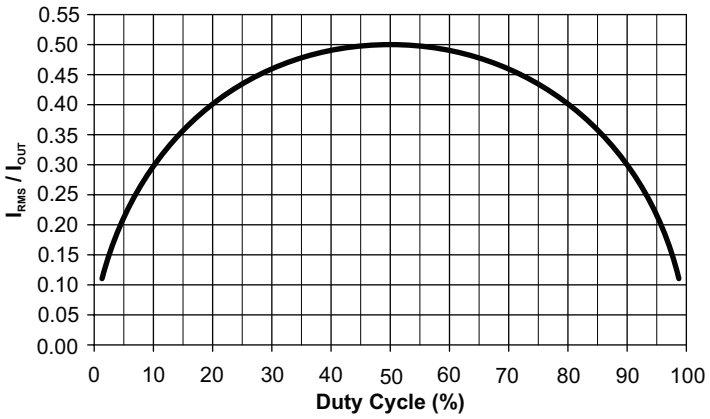


Figure 15: Input Capacitor Ripple vs. Duty Cycle

VIN pin UVLO circuitry ($V_{UVLO(HYS)}$, nominally 800 mV for the A8652/53) at maximum loading and minimum input voltage.

The input capacitors must deliver the RMS current according to:

$$I_{RMS} = I_O \sqrt{D \times (1 - D)} \qquad (21)$$

where the duty cycle D is $D \approx V_{OUT} / V_{IN}$. Figure 15 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 2.6 A of steady-state load current, the input capacitor(s) must support 0.40 × 2.6 A or 1.04 A_{RMS}.

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the A8652/53 UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \qquad (22)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency.

The D × (1 – D) term in equation 20 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on I_{OUT} = 2.6 A, f_{SW} = 85% of 425 kHz, D × (1 – D) = 0.25, and ΔV_{IN} = 150 mV,

$$C_{IN} \geq \frac{2.6\ A \times 0.25}{361\ kHz \times 150\ mV} = 12\ \mu F$$

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e. 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage (such as a load dump as high as 40 V for automotive applications).

Bootstrap Capacitor

A bootstrap capacitor must be connected between the BOOT and SW pins to provide the floating gate drive to the high-side MOSFET. Usually, 100 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

Soft-Start and Hiccup Mode Timing (C_{SS})

The soft-start time of the A8652/53 is determined by the value of the capacitance at the soft-start pin (C_{SS}).

When the A8652/53 is enabled, the voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ($I_{SS(SU)}$). However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above 400 mV. The soft-start delay ($t_{d(SS)}$) can be calculated using equation below,

$$t_{d(SS)} = C_{SS} \times \left(\frac{400\ mV}{I_{SS(SU)}}\right) \quad (23)$$

If the A8652/53 is starting with a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the sum of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors,

$$I_{CO} = C_O \times V_{OUT} / t_{SS}$$

is higher than the pulse-by-pulse current threshold, as shown in Figure 16. This phenomena is more pronounced when using high-value electrolytic type output capacitors.

To avoid prematurely triggering Hiccup mode, the soft-start capacitor (C_{SS}) should be calculated according to equation below,

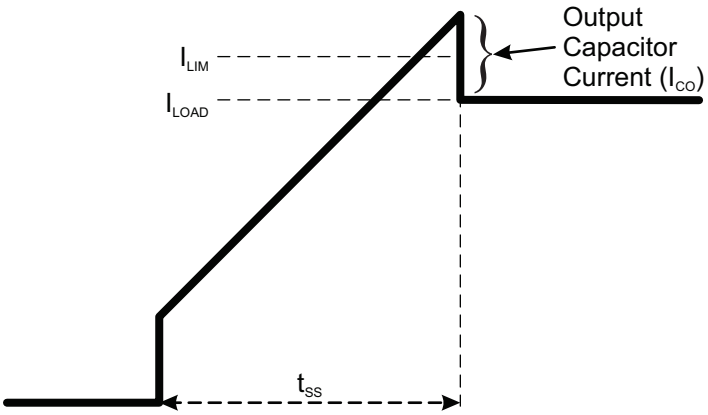


Figure 16: Output Current (I_{CO}) During Startup

$$C_{SS} \geq \frac{I_{SS(SU)} \times V_{OUT} \times C_O}{0.8\ V \times I_{CO}} \quad (24)$$

where V_{OUT} is the output voltage, C_O is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft-start (recommend 0.1 A < I_{CO} < 0.3 A). Higher values of I_{CO} result in faster soft-start times. However, lower values of I_{CO} ensure that Hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft-start time is too slow. If a nonstandard capacitor value for C_{SS} is calculated, the next larger value should be used.

The output voltage ramp time (t_{SS}) can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \text{ or } 0.8\ V \times \frac{C_{SS}}{I_{SS(SU)}} \quad (25)$$

When the A8652/53 is in hiccup mode, the soft-start capacitor is used as a timing capacitor and sets the hiccup period. The soft-start pin charges the soft-start capacitor with $I_{SS(SU)}$ during a startup attempt and discharges the same capacitor with $I_{SS(HIC)}$ between startup attempts. Because the ratio of $I_{SS(SU)}/I_{SS(HIC)}$ is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty cycle will be very low and the junction temperature will be kept low.

Remote Load Regulation Control Components

To compensate the voltage drop across the wiring harness, the wire resistance R_{WIRE} must be know as a priori. The current sense resistor R_{sen},which is connected in series with the load after the output capacitor C_O, is recommended to have a value between 20 and 50 mΩ, considering the tradeoff between measurement accuracy and power dissipation.

When the load side current limit I_{OUT_LIM} is set, the resistor R_{IADJ} at pin IADJ can be calculated from the equation below:

$$R_{IADJ} = \frac{1{,}200}{I_{OUT\_LIM} \times R_{sen}}$$

The needed amount of voltage correction should be equal to the voltage drop across the wiring harness:

$$I_{OUT} \times R_{WIRE} = I_{OUT} \times R_{sen} \times \frac{R_{IADJ}}{R_{GADJ}} \times A_{FB}$$

Thus for given R_{sen}, R_{IADJ}, R_{WIRE}, the resistance R_{GADJ} at pin GADJ can be determined from the equation above:

$$R_{GADJ} = \frac{R_{sen} \times R_{IADJ}}{R_{WIRE}} \times A_{FB}$$

Where $A_{FB} = V_{OUT} / V_{FB}$ is the gain of the FB pin voltage divider.

If the dynamic voltage correction adjustment at pin GADJ is desired (refer to Figure 5), then R_{GADJ} in the equation above should be replaced with the equivalent resistance R_{G_eqv} at pin GADJ:

$$R_{G\_eqv} = \frac{1}{\left(\frac{1}{R_{GADJ}} - \frac{V_G - 1}{R_{G\_E}}\right)}$$

Similarly the equivalent resistance R_{IADJ} at pin IADJ can be calculated below if an external voltage V_I is applied at pin IADJ as shown in Figure 7:

$$R_{I\_eqv} = \frac{1}{\left(\frac{1}{R_{IADJ}} - \frac{V_I - 1}{R_{I\_E}}\right)}$$

The GADJ and IADJ pins are designed for a resistance range of 10 to 34 kΩ, and therefore the controlling voltage V_G and V_I must be limited as follows:

$$10\ k\Omega < R_{G\_eqv} < 34\ k\Omega$$

and,

$$10\ k\Omega < R_{I\_eqv} < 34\ k\Omega$$

Compensation Components (R_Z, C_Z, C_P)

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeroes in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles and where these should be placed to maximize system stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8652/53, the output capacitors, and the load resistance. This circuitry is commonly referred as the "control to output" transfer function. The low frequency gain of this section depends on the COMP to SW current gain (gm_{POWER}), and the value of the load resistor (R_L). The DC gain ($G_{CO(0\ HZ)}$) of the control-to-output is

$$G_{CO(0\ Hz)} = gm_{POWER} \times R_L \quad (26)$$

The control to output transfer function has a pole (f_{P1}) formed by the output capacitance (C_{OUT}) and load resistance (R_L) at

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}} \quad (27)$$

The control to output transfer function also has a zero (f_{Z1}) formed by the output capacitance (C_{OUT}) and its associated ESR

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (28)$$

For a design with very low ESR type output capacitors (i.e. ceramic or OSCON output capacitors), the ESR zero, f_{Z1}, is usually at a very high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as is the case with electrolytic output capacitors), then it should be cancelled by the pole formed by the C_P capacitor and the R_Z resistor (discussed and identified later as f_{P3}).

Next, consider the feedback resistor divider, (R_{FB1} and R_{FB2}), the error amplifier (gm_{EA}), and its compensation network $R_Z/C_Z/C_P$. It greatly simplifies the transfer function derivation if $R_O >> R_Z$, and $C_Z >> C_P$ (where R_O is the error amplifier output impedance). In most cases, $R_O > 2$ MΩ, 1 kΩ < R_Z < 100 kΩ, 220 pF < C_Z < 47 nF, and C_P < 50 pF, so the following equations are very accurate.

The low frequency gain of the control section ($G_{C(0\ Hz)}$) is formed by the feedback resistor divider and the error amplifier. It can be calculated using equation 29:

$$G_{C(0\,Hz)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times gm_{EA} \times R_O = \frac{V_{FB}}{V_{OUT}} \times gm_{EA} \times R_O = \frac{V_{FB}}{V_{OUT}} \times A_{VOL} \quad (29)$$

where

V_{OUT} is the output voltage,

V_{FB} is the reference voltage (0.8 V),

gm_{EA} is the error amplifier transconductance (750 µA/V), and

R_O is the error amplifier output impedance (A_{VOL}/gm_{EA})

The transfer function of the Type-II compensated error amplifier has a (very) low frequency pole (f_{P2}) dominated by the output error amplifier's output impedance R_O and the C_Z compensation capacitor,

$$f_{P2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (30)$$

The transfer function of the Type-II error amplifier also has a low frequency zero (f_{Z2}) dominated by the R_Z resistor and the C_Z capacitor.

$$f_{Z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (31)$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole (f_{P3}) dominated by the R_Z resistor and the C_P capacitor

$$f_{P3} = \frac{1}{2\pi \times R_Z \times C_P} \quad (32)$$

Placing f_{Z2} just above f_{P1} will result in excellent phase margin, but relatively slow transient recovery time.

The magnitude and phase of the entire system are simply the sum of the error amplifier response and the control-to-output response.

A Generalized Tuning Procedure

1. Choose the system bandwidth, f_C, the frequency at which the magnitude of the gain will cross 0 dB. Recommended values for f_C based on the PWM switching frequency are $f_{SW}/20 < f_C < f_{SW}/7.5$. A higher value of f_C will generally provide a better transient response while a lower value of f_C will be easier to obtain higher gain and phase margins.
2. Calculate the R_Z resistor value to set the desired system bandwidth (f_C),

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2 \times \pi \times C_{OUT}}{gm_{POWER} \times gm_{EA}} \quad (33)$$

3. Determine the frequency of the pole (f_{P1}) formed by C_{OUT} and R_L by using equation 27 (repeated here).

$$f_{P1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the C_Z capacitor,

$$\frac{4}{2 \times \pi \times R_Z \times f_c} < C_Z < \frac{1}{2 \times \pi \times R_Z \times 1.5 \times f_{P1}} \quad (34)$$

   To maximize system stability (i.e. have the most gain margin), use a higher value of C_Z. To optimize transient recovery time at the expense of some phase margin, use a lower value of C_Z.

5. Calculate the frequency of the ESR zero (f_{Z1}) formed by the output capacitor(s) by using equation 28 (repeated here).

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

   A. If f_{Z1} is at least 1 decade higher than the target crossover frequency (f_C), then f_{Z1} can be ignored. This is usually the case for a design using ceramic output capacitors. Use equation 32 to calculate the value of C_P by setting f_{P3} to either $5 \times f_C$ or $f_{SW}/2$, whichever is higher.

   B. On the other hand, if f_{Z1} is near or below the target crossover frequency (f_C) then use equation 32 to calculate the value of C_P by setting f_{P3} equal to f_{Z1}. This is usually the case for a design using high ESR electrolytic output capacitors.

Referring to Typical Application Diagram 1 on page 1, several typical designs are provided in Table 3 with V_{LOAD} = 5 V.

Table 3: Recommended Components Values for Several Typical Designs

Design	f_{SW}	R_{FSET}	L_O	C_O	$R_Z + C_Z$ // C_P	R_{sen}	R_{GADJ}	R_{IADJ}
A8653 (set I_{OUT_LIM} = 2.75 A, R_{WIRE} = 125 mΩ)								
A	500 kHz	52.3 kΩ	10 µH (74437368100)	44 µF	14 kΩ + 2.7 nF//33 pF	20 mΩ	20.0 kΩ	20.0 kΩ
B	1 MHz	23.7 kΩ	6.8 µH (74437368068)	44 µF	14 kΩ + 2.7 nF//33 pF	20 mΩ	20.0 kΩ	20.0 kΩ
C	2 MHz	10.5 kΩ	6.8 µH (74437368068)	32 µF	37.4 kΩ + 1.8 nF//4.7 pF	20 mΩ	20.0 kΩ	20.0 kΩ
A8652 (set I_{OUT_LIM} = 1.2 A, R_{WIRE} = 200 mΩ)								
D	500 kHz	52.3 kΩ	33 µH (74437368330)	20 µF	14 kΩ + 2.7 nF//33pF	50 mΩ	31.6 kΩ	20.0 kΩ
E	2 MHz	10.5 kΩ	10 µH (74437368100)	20 µF	24.3 kΩ + 2.2 nF//4.7 pF	50 mΩ	31.6 kΩ	20.0 kΩ

POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A8652/53 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SW1}), the power dissipated due to the RMS current being conducted by the high-side MOSFET (P_{COND1}) and low-side MOSFET (P_{COND2}), and the power dissipated by both gate drivers (P_{DRIVER}).

The power dissipated from the V_{IN} supply current can be calculated using equation 35,

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times (Q_{G1} + Q_{G2}) \times f_{SW} \quad (35)$$

where

V_{IN} is the input voltage,

I_Q is the input quiesent current drawn by the A8652/53 (see EC table),

V_{GS} is the MOSFET gate drive voltage (typically 5 V),

Q_{G1} and Q_{G2} is the internal high-side and low-side MOSFET gate charges (approximately 5.8 nC and 10.4 nC, respectively), and

f_{SW} is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using equation 36,

$$P_{SW1} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (36)$$

where

V_{IN} is the input voltage,

I_{OUT} is the regulator output current,

f_{SW} is the PWM switching frequency, and

t_r and t_f are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 10 to 20 ns.

The power dissipated by the high-side MOSFET while it is conducting can be calculated using equation 37,

$$P_{COND1} = I^2_{RMS,FET} \times R_{DS(ON)HS} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(ON)HS} \quad (37)$$

Similarly, the conduction losses dissipated by the low-side MOSFET while it is conducting can be calculated by the following equation:

$$P_{COND2} = I^2_{RMS,FET} \times R_{DS(ON)LS} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I_L^2}{12}\right) \times R_{DS(ON)LS} \quad (38)$$

where

I_{OUT} is the regulator output current,

ΔI_L is the peak-to-peak inductor ripple current,

$R_{DS(ON)HS}$ is the on-resistance of the high-side MOSFET,

$R_{DS(ON)LS}$ is the on-resistance of the low-side MOSFET

The $R_{DS(ON)}$ of the both MOSFETs have some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accomodate an $R_{DS(ON)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated from the low-side MOSFET body diode during the non-overlap time can be calculated as follows:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW} \quad (39)$$

where

V_{SD} is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and

t_{NO} is the non-overlap time (15 ns(typ))

The sum of the power dissipated by the internal gate driver can be calculated using equation 40,

$$P_{DRIVER} = (Q_{G1} + Q_{G2}) \times V_{GS} \times f_{SW} \quad (40)$$

where

V_{GS} is the gate drive voltage (typically 5 V),

Q_{G1} and Q_{G2} is the gate charges to drive high-side and low-side MOSFETs to V_{GS} = 5 V (about 5.8 nC and 10.4 nC respectively), and

f_{SW} is the PWM switching frequency.

Finally, the total power dissipated by the A8652/53 (P_{TOTAL}) is the sum of the previous equations,

$$P_{TOTAL} = P_{IN} + P_{SW1} + P_{COND1} + P_{COND2} + P_{NO} + P_{DRIVER} \quad (41)$$

The average junction temperature can be calculated with the equation below,

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A \quad (42)$$

where

P_{TOTAL} is the total power dissipated from equation 40,

$R_{\theta JA}$ is the junction-to-ambient thermal resistance (34°C/W on a 4-layer PCB), and

T_A is the ambient temperature.

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to the ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical for the A8652/53 to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 17 shows a typical buck converter schematic with the critical power paths/loops. Figure 18 shows an example PCB component placement and routing with the same critical power paths/loops from the schematic.

1. The current sensing traces from ISEN+ and ISEN– are most sensitive to noise. A Kelvin connection is strongly recommended for the low ohmic current sensing resistor. The loop formed by ISEN+ and ISEN– traces should be minimal. The loop should be away from the noisy switching areas and can be placed on the bottom layer of PCB where it is away from the high di/dt and dv/dt areas. This critical loop is shown as trace 1 in Figure 17 and 18.
2. Place the ceramic input capacitors as close as possible to the VIN pin and GND pins to make the loop area minimal, and the traces of the input capacitors to VIN pin should be short and wide to minimize the inductance. This critical loop is shown as trace 2 in Figure 17 and 18. The larger input capacitor can be located further away from VIN pin. The input capacitors and A8652/53 IC should be on the same side of the board with traces on the same layer.
3. The loop from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground should be minimized with relatively wide traces.
4. When the high-side MOSFET is off, free-wheeling current flows from ground, through the synchronous low-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces, shown as trace 4 in Figure 17 and 18.
5. Place the output capacitors relatively close to the output inductor (L_O) and the A8652/53. Ideally, the output capacitors, output inductor and the controller IC A8652/53 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection to the GND.
6. Place the output inductor (L_O) as close as possible to the SW pin with short and wide traces. This critical trace is shown as trace 3 in Figure 17 and 18. The SW node voltage transitions from 0 V to V_{IN} and with a high dv/dt rate. This node is the root cause of many noise issues. It is suggested to minimize the SW copper area to minimize the coupling capacitance between SW node and other noise-sensitive nodes. However, the SW node area cannot be too small in order to conduct high current. A ground copper area can be placed beneath the SW node to provide additional shielding. Also, keep low level analog signals (like FB, COMP) away from the SW polygon.
7. Place the feedback resistor divider (R_{FB1} and R_{FB2}) very close to the FB pin. Make the ground side of R_{FB2} as close as possible to the A8652/53.
8. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. Also make the ground side of C_Z and C_P as close as possible to the A8652/53.
9. Place the FSET resistor as close as possible to the SYNC/FSET pin. Place the soft-start capacitor C_{SS} as close as possible to the SS pin.
10. The output voltage sense trace (from V_{OUT} to R_{FB1}) should be connected as close as possible to the load to obtain the best load regulation.
11. Place the bootstrap capacitor (C_{BOOT}) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible.
12. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
13. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.
14. The thermal pad under the A8652/53 IC should be connected to the GND plane (preferably on the top and bottom layer) with as many vias as possible. Allegro recommends vias with an approximately 0.25 to 0.30 mm hole and a 0.13 and 0.18 mm ring.
15. EMI/EMC issues are always a concern. Allegro recommends having locations for an RC snubber from SW to ground. The resistor should be 0805 or 1206 size.

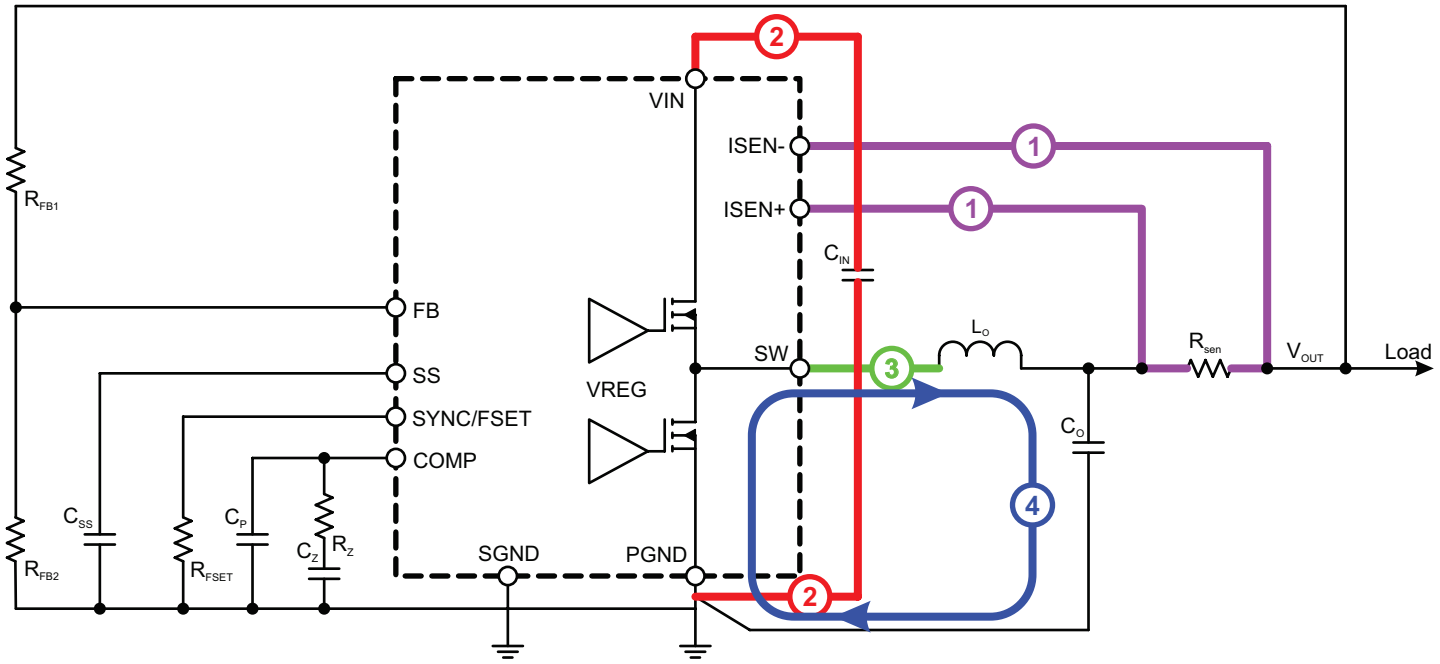


Figure 17: Typical Synchronous Buck Regulator with Current Sensing Resistor for Remote Load Regulation

A single-point ground is recommended, which could be the exposed thermal pad under the IC.

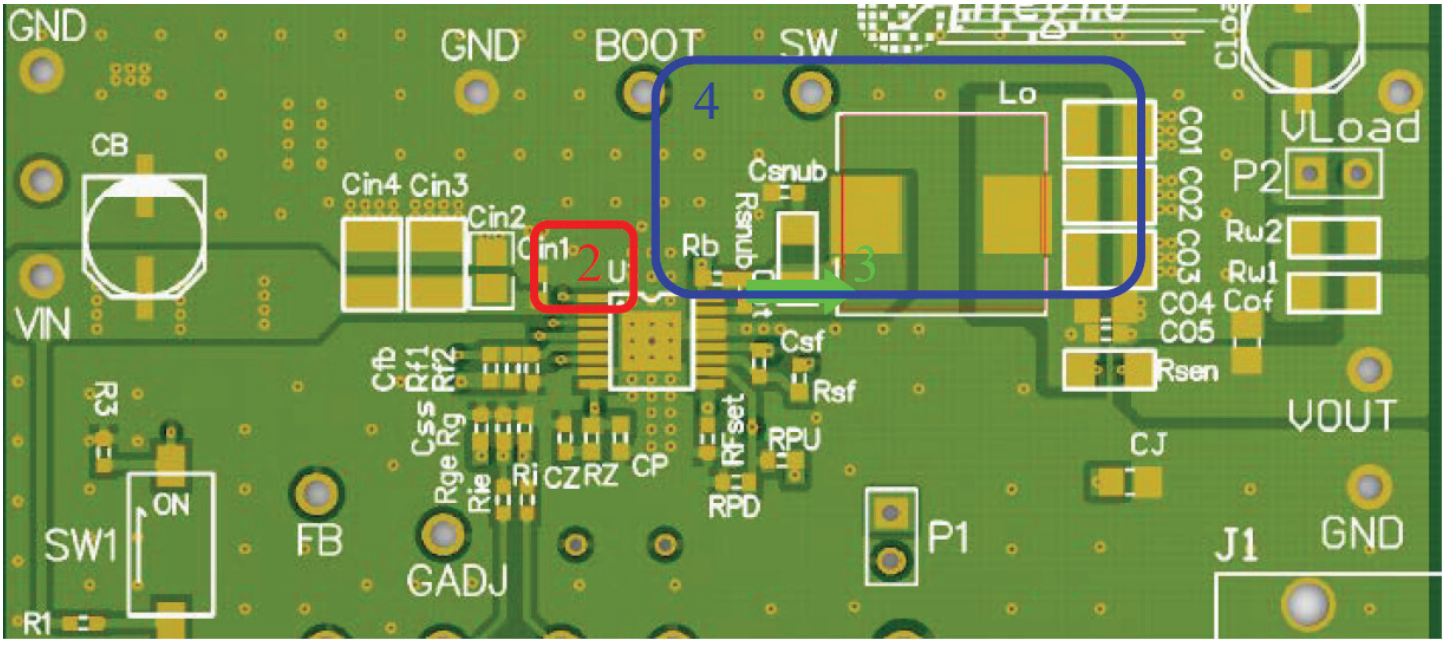


Figure 18a: Example PCB Component Placement and Routing, Top Layer

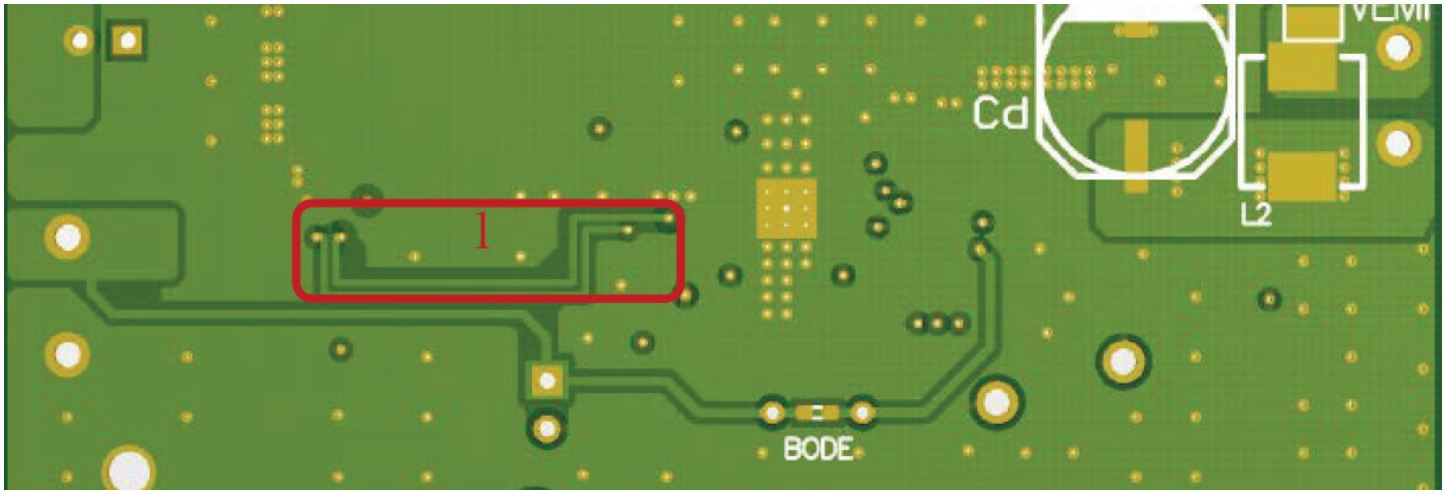
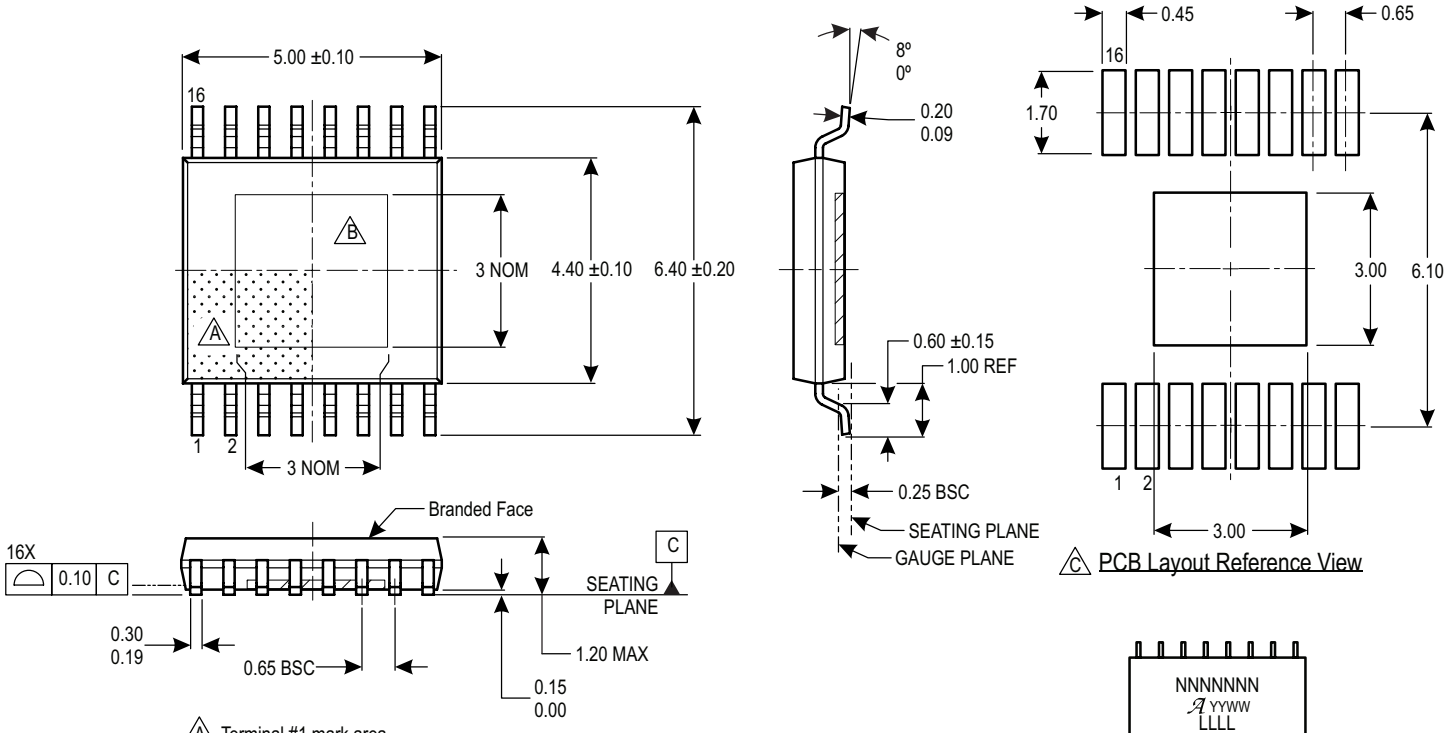


Figure 18b: Example PCB Component Placement and Routing, Bottom Layer

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 ABT)
Dimensions in millimeters. NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W= Week of manufacture
L = Characters 5-8 of lot number

Figure 19: Package LP, 16-Pin eTSSOP with Exposed Thermal Pad

Revision Table

Number	Date	Description
–	February 6, 2015	Initial Release
1	March 2, 2016	Corrected Output Voltage Accuracy symbol (page 6), Synchronization Input Rise and Fall Time units and Threshold symbols (page 7), SS Maximum Charge Voltage (page 8), and miscellaneous editorial changes.
2	April 7, 2016	Test specifications changed.

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