

# 2SC5121

## Silicon NPN triple diffusion planar type

For general amplification

### ■ Features

- High collector-base voltage (Emitter open)  $V_{CBO}$
- High collector-emitter voltage (Base open)  $V_{CEO}$
- Small collector output capacitance (Common base, input open circuited)  $C_{ob}$
- TO-126B package which requires no insulation plate for installation to the heat sink

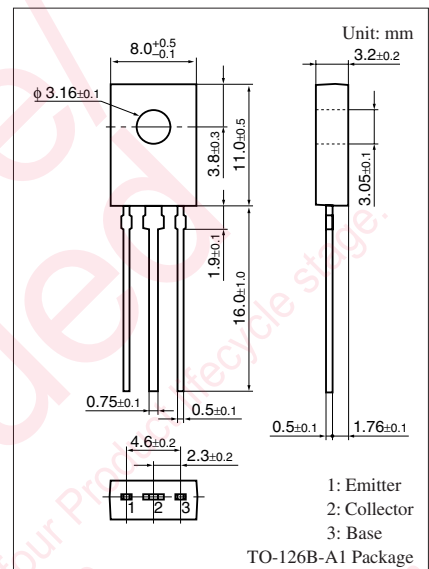
### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

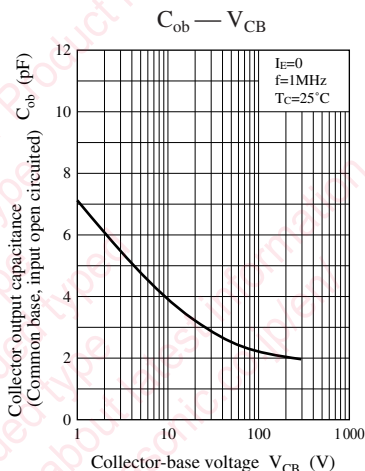
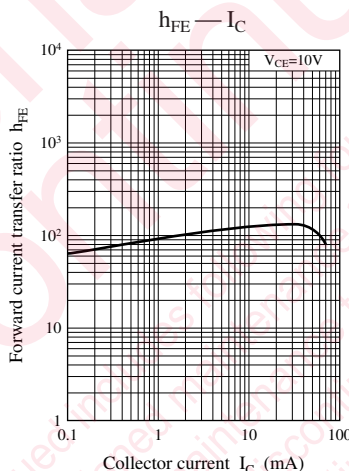
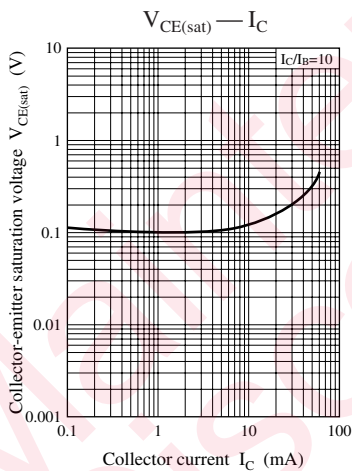
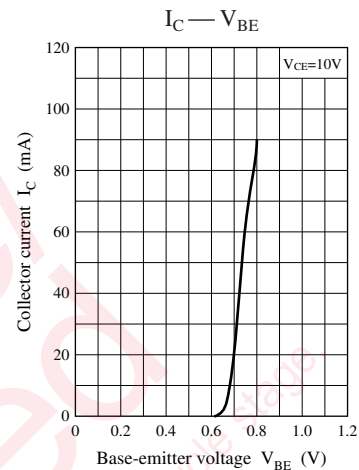
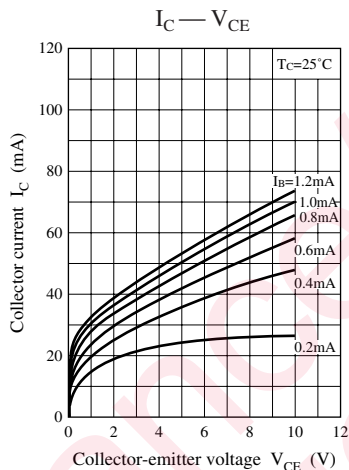
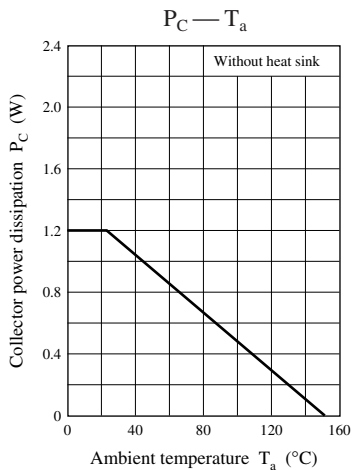
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	400	V
Collector-emitter voltage (Base open)	$V_{CEO}$	400	V
Emitter-base voltage (Collector open)	$V_{EBO}$	7	V
Collector current	$I_C$	70	mA
Peak collector current	$I_{CP}$	100	mA
Collector power dissipation	$P_C$	1.2	W
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = 100 \mu\text{A}$ , $I_B = 0$	400			V
Emitter-base voltage (Collector open)	$V_{EBO}$	$I_E = 1 \mu\text{A}$ , $I_C = 0$	7			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 300 \text{V}$ , $I_E = 0$			10	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = 380 \text{V}$ , $I_B = 0$ , $T_a = 80^\circ\text{C}$			10	$\mu\text{A}$
Forward current transfer ratio *	$h_{FE}$	$V_{CE} = 10 \text{V}$ , $I_C = 5 \text{mA}$	30		100	—
Collector-emitter saturation voltage *	$V_{CE(sat)}$	$I_C = 50 \text{mA}$ , $I_B = 5 \text{mA}$			1.2	V
Transition frequency	$f_T$	$V_{CB} = 10 \text{V}$ , $I_E = -10 \text{mA}$ , $f = 200 \text{MHz}$	50	80		MHz
Collector output capacitance (Common base, input open circuited)	$C_{ob}$	$V_{CB} = 10 \text{V}$ , $I_E = 0$ , $f = 1 \text{MHz}$		4	8	pF

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.





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