# SSL8516T
## Greenchip PFC and flyback controller

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## 1. General description

The GreenChip is the latest generation of green Switched Mode Power Supply (SMPS) controller ICs. The SSL8516T combines a controller for Power Factor Correction (PFC) and a flyback controller. Its high level of integration enables cost-effective LED lighting application power supply design using a very low number of external components.

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM), with valley switching.

The specially built-in green functions provide high efficiency at all power levels. At high power levels, the flyback operates in QR mode or DCM with valley detection. At medium power levels, the flyback controller switches to Frequency Reduction (FR) mode and limits the peak current to an adjustable minimum value. It ensures high efficiency while minimizing the audible noise from the transformer. In low-power mode, the PFC switches off to maintain high efficiency. Valley switching is used in all operating modes.

The SSL8516T is a Multi-Chip Module (MCM), containing two chips. The proprietary high-voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. The second low voltage Silicon-On-Insulator (SOI) is used for accurate, high-speed protection functions and control.

The SSL8516T enables easy design of highly efficient and reliable LED lighting application power supplies between 25 W and 300 W.

LED drivers in particular benefit from the high level of integration. The IC meets the lighting class C requirements on mains current harmonics as specified by IEC 61000-3-2 over a wide input voltage range and a wide output power range.

**Remark:** All values in this document are typical values unless otherwise stated.

## 2. Features and benefits

### 2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation between 90 V (AC) to 305 V (AC)
- Fixed boost PFC with accurate maximum output voltage (NXP Semiconductors patented)
- High level of integration, results in cost-effective designs with very low external component counts
- Adjustable PFC switch off delay
- External PFC switch on and switch off override
- Accurate PFC switch on and switch off control (NXP Semiconductors patent pending)

### 2.2 Green features

- On-chip start-up current source
- Power-down functionality for very low standby power

### 2.3 PFC green features

- Valley/Zero-Voltage Switching (ZVS) for minimum switching losses (NXP Semiconductors patented)
- Frequency limitation reduces switching losses
- PFC switched off when a low-load is detected at the flyback output

### 2.4 Flyback green features

- Valley switching for minimum switching losses (NXP Semiconductors patented)
- Frequency reduction with adjustable minimum peak current at low-power operation maintains high-efficiency at low output power levels

### 2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection using demagnetization detection for both converters (NXP Semiconductors patented)
- UnderVoltage Protection (UVP) (foldback during overload)
- Accurate OverVoltage Protection (OVP) for both converters (adjustable for flyback converter)
- Mains voltage independent OverPower Protection (OPP)
- Open control loop protection for both converters. The open-loop protection on the flyback converter is safe restart
- OverTemperature Protection (OTP)
- Low and adjustable OverCurrent Protection (OCP) trip level for both converters
- General-purpose input for latched protection, for use with system OverTemperature Protection (OTP)

## 3. Applications

■ This IC can be used in all lighting applications requiring efficient and cost-effective AC-DC offline switch mode power solutions from 25 W to 300 W.

## 4. Ordering information

**Table 1.**    **Ordering information**

| Type number | Package | | |
| --- | --- | --- | --- |
| | **Name** | **Description** | **Version** |
| SSL8516T | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 5. Block diagram
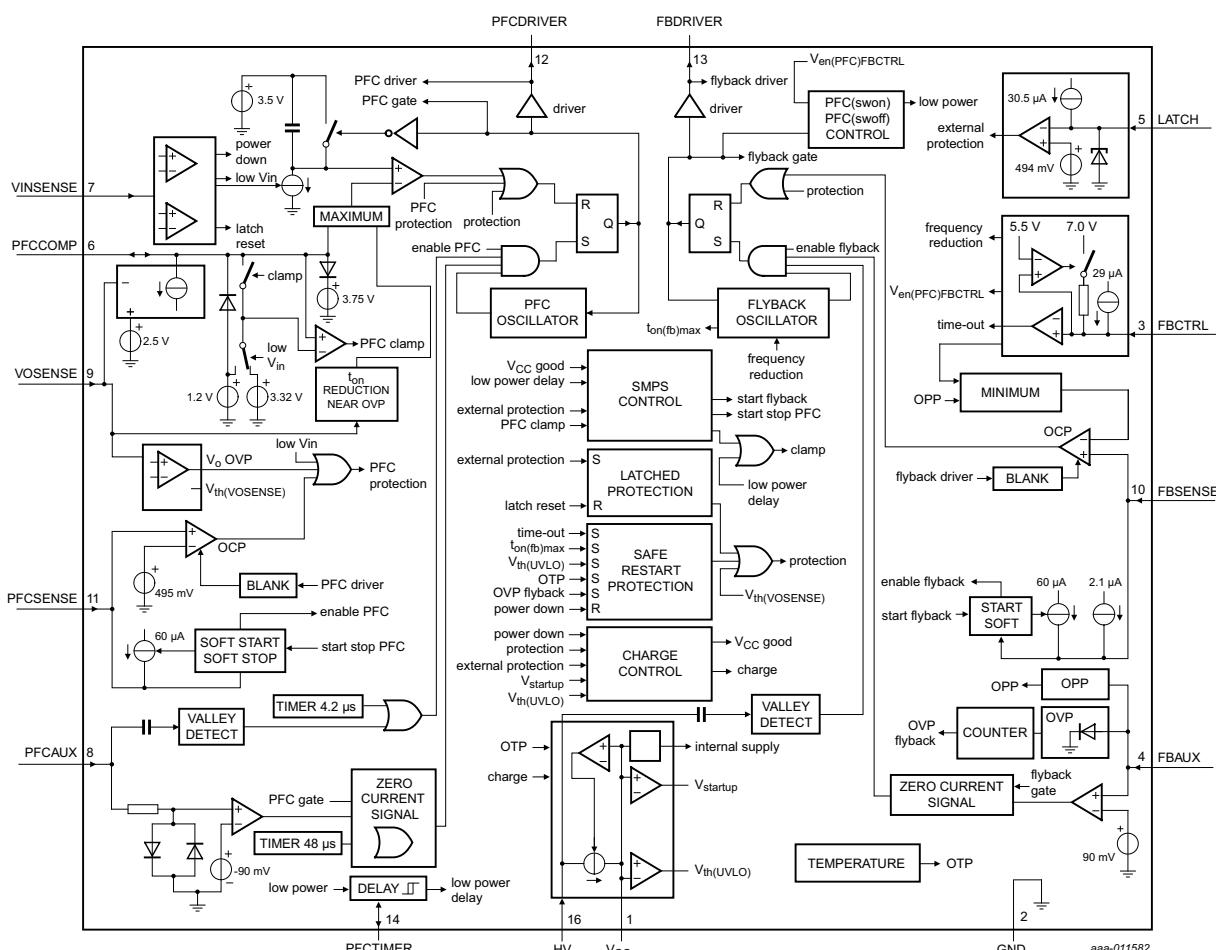


**Fig 1. SSL8516T block diagram**

# 6. Pinning information

## 6.1 Pinning

```
                    ┌──────────┐
        VCC   1 ─┤          ├─ 16   HV
        GND   2 ─┤          ├─ 15   HVS
      FBCTRL  3 ─┤          ├─ 14   PFCTIMER
       FBAUX  4 ─┤          ├─ 13   FBDRIVER
       LATCH  5 ─┤    IC    ├─ 12   PFCDRIVER
     PFCCOMP  6 ─┤          ├─ 11   PFCSENSE
     VINSENSE 7 ─┤          ├─ 10   FBSENSE
      PFCAUX  8 ─┤          ├─  9   VOSENSE
                    └──────────┘
                    aaa-002623
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**Fig 2.** **SSL8516T pin configuration (SOT109-1)**
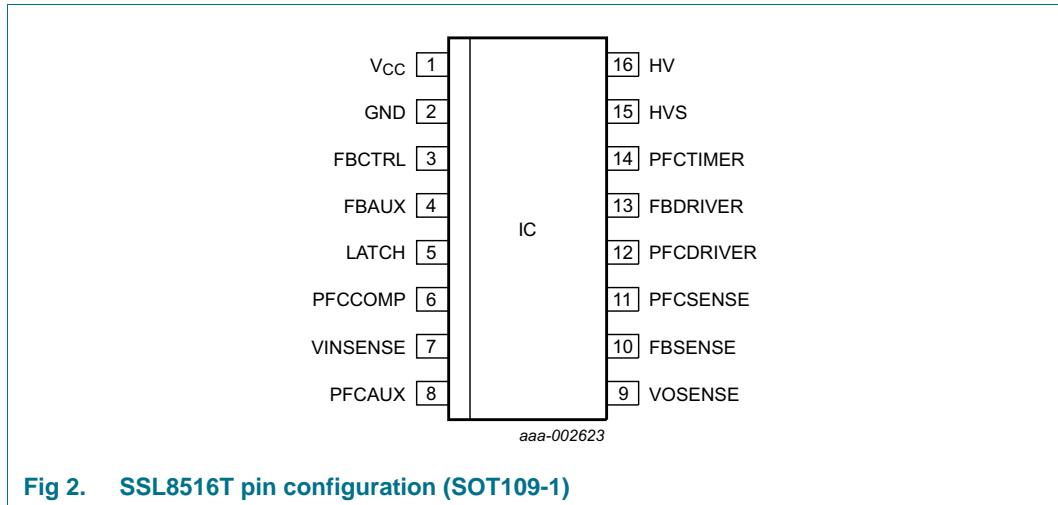
## 6.2 Pin description

**Table 2.** **Pin description**

| Symbol | Pin | Description |
|--------|-----|-------------|
| V$_{CC}$ | 1 | supply voltage |
| GND | 2 | ground |
| FBCTRL | 3 | flyback control input |
| FBAUX | 4 | auxiliary winding input for demagnetization timing and flyback OVP |
| LATCH | 5 | general-purpose protection input |
| PFCCOMP | 6 | PFC frequency compensation |
| VINSENSE | 7 | mains voltage sense input |
| PFCAUX | 8 | auxiliary winding input for demagnetization timing of the PFC |
| VOSENSE | 9 | sense input for PFC output voltage |
| FBSENSE | 10 | flyback current sense input |
| PFCSENSE | 11 | PFC current sense input |
| PFCDRIVER | 12 | PFC gate-driver output |
| FBDRIVER | 13 | flyback gate-driver output |
| PFCTIMER | 14 | PFC override and switch-off delay timer |
| HVS | 15 | high-voltage safety spacer; not connected |
| HV | 16 | high-voltage start-up and flyback valley sensing |

# 7. Functional description

## 7.1 General control

The SSL8516T contains a power factor correction circuit controller and a flyback circuit controller. A typical configuration is shown in Figure 3.



(1) The HV pin can either be connected to the center tap of the flyback transformer or to the drain of MOSFET S2.

**Fig 3.    A typical SSL8516T configuration**

### 7.1.1 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the $V_{CC}$ pin is charged from the high-voltage mains using the HV pin.

When $V_{CC}$ is less than $V_{trip}$, the charge current is $I_{ch(low)}$. This low current protects the IC if the $V_{CC}$ pin is shorted to ground. To ensure a short start-up time, the charge current above the $V_{trip}$ level is increased to $I_{ch(high)}$, until $V_{CC}$ reaches $V_{startup}$. Except during start-up, when $V_{CC}$ is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current becomes $I_{ch(low)}$ to ensure a low safe restart duty cycle during fault conditions.

When $V_{CC}$ is lowered to 2 V, the IC is reset. During the next start-up, the charge current between $V_{th(UVLO)}$ and $V_{startup}$ is $I_{ch(high)}$.

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The control logic activates the internal circuitry and switches off the HV charge current when $V_{CC}$ passes the $V_{startup}$ level. First, the LATCH pin current source is activated and the soft-start capacitors on the PFCSENSE and FBSENSE pins are charged. Also the clamp circuit on the PFCCOMP pin is activated.

The PFC circuit is activated when the following conditions are met:

- the LATCH pin voltage exceeds the $V_{en(LATCH)}$ voltage
- the PFCCOMP pin charging current drops below the absolute value of the $I_{en(PFCCOMP)}$ current
- the soft-start capacitor on the PFCSENSE pin is charged

If the soft-start capacitor on the FBSENSE pin is charged, the flyback converter is activated. The flyback converter output voltage is then regulated to its nominal output voltage. The auxiliary winding of the flyback converter takes over the IC supply (see Figure 4).

If during start-up, the LATCH pin does not reach the $V_{en(LATCH)}$ level before $V_{CC}$ reaches $V_{th(UVLO)}$, the LATCH pin output is deactivated. The charge current is switched on again.

When the flyback converter is started, $V_{FBCTRL}$ is monitored. If the output voltage does not reach its intended regulation level within a specified time, $V_{FBCTRL}$ reaches the $V_{to(FBCTRL)}$ level. An error is then assumed and a safe restart is initiated.

When one of the safe restart or latched protection functions are triggered, both converters stop switching and the $V_{CC}$ voltage drops to $V_{th(UVLO)}$. A latched protection recharges capacitor $C_{VCC}$ using $I_{ch(low)}$ from the HV pin, but does not restart the converters. To provide safe restart protection, the capacitor is recharged using $I_{ch(low)}$ from the HV pin and the device restarts (see Figure 1).

If OVP is triggered on the PFC circuit ($V_{VOSENSE} > V_{OVP(VOSENSE)}$), the PFC controller stops switching until the $V_{VOSENSE} < V_{OVP(VOSENSE)}$. If a mains UVP is detected, $V_{VINSENSE} < V_{stop(VINSENSE)}$, the PFC controller stops switching until $V_{VINSENSE} > V_{start(VINSENSE)}$ again. OVP and UVP of the PFC circuit do not disable flyback controller switching.

When the $V_{CC}$ pin voltage drops under the UVLO level, both controllers stop switching and enter safe restart mode. In the safe restart mode, the $V_{CC}$ pin capacitor is recharged using $I_{ch(low)}$ from the HV pin.

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The protection signal resembles an imaginary protection trigger.

**Fig 4.    Start-up sequence, normal operation and restart sequence**
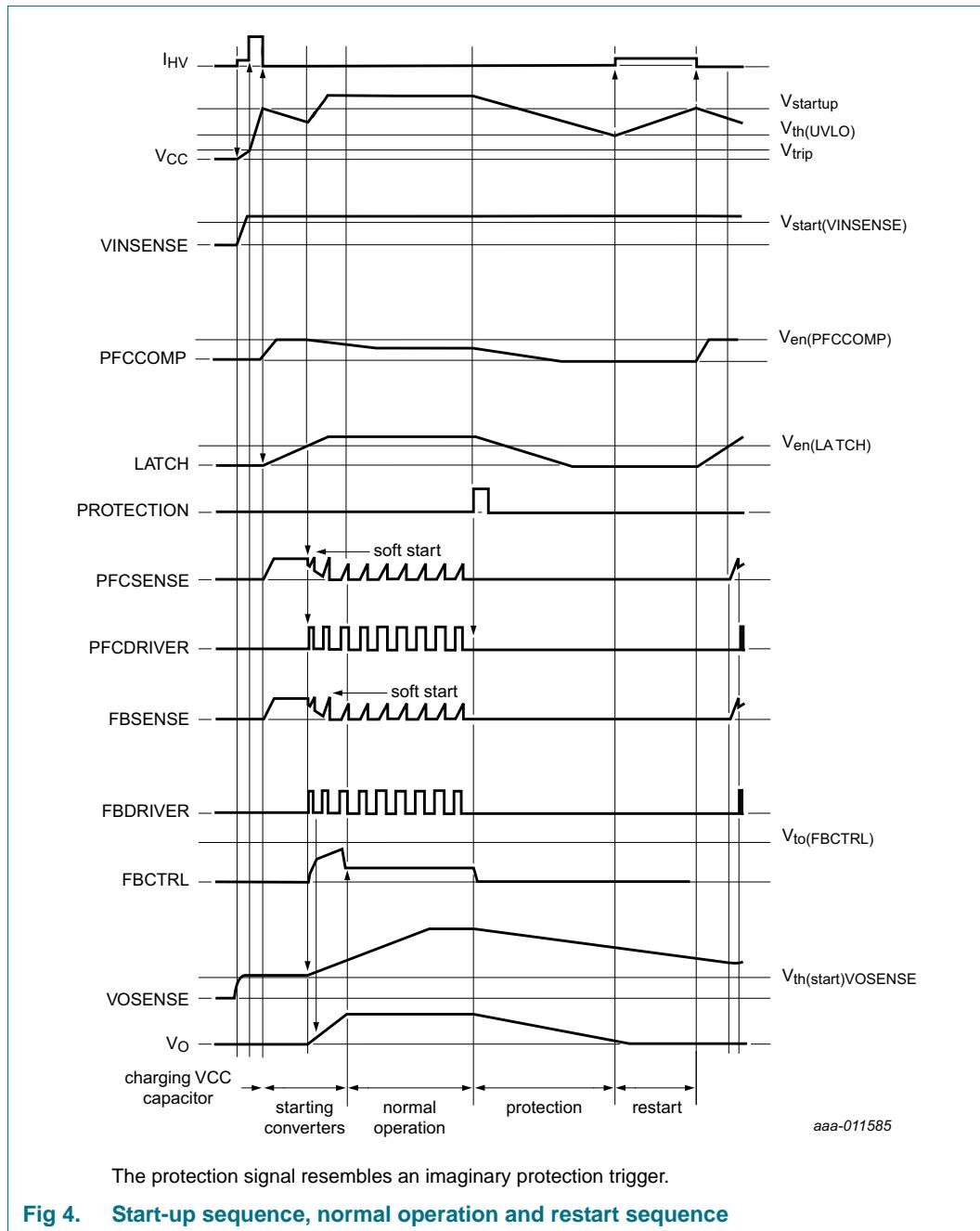
### 7.1.2 Power-down mode

The power-down mode can be activated for very low standby power applications by pulling the $V_{VINSENSE} < V_{th(pd)}$ level. The SSL8516T stops switching and safe restart protection is activated. The high-voltage start-up current source is also disabled during power-down and the SSL8516T does not restart until $V_{VINSENSE}$ is raised again.

During Power-down mode, all internal circuitry is disabled except for a voltage detection circuit on the VINSENSE pin. This circuit is supplied by the HV pin and draws 12 $\mu$A from the HV pin for biasing.

### 7.1.3 Supply management

All internal reference voltages are derived from a temperature compensated and trimmed on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

### 7.1.4 Latch input

The LATCH pin is a general-purpose input pin which is used to switch off both converters. The pin sources a current $I_{O(LATCH)}$ of 30.5 $\mu$A. Switching of both converters is stopped when $V_{LATCH}$ is < 494 mV. A latched protection is triggered. It can be reset by removing the voltage from both the $V_{CC}$ and HV pins or by the fast latch reset function (see Section 7.1.5).

At initial start-up, switching is prevented until the capacitor on the LATCH pin is charged above 582 mV. No internal filtering is performed on this pin. An internal 1.75 V clamp protects the pin from excessive voltages.

### 7.1.5 Fast latch reset

In a typical application, the mains can be interrupted briefly to reset the latched protection. The bulk capacitor $C_{bulk}$ does not have to discharge for this latched protection to reset.

When the VINSENSE voltage drops below 750 mV and is then raised to 860 mV, the latched protection is reset.

The latched protection is also reset by removing both the voltage on the $V_{CC}$ and HV pins.

### 7.1.6 Overtemperature protection

An accurate internal temperature protection is provided in the IC. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching. While OTP is active, the capacitor $C_{VCC}$ is not recharged from the HV mains. If the $V_{CC}$ supply voltage is not sufficient, the OTP circuit is supplied from the HV pin.

OTP is a safe restart protection.

## 7.2 Power factor correction circuit

The Power Factor Correction (PFC) circuit operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached the minimum value.

$V_{PFCAUX}$ is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

### 7.2.1 $t_{on}$ control (PFCCOMP pin)

The power factor correction circuit is operated in $t_{on}$ control. The resulting mains harmonic reduction is well within the class-C lighting requirements.

$V_{PFCCOMP}$ determines the on-time of the PFC. The $V_{VOSENSE}$ is the transconductance amplifier input which outputs current to the PFCCOMP pin. The regulation $V_{VOSENSE}$ = 2.5 V. The network connected to the PFCCOMP pin and the transconductance amplifier determine the dynamic behavior of the PFC control.

Operating near the PFC OVP level causes the PFC stage on-time to decrease rapidly to zero.

To reduce the response time, in case of load variation, the PFCCOMP pin is clamped to a minimum level of 1.19 V during PFC operation. Clamping prevents the on-time increasing too much and improves the PFC response time when the load decreases again.

### 7.2.2  Valley switching and demagnetization (PFCAUX pin)

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. To reduce switching losses and ElectroMagnetic Interference (EMI), the next stroke is started when the voltage across the PFC MOSFET is at its minimum (valley switching).

If a demagnetization signal is not detected on the PFCAUX pin, the controller generates a Zero-Current Signal (ZCS) 48 $\mu$s after the last PFC MOSFET gate signal.

If valley signal is not detected on the PFCAUX pin, the controller generates a valley signal 4.2 $\mu$s after demagnetization is detected.

To protect the internal circuitry during, for example, lightning events, add a 5 k$\Omega$ series resistor to the PFCAUX pin. To prevent incorrect switching due to external interference, place the resistor close to the IC on the PCB.

### 7.2.3  Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation is above the $f_{sw(PFC)max}$ limit, the system switches to DCM. The PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching).

### 7.2.4  Mains voltage compensation (VINSENSE pin)

The equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, it results in a low bandwidth for low mains input voltages.

To compensate for the influence of the mains input voltage, the SSL8516T contains a correction circuit. The average input voltage is measured using the VINSENSE pin and the information is fed to an internal compensation circuit. Using this compensation, it is possible to keep the regulation loop bandwidth constant over the mains input range. This feature gives a fast transient response on load steps while complying with class-C MHR requirements.

In a typical application, a resistor and two capacitors connected to the PFCCOMP pin set the regulation loop bandwidth.

### 7.2.5  Soft-start (PFCSENSE pin)

To prevent audible transformer noise at start-up or during hiccup, the soft-start function slowly increases the transformer peak current. Place a capacitor $C_{SS1}$ in parallel with resistor $R_{SS1}$ (see Figure 5) to implement a soft-start function. An internal current source charges the capacitor to:

$$V_{PFCSENSE} = I_{start(soft)PFC} \times R_{SS1} \tag{1}$$

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The voltage is limited to $V_{start(soft)PFC}$.

The start level and time constant of the increasing primary current level is externally adjusted by changing the $R_{SS1}$ and $C_{SS1}$ values.

$$\tau_{start(soft)PFC} = 3 \times R_{SS1} \times C_{SS1} \tag{2}$$

The charging current $I_{start(soft)PFC}$ flows while the PFCSENSE pin voltage is < 0.5 V. If $V_{PFCSENSE}$ exceeds 0.5 V, the soft-start current source starts limiting current $I_{start(soft)PFC}$. When the PFC starts switching, the $I_{start(soft)PFC}$ current source is switched off; see Figure 5.
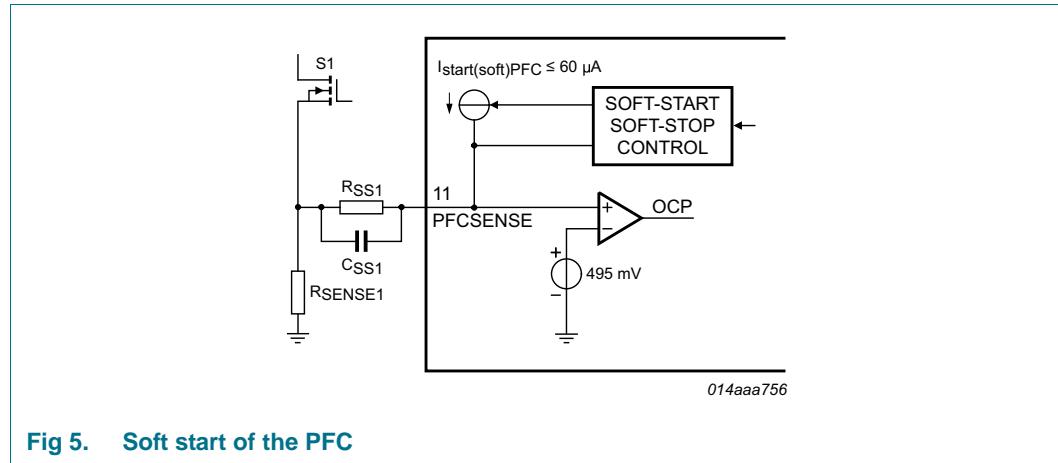


**Fig 5.  Soft start of the PFC**

### 7.2.6 PFC switch-on/switch-off control

When the flyback converter output power (see Section 7.3) is low, the flyback converter switches to FR mode. When the switching frequency of the flyback in FR mode < $f_{sw(fb)swoff(PFC)}$ (53 kHz), the PFC circuit is switched off to maintain high efficiency. Connect a capacitor to the PFCTIMER pin (see Section 7.2.7) to delay the PFC switching off.

During low-power mode operation and start-up (when PFC is disabled, e.g. at no-load), the PFCCOMP pin is clamped to a minimum voltage of 3.32 V or 1.18 V and a maximum voltage of 3.75 V. The minimum clamp voltage depends on $V_{VINSENSE}$. This voltage limits the maximum power that is delivered when the PFC switches on again. The upper clamp voltage ensures that the PFC returns from low-power mode to its normal regulation point in a limited time.

In FR mode, when the flyback converter switching frequency exceeds $f_{sw(fb)swon(PFC)}$ (73 kHz), the PFC circuit is switched on. If the flyback converter duty cycle is > 50 % or $V_{FBCTRL}$ is > 3.75 V, the PFC circuit is also switched on.

### 7.2.7 PFC switch off delay (PFCTIMER pin)

When the flyback converter switching frequency in FR mode is < $f_{sw(fb)swoff(PFC)}$ (53 kHz), the IC then outputs a 4.7 μA current to the PFCTIMER pin. When $V_{PFCTIMER}$ reaches 3 V, the PFC is switched off by performing a soft-stop.

A switch discharges the PFCTIMER pin capacitor when the flyback controller operating frequency is > $f_{sw(fb)swon(PFC)}$ (73 kHz). At the same moment, the PFC stage is also switched on.

Connect a capacitor to the PFCTIMER pin (see Section 7.2.7) to prevent the PFC from switching off due to a dynamic load that leads to repetitive crossing of $f_{sw(fb)swoff(PFC)}$ and $f_{sw(fb)swon(PFC)}$. A 1 nF minimum capacitor value is recommended to prevent noise influencing the PFC switch on/ switch off behavior.

The PFCTIMER pin capacitor is also discharged when PFC is on and the flyback switching frequency is higher than 53 kHz. This feature prevents PFC on/off toggling during dynamic loads causing the flyback to operate repetitively near $f_{sw(fb)swoff(PFC)}$ and $f_{sw(fb)swon(PFC)}$.

It is also possible to control PFC switch-on and switch off externally. When $V_{PFCTIMER}$ is driven below 1.03 V, the PFC stage is on. When the PFCTIMER pin voltage is driven above 4.4 V, the PFC stage is switched off. The external control overrides the PFC stage control by the flyback controller (see Figure 6).

The PFCTIMER pin has an internal clamp circuit starting around 10 V with a current capability of 0.1 mA
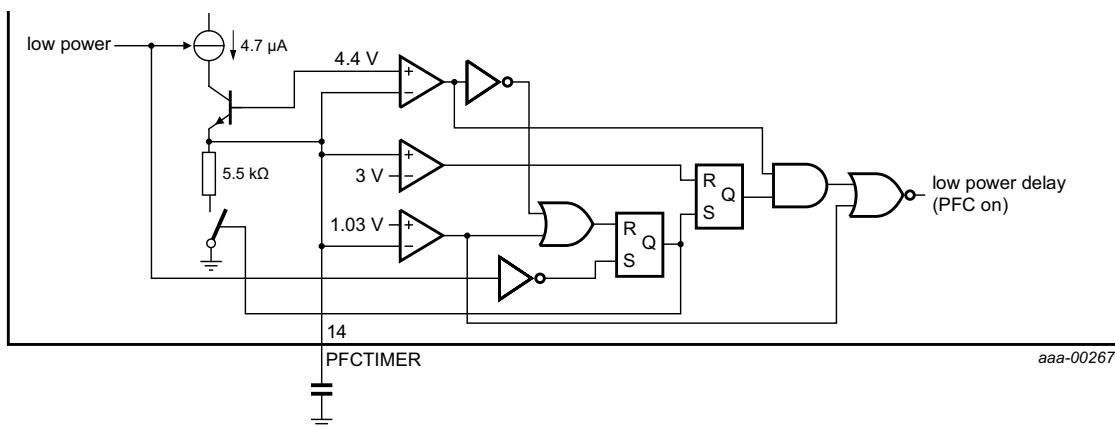


**Fig 6.    PFC switch on and switch off using the PFCTIMER pin**

### 7.2.8  Overcurrent protection (PFCSENSE pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor, $R_{SENSE1}$, on the source of the external MOSFET. The voltage is measured using the PFCSENSE pin.

### 7.2.9  Mains undervoltage lockout/brownout protection (VINSENSE pin)

To prevent the PFC from operating at very low mains input voltages, $V_{VINSENSE}$ is sensed continuously. When $V_{VINSENSE}$ drops below the $V_{stop(VINSENSE)}$ level, switching of the PFC is stopped.

### 7.2.10  Overvoltage protection (VOSENSE pin)

To prevent output overvoltage during load steps and mains transients, an overvoltage protection circuit is built in.

When $V_{VOSENSE}$ exceeds the $V_{OVP(VOSENSE)}$ level, switching of the PFC circuit is prevented. Switching of the PFC restarts when the VOSENSE pin voltage drops below the $V_{OVP(VOSENSE)}$ level again.

OVP is also triggered when the resistor between the VOSENSE pin and ground is open.

### 7.2.11 PFC open-loop protection (VOSENSE pin)

The PFC circuit does not start switching until the $V_{VOSENSE}$ pin is greater than the $V_{th(start)(VOSENSE)}$ level. This feature protects the application from open-loop and VOSENSE short-circuit situations.

### 7.2.12 Driver (PFCDRIVER pin)

The driver circuit to the gate of the power MOSFET includes a current sourcing capability of 500 mA at 2 V on the PFCDRIVER pin. It also includes a current sink capability of 1.2 A at 10 V on the PFCDRIVER pin. These capabilities ensure fast switch-on and switch-off of the power MOSFET for efficient operation.

## 7.3 Flyback controller

The SSL8516T includes a controller for a flyback converter. The flyback converter operates in quasi-resonant or discontinuous conduction mode with valley switching. The auxiliary winding of the flyback transformer provides demagnetization detection and powers the IC after start-up.

### 7.3.1 Multimode operation

The SSL8516T flyback controller can operate in several modes; see Figure 7.
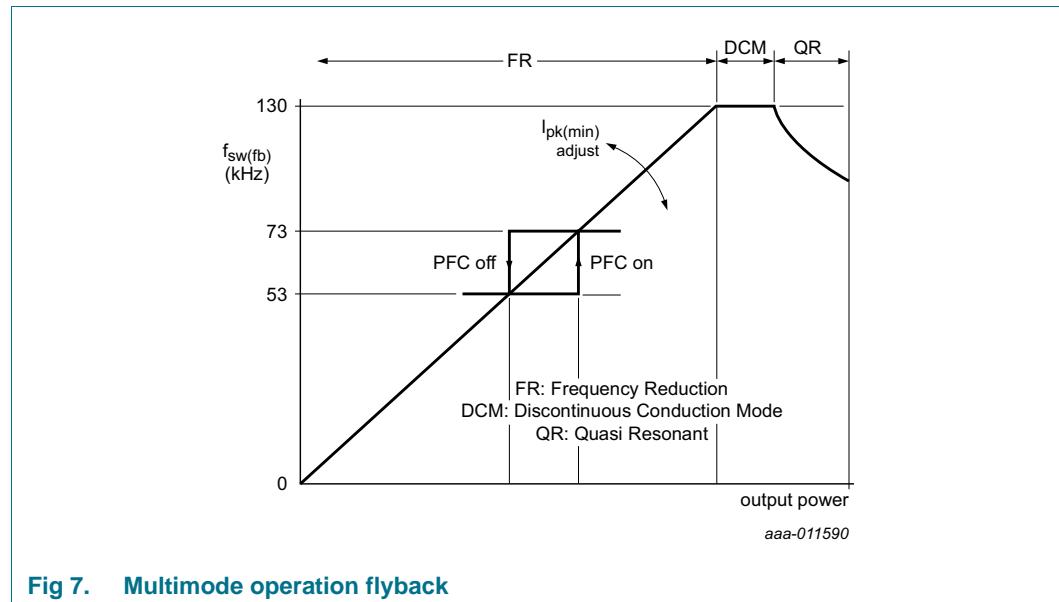


**Fig 7.  Multimode operation flyback**

At high output power the converter switches to quasi-resonant mode. The next converter stroke starts after demagnetization of the transformer and detection of the valley. In quasi-resonant mode switching losses are minimized. This minimization is achieved by the converter only switching on when the voltage across the external MOSFET is at its minimum (see Section 7.3.2).

Valley switching is active in all operating modes.

To prevent high frequency operation at lower loads, the quasi-resonant operation switches to discontinuous mode operation with valley skipping. When the frequency limit is reached, the quasi-resonant operation changes to DCM with valley skipping. The frequency limit reduces the MOSFET switch-on losses and conducted EMI.

At medium and low power levels, the controller enters Frequency Reduction (FR) mode. A Voltage Controlled Oscillator (VCO) controls the frequency. During frequency reduction mode, the primary peak current is kept at an adjustable minimal level to maintain a high efficiency. Valley switching is also active in this mode.

In frequency reduction mode, the PFC controller switches off when the flyback switching frequency has dropped to below 53 kHz and $V_{PFCTIMER}$ has reached 3 V. The flyback maximum frequency changes linearly with the control $V_{FBCTRL}$ (see Figure 8). Hysteresis is added to ensure a stable PFC switch-on and switch-off. In no-load operation, the switching frequency is reduced to (almost) zero.



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**Fig 8.    Flyback frequency control**
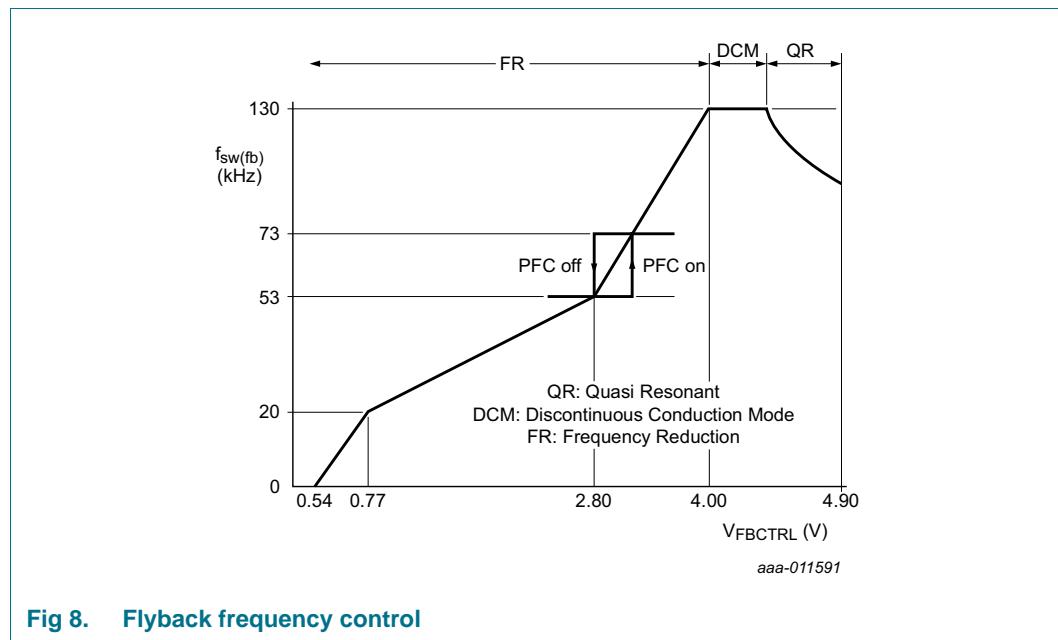
### 7.3.2  Valley switching (HV pin)

A new cycle starts when the external MOSFET is switched on. $V_{FBSENSE}$ and $V_{FBCTRL}$ determine the on-time. The MOSFET is then switched off and the secondary stroke starts (see Figure 9). After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately:

$$f = \frac{1}{[2 \times \pi \times \sqrt{(L_p \times C_d)}]} \tag{3}$$

where $L_p$ is the primary self-inductance of the flyback transformer and $C_d$ is the capacitance on the drain node.

When the secondary stroke ends and the internal oscillator voltage is high again, the circuit waits for the lowest drain voltage before starting a new primary stroke.

Figure 9 shows the drain voltage, valley signal, secondary stroke signal and the internal oscillator signal.

Valley switching allows high frequency operation because capacitive switching losses are reduced (see Equation 4). High frequency operation makes small and cost-effective magnetic components possible.

$$P = \frac{1}{2} \times C_d \times V^2 \times f \tag{4}$$



(1) Start of a new cycle at lowest drain voltage.

(2) Start of a new cycle in a classical Pulse-Width Modulation (PWM) system without valley detection.

**Fig 9.    Signals for valley switching**
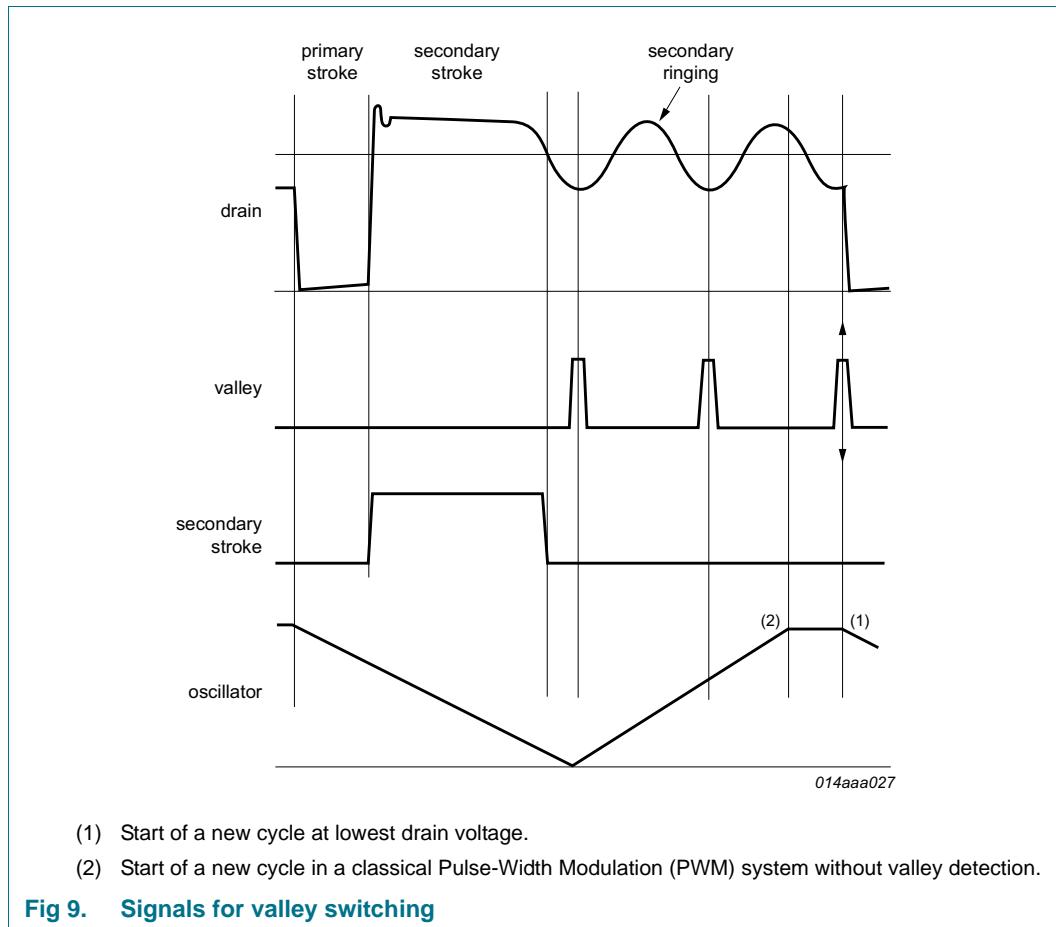
### 7.3.3  Current mode control (FBSENSE pin)

Current mode control is used for the flyback converter because of its good line regulation.

The FBSENSE pin senses the primary current across an external resistor and compares it to an internal control voltage. The internal control voltage is proportional to $V_{FBCTRL}$ (see Figure 10).

The FBSENSE pin outputs a current of 2.1 $\mu$A. This current runs through the resistors from the FBSENSE pin to the sense resistor $R_{SENSE2}$ and creates an offset voltage. Resistor $R_{SS2}$ causes the offset voltage because $R_{SENSE2}$ is relatively small. The minimum flyback peak current is adjusted using this offset voltage. Adjusting the minimum peak current level, changes the frequency reduction slope (see Figure 7).
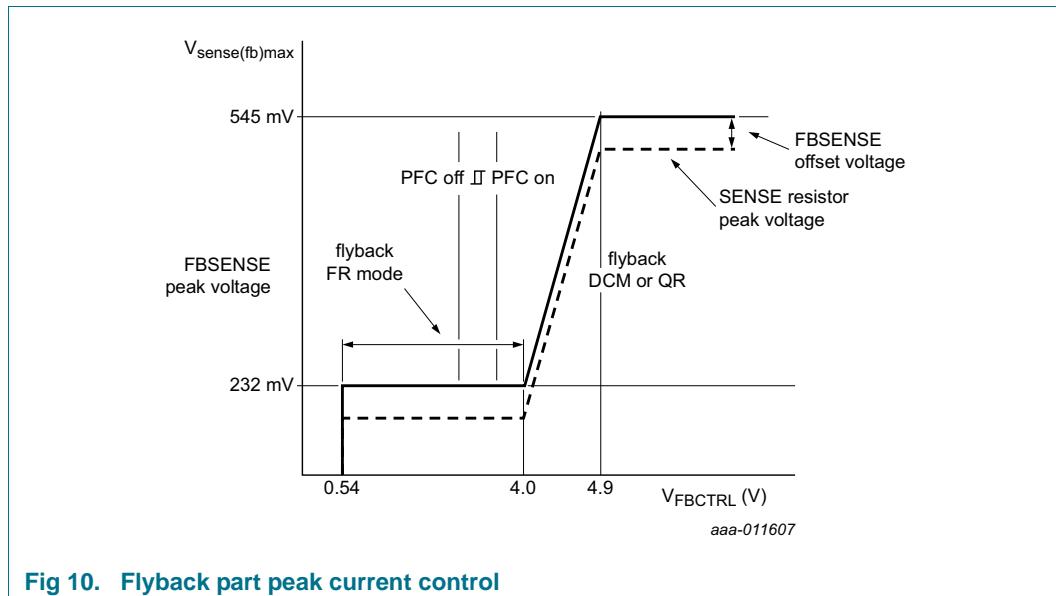
**Fig 10. Flyback part peak current control**

### 7.3.4 Demagnetization (FBAUX pin)

The system is always in QR or DCM. The internal oscillator does not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time) and reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time of 2.2 $\mu$s. This suppression can be necessary at low output voltages, during start-up and in applications where the transformer has a large leakage inductance.

If the FBAUX pin is open-circuit or not connected, a fault condition is assumed and the converter immediately stops. Operation restarts when the fault condition is removed.

### 7.3.5 Flyback control/time-out (FBCTRL pin)

The FBCTRL pin is connected to an internal voltage source of 7 V using an internal 13.2 k$\Omega$ resistor. When $V_{FBCTRL} > 5.5$ V, the resistor is disconnected. The pin is biased with a 29 $\mu$A current. When $V_{FBCTRL} > 7.75$ V, a fault is assumed, switching is stopped and a restart is made.

If a capacitor and resistor are connected in series to the pin, a time-out function is created which protects against open control loop situations. See Figure 11 and Figure 12. The time-out function is disabled by connecting a resistor (200 k$\Omega$) to ground on the FBCTRL pin.

If the pin is short-circuited to ground, switching of the flyback controller is stopped.

Under normal operating conditions, the converter regulates the output voltage. $V_{FBCTRL}$ varies between 0.54 V at minimum output power and 4.9 V at maximum output power.

**Fig 11. Time-out protection circuit**



**Fig 12. SSL8516T time-out protection (signals) and safe restart**
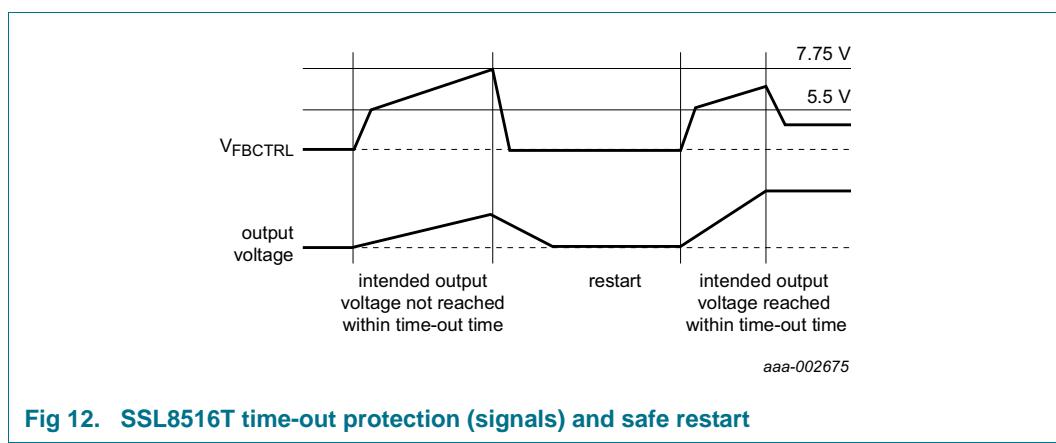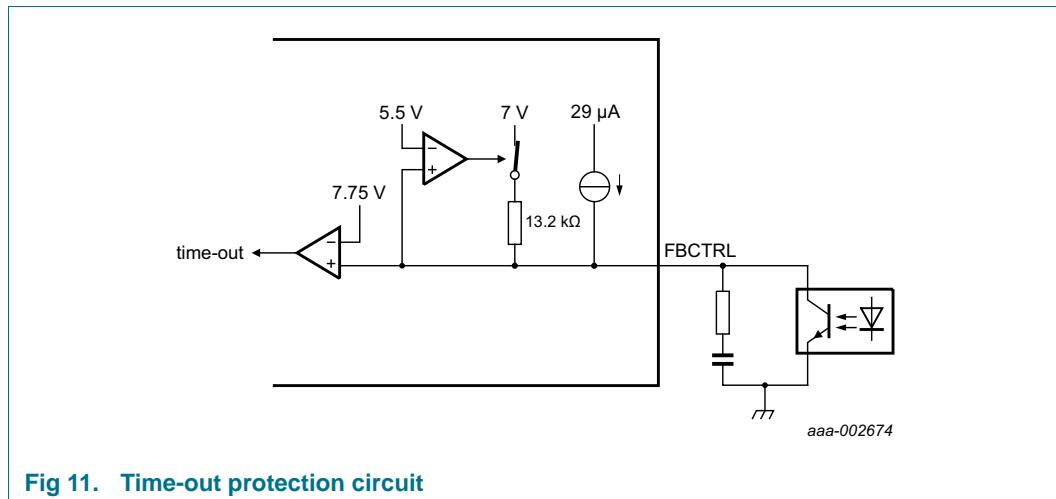
### 7.3.6 Soft-start (FBSENSE pin)

To prevent audible transformer noise during start-up, the soft-start function slowly increases the transformer peak current. Place a capacitor $C_{SS2}$ in parallel with resistor $R_{SS2}$ (see Figure 13) to implement the soft-start function.

An internal current source charges the capacitor to:

$$V = I_{start(soft)fb} \times R_{SS2}$$

(5)

with a maximum of 0.55 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of $R_{SS2}$ and $C_{SS2}$.

$$\tau_{start(soft)fb} = 3 \times R_{SS2} \times C_{SS2}$$

(6)

The soft-start current $I_{start(soft)fb}$ switches on when $V_{CC}$ reaches $V_{startup}$. When the $V_{FBSENSE}$ reaches 0.55 V, the flyback converter starts switching.

The charging current $I_{start(soft)fb}$ flows when the $V_{FBSENSE}$ is < 0.55 V. If $V_{FBSENSE}$ exceeds 0.55 V, the soft-start current source starts limiting the current. After the flyback converter has started, the soft-start current source is switched off.

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**Fig 13. Flyback soft-start**
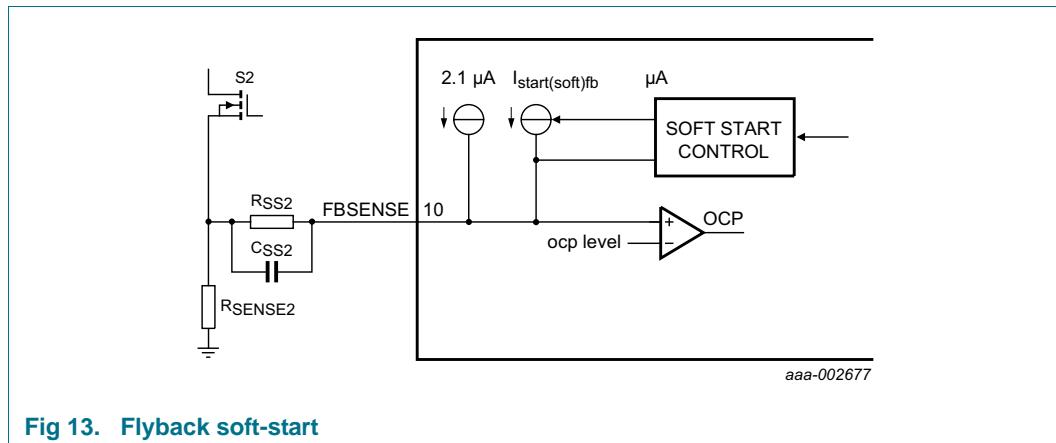
### 7.3.7 Maximum on-time

The flyback controller limits the on-time of the external MOSFET to 38.5 μs. When the on-time is longer than 38.5 μs, the IC stops switching and enters the safe restart state.

### 7.3.8 Overvoltage protection (FBAUX pin)

An output OVP is implemented in the GreenChip series. In the SSL8516T, the auxiliary voltage is sensed using the current flowing into the FBAUX pin during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. An internal filter averages voltage spikes.

An internal up-down counter prevents false OVP detection which can occur during ESD or lightning events. The internal counter counts up by one when the output voltage exceeds the OVP trip level within one switching cycle. The internal counter counts down by two when the output voltage has not exceeded the OVP trip level in one switching cycle. When the counter has reached six, the IC assumes a true overvoltage and triggers the safe start protection

The demagnetization resistor, $R_{FBAUX}$ sets the output voltage $V_{o(OVP)}$ at which the OVP function trips:

$$V_{o(OVP)} = \frac{N_s}{N_{aux}}(I_{ovp(FBAUX)} \times R_{FBAUX} + V_{clamp(FBAUX)})$$

(7)

where $N_s$ is the number of secondary windings and $N_{aux}$ is the number of auxiliary windings of the transformer. Current $I_{ovp(FBAUX)}$ is internally trimmed.

Accurate OVP detection is made possible by adjusting the value of $R_{FBAUX}$ to the turns ratio of the transformer.

### 7.3.9 Overcurrent protection (FBSENSE pin)

The primary peak current in the transformer is measured accurately cycle-by-cycle using the external sense resistor $R_{SENSE2}$. The OCP circuit limits $V_{FBSENSE}$ to a level set by $V_{FBCTRL}$ (see also Section 7.3.3). The OCP detection is suppressed during the leading-edge blanking period, $t_{leb}$ (equals $t_{on(fb)min} - t_{d(FBDRIVER)}$), to prevent false triggering due to switch-on spikes.

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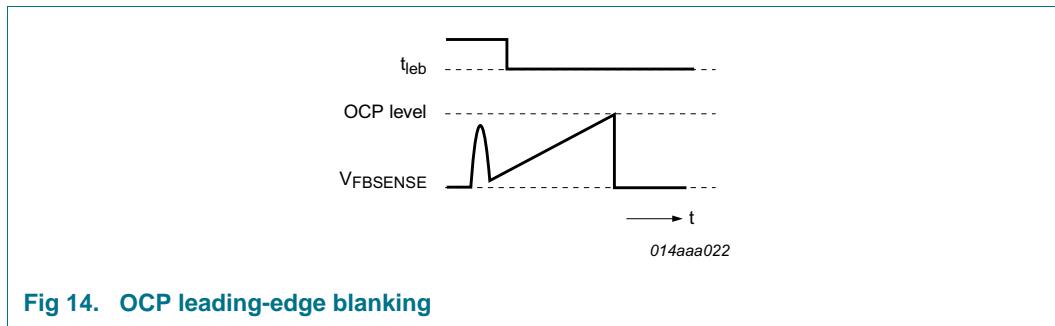
**Fig 14. OCP leading-edge blanking**

### 7.3.10 Overpower protection

During the flyback converter primary stroke, the flyback converter input voltage is measured by sensing the current that is drawn from the FBAUX pin.

The current information is used to limit the maximum flyback converter peak current and is measured using the FBSENSE pin. The internal compensation is such, that a maximum output power is obtained which is almost independent of the PFC output voltage.

The OPP curve is given in Figure 15.
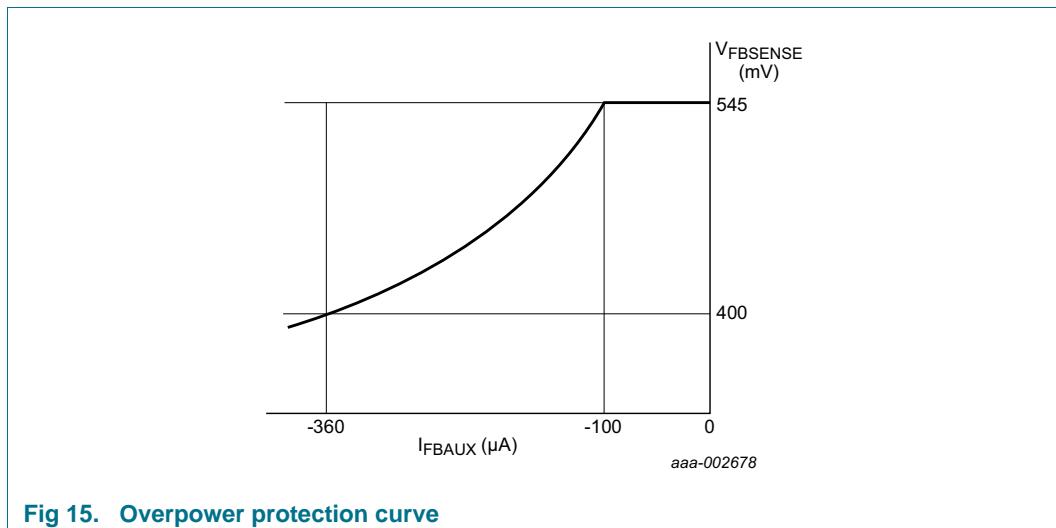


**Fig 15. Overpower protection curve**

### 7.3.11 Driver (FBDRIVER pin)

The driver circuit for the external power MOSFET gate includes a current sourcing capability of 500 mA at 2 V on the FBDRIVER pin. It also includes a current sink capability of 1.2 A at 10 V on the FBDRIVER pin. These capabilities ensure fast switch-on and switch-off of the power MOSFET for efficient operation.

## 8. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Voltages** | | | | | |
| $V_{CC}$ | supply voltage | | −0.4 | +38 | V |
| $V_{LATCH}$ | voltage on pin LATCH | current limited | −0.4 | +10 | V |
| $V_{FBCTRL}$ | voltage on pin FBCTRL | | −0.4 | +9 | V |
| $V_{PFCCOMP}$ | voltage on pin PFCCOMP | | −0.4 | +5 | V |
| $V_{VINSENSE}$ | voltage on pin VINSENSE | current limited | −0.4 | +10 | V |
| $V_{VOSENSE}$ | voltage on pin VOSENSE | current limited | −0.4 | +10 | V |
| $V_{PFCAUX}$ | voltage on pin PFCAUX | | −25 | +25 | V |
| $V_{FBSENSE}$ | voltage on pin FBSENSE | current limited | −0.4 | +5 | V |
| $V_{PFCSENSE}$ | voltage on pin PFCSENSE | current limited | −0.4 | +5 | V |
| $V_{PFCTIMER}$ | voltage on pin PFCTIMER | current limited | −0.4 | +10 | V |
| $V_{HV}$ | voltage on pin HV | | −0.4 | +650 | V |
| **Currents** | | | | | |
| $I_{FBCTRL}$ | current on pin FBCTRL | | −3 | 0 | mA |
| $I_{FBAUX}$ | current on pin FBAUX | | −1 | +1 | mA |
| $I_{PFCSENSE}$ | current on pin PFCSENSE | | −1 | +10 | mA |
| $I_{FBSENSE}$ | current on pin FBSENSE | | −1 | +10 | mA |
| $I_{FBDRIVER}$ | current on pin FBDRIVER | $\delta < 10\ \%$ | −0.8 | +2 | A |
| $I_{PFCDRIVER}$ | current on pin PFCDRIVER | $\delta < 10\ \%$ | −0.8 | +2 | A |
| $I_{PFCTIMER}$ | current on pin PFCTIMER | | −1 | +0.1 | mA |
| $I_{HV}$ | current on pin HV | during start-up and restart | - | 8 | mA |
| | | $\delta = 3\ \%$ due to dV/dt on HV pin | −15 | +30 | mA |
| **General** | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} < 75\ °C$ | - | 0.6 | W |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_j$ | junction temperature | | −40 | +155 | °C |
| **ESD** | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | human body model | | | |
| | | pins 1 to 14 [1] | −2 | 2 | kV |
| | | pin 16 (HV) [1] | −1.5 | 1.5 | kV |
| | | charged device model | −500 | 500 | V |

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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## 9. Thermal characteristics

**Table 4.    Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|--------|-----------|------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; JEDEC test board | 127 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | in free air; JEDEC test board | 36 | K/W |

## 10. Characteristics

**Table 5.    Characteristics**

$T_{amb} = 25\ °C$; $V_{CC} = 20\ V$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| **Start-up current source (HV pin)** | | | | | | |
| $I_{HV}$ | current on pin HV | $V_{HV} > 75\ V$ | | | | |
| | | $V_{CC} < V_{trip}$ | 0.9 | 1.1 | 1.3 | mA |
| | | $V_{th(UVLO)} < V_{CC} < V_{startup}$; initial start-up | 4 | 5 | 6 | mA |
| | | $V_{th(UVLO)} < V_{CC} < V_{startup}$; restart | 0.8 | 1 | 1.2 | mA |
| | | $V_{trip} < V_{CC} < V_{th(UVLO)}$ | 4 | 5 | 6 | mA |
| | | with auxiliary supply | - | - | 1.5 | µA |
| | | in Power-down mode; $V_{CC} = 0\ V$ | 5 | 12 | 25 | µA |
| $V_{BR}$ | breakdown voltage | | 650 | - | - | V |
| **Supply voltage management ($V_{CC}$ pin)** | | | | | | |
| $V_{trip}$ | trip voltage | | 0.5 | 0.6 | 0.7 | V |
| $V_{startup}$ | start-up voltage | | 21.3 | 22.3 | 23.3 | V |
| $V_{th(UVLO)}$ | undervoltage lockout threshold voltage | | 12.4 | 13.4 | 14.4 | V |
| $V_{hys}$ | hysteresis voltage | $V_{startup} - V_{th(UVLO)}$ | 8.3 | 8.9 | 9.5 | V |
| $I_{ch(low)}$ | low charging current | $V_{HV} > 75\ V$ | | | | |
| | | $V_{CC} < V_{trip}$ | −1.15 | −1 | −0.85 | mA |
| | | $V_{th(UVLO)} < V_{CC} < V_{startup}$ | −1.05 | −0.9 | −0.75 | mA |
| $I_{ch(high)}$ | high charging current | $V_{HV} > 75\ V$; $V_{trip} < V_{CC} < V_{th(UVLO)}$ | −5.8 | −4.9 | −4 | mA |
| | | $V_{th(UVLO)} < V_{CC} < V_{startup}$; initial start-up | −5.8 | −4.9 | −4 | mA |
| $I_{CC(oper)}$ | operating supply current | no-load on pins FBDRIVER and PFCDRIVER; $V_{FBCTRL} = 5\ V$; $f_{FB} = f_{PFC} = 100\ kHz$; $\delta = 30\ \%$ | 2.45 | 2.7 | 2.95 | mA |
| | | no-load on pins FBDRIVER and PFCDRIVER; flyback switching; $V_{FBCTRL} = 0.77\ V$; $V_{PFCSENSE} = 0\ V$ | 2.6 | 2.9 | 3.2 | mA |
| $I_{CC(prot)}$ | protection supply current | time-out protection triggered; $V_{HV} = 0\ V$ | 0.3 | 0.45 | 0.6 | mA |
| $I_{CC(pd)}$ | power-down mode supply current | IC in power-down mode; $V_{HV} = 0\ V$ | 0.3 | 0.45 | 0.6 | mA |

**Table 5.    Characteristics** *…continued*

$T_{amb} = 25\ °C$; $V_{CC} = 20\ V$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input voltage sensing PFC (VINSENSE pin)** | | | | | | |
| $V_{stop(VINSENSE)}$ | stop voltage on pin VINSENSE | | 0.86 | 0.89 | 0.92 | V |
| $V_{start(VINSENSE)}$ | start voltage on pin VINSENSE | | 1.12 | 1.16 | 1.20 | V |
| $V_{flr}$ | fast latch reset voltage | active after $V_{th(UVLO)}$ is detected | 0.6 | 0.75 | 0.9 | V |
| $V_{flr(hys)}$ | hysteresis of fast latch reset voltage | | 60 | 110 | 160 | mV |
| $I_{I(VINSENSE)}$ | input current on pin VINSENSE | $V_{VINSENSE} > V_{stop(VINSENSE)}$ after $V_{start(VINSENSE)}$ is detected | 5 | 20 | 50 | nA |
| $V_{th(sel)clmp}$ | clamp select threshold voltage | on pin VINSENSE | 1.9 | 2 | 2.1 | V |
| $V_{th(sel)clmp(hys)}$ | clamp select threshold voltage hysteresis | | 60 | 100 | 140 | mV |
| $V_{th(pd)}$ | power-down threshold voltage | | 285 | 385 | 485 | mV |
| $V_{th(pd)exit}$ | exit power-down threshold voltage | $V_{CC} = 0\ V$ | 335 | 460 | 585 | mV |
| $V_{hys(pd)}$ | power-down hysteresis voltage | | 45 | 75 | 105 | mV |
| **Loop compensation PFC (PFCCOMP pin)** | | | | | | |
| $g_m$ | transconductance | $V_{VOSENSE}$ to $I_{O(PFCCOMP)}$ | 57 | 77 | 97 | μA/V |
| $I_{O(PFCCOMP)}$ | output current on pin PFCCOMP | $V_{VOSENSE} = 2\ V$; $V_{PFCCOMP} = 2.75\ V$ | 30 | 37 | 44 | μA |
| | | $V_{VOSENSE} = 3.3\ V$; $V_{PFCCOMP} = 2.75\ V$ | −108 | −88 | −68 | μA |
| $I_{en(PFCCOMP)}$ | enable current on pin PFCCOMP | | - | −55 | - | μA |
| $V_{clamp(PFCCOMP)}$ | clamp voltage on pin PFCCOMP | low-power mode; PFC off; initial start-up; lower clamp voltage. [1] | | | | |
| | | VINSENSE ≥ $V_{th(sel)clmp}$ + $V_{th(sel)clmp(hys)}$ on pin VINSENSE; $V_{VOSENSE} = 2\ V$ [2] | 3.2 | 3.32 | 3.44 | V |
| | | VINSENSE < $V_{th(sel)clmp}$ on pin VINSENSE; $V_{VOSENSE} = 2\ V$ [2] | 1.06 | 1.18 | 1.30 | V |
| | | upper clamp voltage | 3.6 | 3.75 | 3.9 | V |
| | | high-power mode; PFC on; uni-directional source clamp; $I_{PFCCOMP} = −30\ μA$; $V_{VOSENSE} = 2.5\ V$ | 1.09 | 1.19 | 1.29 | V |
| $V_{ton(PFCCOMP)zero}$ | zero on-time voltage on pin PFCCOMP | | 3.4 | 3.5 | 3.6 | V |

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**Table 5.    Characteristics** *…continued*

$T_{amb} = 25\ °C$; $V_{CC} = 20\ V$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Pulse-width modulator PFC** | | | | | | |
| $t_{on(PFC)}$ | PFC on-time | $V_{VINSENSE} = 3.3\ V$; $V_{VOSENSE} = 2\ V$; $V_{PFCCOMP} = V_{clamp(PFCCOMP)}$ (lower clamp) | 3.6 | 4.7 | 5.8 | µs |
| | | $V_{VINSENSE} = 1\ V$; $V_{VOSENSE} = 2\ V$; $V_{PFCCOMP} = V_{clamp(PFCCOMP)}$ (lower clamp) | 33 | 46 | 59 | µs |
| **Output voltage sensing PFC (VOSENSE pin)** | | | | | | |
| $V_{th(start)VOSENSE}$ | start threshold voltage on pin VOSENSE | open-loop | 0.45 | 0.5 | 0.55 | V |
| $V_{th(stop)VOSENSE}$ | threshold stop voltage on pin VOSENSE | | 0.35 | 0.4 | 0.45 | V |
| $V_{hys(VOSENSE)}$ | hysteresis voltage on pin VOSENSE | $V_{th(start)VOSENSE} - V_{th(stop)VOSENSE}$ | 75 | 100 | 125 | mV |
| $V_{reg(VOSENSE)}$ | regulation voltage on pin VOSENSE | for $I_{O(PFCCOMP)} = 0\ A$ | 2.475 | 2.5 | 2.525 | V |
| $V_{OVP(VOSENSE)}$ | | $t_{on} = 0\ µs$ | 2.59 | 2.62 | 2.65 | V |
| $I_{prot(VOSENSE)}$ | protection current on pin VOSENSE | | −50 | −25 | −5 | nA |
| **Overcurrent protection PFC (PFCSENSE pin)** | | | | | | |
| $V_{sense(PFC)max}$ | maximum PFC sense voltage | $\Delta V/\Delta t = 0\ V/s$ | 465 | 495 | 525 | mV |
| $t_{d(PFCDRIVER)}$ | delay time on pin PFCDRIVER | $V_{PFCSENSE}$ pulse-stepping 400 mV around $V_{sense(PFC)max}$ | - | 50 | - | ns |
| $t_{leb(PFC)}$ | PFC leading edge blanking time | $V_{PFCSENSE} = 0.75\ V$ | 230 | 290 | 350 | ns |
| $I_{prot(PFCSENSE)}$ | protection current on pin PFCSENSE | | −50 | - | −5 | nA |
| **Soft-start PFC (PFCSENSE pin)** | | | | | | |
| $I_{start(soft)PFC}$ | PFC soft start current | | −73 | −60 | −47 | µA |
| $V_{start(soft)PFC}$ | PFC soft start voltage | enabling voltage | 0.45 | 0.5 | 0.55 | V |
| $V_{stop(soft)PFC}$ | PFC soft stop voltage | disabling voltage | 0.4 | 0.45 | 0.5 | V |
| **Oscillator PFC** | | | | | | |
| $f_{sw(PFC)max}$ | maximum PFC switching frequency | | 320 | 400 | 480 | kHz |
| $t_{off(PFC)min}$ | minimum PFC off-time | secondary stroke | 0.8 | 1.1 | 1.4 | µs |
| **Valley switching PFC (PFCAUX pin)** | | | | | | |
| $(\Delta V/\Delta t)_{vrec(PFC)}$ | PFC valley recognition voltage change with time | | - | - | 1.7 | V/µs |
| $t_{to(vrec)PFC}$ | PFC valley recognition time-out time | | 3 | 4.2 | 5.4 | µs |

**Table 5.    Characteristics** *…continued*

$T_{amb} = 25\ ^{\circ}C$; $V_{CC} = 20$ V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Demagnetization management PFC (PFCAUX pin)** | | | | | | |
| $V_{th(comp)PFCAUX}$ | comparator threshold voltage on pin PFCAUX | | −125 | −90 | −55 | mV |
| $t_{to(demag)PFC}$ | PFC demagnetization time-out time | | 39 | 48 | 57 | µs |
| $I_{prot(PFCAUX)}$ | protection current on pin PFCAUX | $V_{PFCAUX} = 50$ mV | −75 | - | −5 | nA |
| **PFC off delay (PFCTIMER pin)** | | | | | | |
| $I_{source(PFCTIMER)}$ | source current on pin PFCTIMER | $V_{PFCTIMER} = 2.5$ V | −5.4 | −4.7 | −4 | µA |
| $R_{sink(PFCTIMER)}$ | sink resistance on pin PFCTIMER | $V_{PFCTIMER} = 2.5$ V | 4 | 5.5 | 7 | kΩ |
| $V_{start(PFCTIMER)}$ | start voltage on pin PFCTIMER | | 0.93 | 1.03 | 1.13 | V |
| $V_{stop(PFCTIMER)}$ | stop voltage on pin PFCTIMER | | 2.85 | 3 | 3.15 | V |
| $V_{th(off)PFCTIMER}$ | switch-off threshold voltage on pin PFCTIMER | PFC override voltage | 4.2 | 4.4 | 4.6 | V |
| **Driver (PFCDRIVER pin)** | | | | | | |
| $I_{src(PFCDRIVER)}$ | source current on pin PFCDRIVER | $V_{PFCDRIVER} = 2$ V | - | −0.5 | - | A |
| $I_{sink(PFCDRIVER)}$ | sink current on pin PFCDRIVER | $V_{PFCDRIVER} = 2.5$ V | - | 0.7 | - | A |
| $V_{O(PFCDRIVER)max}$ | maximum output voltage on pin PFCDRIVER | | 10 | 11 | 12 | V |
| **OverVoltage Protection flyback (FBAUX pin)** | | | | | | |
| $I_{ovp(FBAUX)}$ | overvoltage protection current on pin FBAUX | | 279 | 300 | 321 | µA |
| **Demagnetization management flyback (FBAUX pin)** | | | | | | |
| $V_{th(comp)FBAUX}$ | comparator threshold voltage on pin FBAUX | | 60 | 90 | 120 | mV |
| $I_{prot(FBAUX)}$ | protection current on pin FBAUX | $V_{FBAUX} = 50$ mV | −65 | - | −5 | nA |
| $V_{clamp(FBAUX)}$ | clamp voltage on pin FBAUX | $I_{FBAUX} = -100$ µA | −0.75 | −0.7 | −0.65 | V |
| | | $I_{FBAUX} = 300$ µA | 0.87 | 0.92 | 0.97 | V |
| $t_{sup(xfmr\_ring)}$ | transformer ringing suppression time | | 1.7 | 2.2 | 2.7 | µs |
| **Pulse width modulator flyback** | | | | | | |
| $t_{on(fb)max}$ | maximum flyback on-time | | 32.5 | 38.5 | 44.5 | µs |

**Table 5.** **Characteristics** *…continued*

$T_{amb} = 25\ ^\circ C;\ V_{CC} = 20\ V;$ all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator flyback** | | | | | | |
| $f_{sw(fb)max}$ | maximum flyback switching frequency | | 110 | 130 | 150 | kHz |
| $V_{start(red)f}$ | frequency reduction start voltage | transfer from DCM/QR to FR mode | 3.8 | 4 | 4.2 | V |
| $f_{sw(fb)swon(PFC)}$ | PFC switch-on flyback switching frequency | | 70 | 73 | 76 | kHz |
| $f_{sw(fb)swoff(PFC)}$ | PFC switch-off flyback switching frequency | | 50 | 53 | 56 | kHz |
| $V_{en(PFC)FBCTRL}$ | PFC enable voltage on pin FBCTRL | override voltage | 3.4 | 3.75 | 4.1 | V |
| $f_{sw(fb)VCO}$ | VCO flyback switching frequency | $V_{FBCTRL} = 2.8\ V$ | 45 | 53 | 61 | kHz |
| | | $V_{FBCTRL} = 0.77\ V$ | 16 | 20 | 24 | kHz |
| $V_{swoff(fb)FBCTRL}$ | flyback switch-off voltage on pin FBCTRL | | 0.4 | 0.54 | 0.68 | V |
| **Peak current control flyback (FBCTRL pin)** | | | | | | |
| $V_{FBCTRL}$ | voltage on pin FBCTRL | for maximum flyback peak current | 4.6 | 4.9 | 5.2 | V |
| $V_{to(FBCTRL)}$ | time-out voltage on pin FBCTRL | enable voltage | 5.3 | 5.5 | 5.7 | V |
| | | trip voltage | 7.3 | 7.75 | 8.2 | V |
| $I_{O(FBCTRL)}$ | output current on pin FBCTRL | $V_{FBCTRL} = 0\ V$ | −0.75 | −0.6 | −0.45 | mA |
| | | $V_{FBCTRL} = 4.5\ V$ | −0.3 | −0.24 | −0.18 | mA |
| $I_{to(FBCTRL)}$ | time-out current on pin FBCTRL | $V_{FBCTRL} = 6\ V$ | −35 | −29 | −23 | µA |
| $R_{int(FBCTRL)}$ | internal resistance on pin FBCTRL | | 9.8 | 13.2 | 16.5 | kΩ |
| **Valley switching flyback (HV pin)** | | | | | | |
| $(\Delta V/\Delta t)_{vrec(fb)}$ | flyback valley recognition voltage change with time | [3] | −75 | - | +75 | V/µs |
| $t_{d(vrec-swon)}$ | valley recognition to switch-on delay time | [3] | - | 75 | - | ns |
| **Soft-start flyback (FBSENSE pin)** | | | | | | |
| $I_{start(soft)fb}$ | flyback soft start current | | −75 | −60 | −45 | µA |
| $V_{start(soft)fb}$ | flyback soft start voltage | enable voltage | 0.5 | 0.55 | 0.6 | V |
| **OverCurrent Protection (OCP) flyback (FBSENSE pin)** | | | | | | |
| $V_{sense(fb)max}$ | maximum flyback sense voltage | $\Delta V/\Delta t = 0\ V/s$ | 525 | 545 | 565 | mV |
| $V_{sense(fb)min}$ | minimum flyback sense voltage | $\Delta V/\Delta t = 0\ V/s$ | 221 | 232 | 243 | mV |

**Table 5.    Characteristics** *…continued*

$T_{amb} = 25\ °C$; $V_{CC} = 20\ V$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(FBDRIVER)}$ | delay time on pin FBDRIVER | $V_{FBSENSE}$ pulse-stepping 400 mV around $V_{sense(fb)max}$ | - | 80 | - | ns |
| $t_{on(fb)min}$ | minimum flyback on-time | $V_{FBCRTL} = 3\ V$; $V_{FBSENSE} = 0.75\ V$ | 280 | 340 | 400 | ns |
| $I_{adj(FBSENSE)}$ | adjust current on pin FBSENSE | | −2.29 | −2.1 | −1.91 | µA |
| **OverPower Protection (OPP) flyback (FBSENSE pin)** | | | | | | |
| $V_{sense(fb)max}$ | maximum flyback sense voltage | $\Delta V/\Delta t = 0\ V/s$ | | | | |
| | | $I_{FBAUX} = 80\ µA$ | 525 | 545 | 565 | mV |
| | | $I_{FBAUX} = 120\ µA$ | 495 | 540 | 565 | mV |
| | | $I_{FBAUX} = 240\ µA$ | 400 | 445 | 490 | mV |
| | | $I_{FBAUX} = 360\ µA$ | 345 | 400 | 455 | mV |
| **Driver (FBDRIVER pin)** | | | | | | |
| $I_{src(FBDRIVER)}$ | source current on pin FBDRIVER | $V_{FBDRIVER} = 2\ V$ | - | −0.5 | - | A |
| $I_{sink(FBDRIVER)}$ | sink current on pin FBDRIVER | $V_{FBDRIVER} = 2.5\ V$ | - | 0.7 | - | A |
| $V_{O(FBDRIVER)(max)}$ | maximum output voltage on pin FBDRIVER | | 10 | 11 | 12 | V |
| **LATCH input (LATCH pin)** | | | | | | |
| $V_{prot(LATCH)}$ | protection voltage on pin LATCH | | 469 | 494 | 519 | mV |
| $I_{O(LATCH)}$ | output current on pin LATCH | $V_{prot(LATCH)} < V_{LATCH} < V_{oc(LATCH)}$ | −32.5 | −30.5 | −28.5 | µA |
| $V_{en(LATCH)}$ | enable voltage on pin LATCH | at start-up | 552 | 582 | 612 | mV |
| $V_{hys(LATCH)}$ | hysteresis voltage on pin LATCH | $V_{en(LATCH)} − V_{prot(LATCH)}$ | 68 | 88 | 108 | mV |
| $V_{oc(LATCH)}$ | open-circuit voltage on pin LATCH | | - | 1.75 | - | V |

**Table 5.    Characteristics** *…continued*

$T_{amb} = 25\ °C$; $V_{CC} = 20\ V$; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| **Temperature protection** | | | | | | |
| $T_{pl(IC)}$ | IC protection level temperature | | 135 | 145 | 155 | °C |
| $T_{pl(IC)hys}$ | hysteresis of IC protection level temperature | [3] | - | 10 | - | °C |

[1]  A typical application with a compensation network on the PFCCOMP pin, such as the example in Figure 3.

[2]  The clamp voltage on the PFCCOMP pin is dependent on the VINSENSE voltage. When the $V_{VINSENSE}$ rises above $V_{th(sel)clmp} + V_{th(sel)clmp(hys)}$, the high clamp level is active. When the voltage on the VINSENSE pin drops below the $V_{th(sel)clmp}$ level again, the low clamp level is active.

[3]  Guaranteed by design.

## 11. Application information

An LED driver with the SSL8516T consists of a PFC circuit and a flyback converter (see Figure 16).

Capacitor $C_{VCC}$ buffers the IC supply voltage. The IC supply is charged from the high voltage rectified mains during start-up and the auxiliary winding of the flyback converter during operation. Sense resistors $R_{SENSE1}$ and $R_{SENSE2}$ convert the current through the MOSFETs S1 and S2 into a voltage on the PFCSENSE and FBSENSE pins. The $R_{SENSE1}$ and $R_{SENSE2}$ values define the maximum primary peak current in MOSFETs S1 and S2.

In the example, the LATCH pin is connected to a Negative Temperature Coefficient (NTC) resistor. The protection is activated when the resistance drops below the value as calculated in Equation 8:

$$\frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = 16.2\ k\Omega \tag{8}$$

Capacitor $C_{TIMEOUT}$ is connected to the FBCTRL pin. $R_{LOOP}$ ensures that the time-out capacitor does not interfere with the flyback regulation control loop.

$R_{S1}$ and $R_{S2}$ prevent that the soft-start capacitors $C_{SS1}$ and $C_{SS2}$ are charged during normal operation due to negative voltage spikes across the sense resistors.

Resistor $R_{AUX1}$ protects the IC from damage during lightning events.

$R_{S3}$ and $R_{COMP}$ can be used to lower the PFC on/off power level. The minimum and maximum peak current ratio increase. So, the PFC switch-on and switch-off power level decreases.

$R_{DRV1}$ and $R_{DRV2}$ prevent that the internal MOSET drivers are damaged due to, for example, power MOSFET avalanche.

Depending on the drain voltage maximum rating of MOSFET S2, the HV pin of the IC can either be connected to the center tap of the flyback transformer or to the drain of MOSFET S2.

(1) In the application, the HV pin of the IC can either be connected to the center tap of the flyback transformer or to the drain of MOSFET S2.

**Fig 16.  SSL8516T typical application diagram**
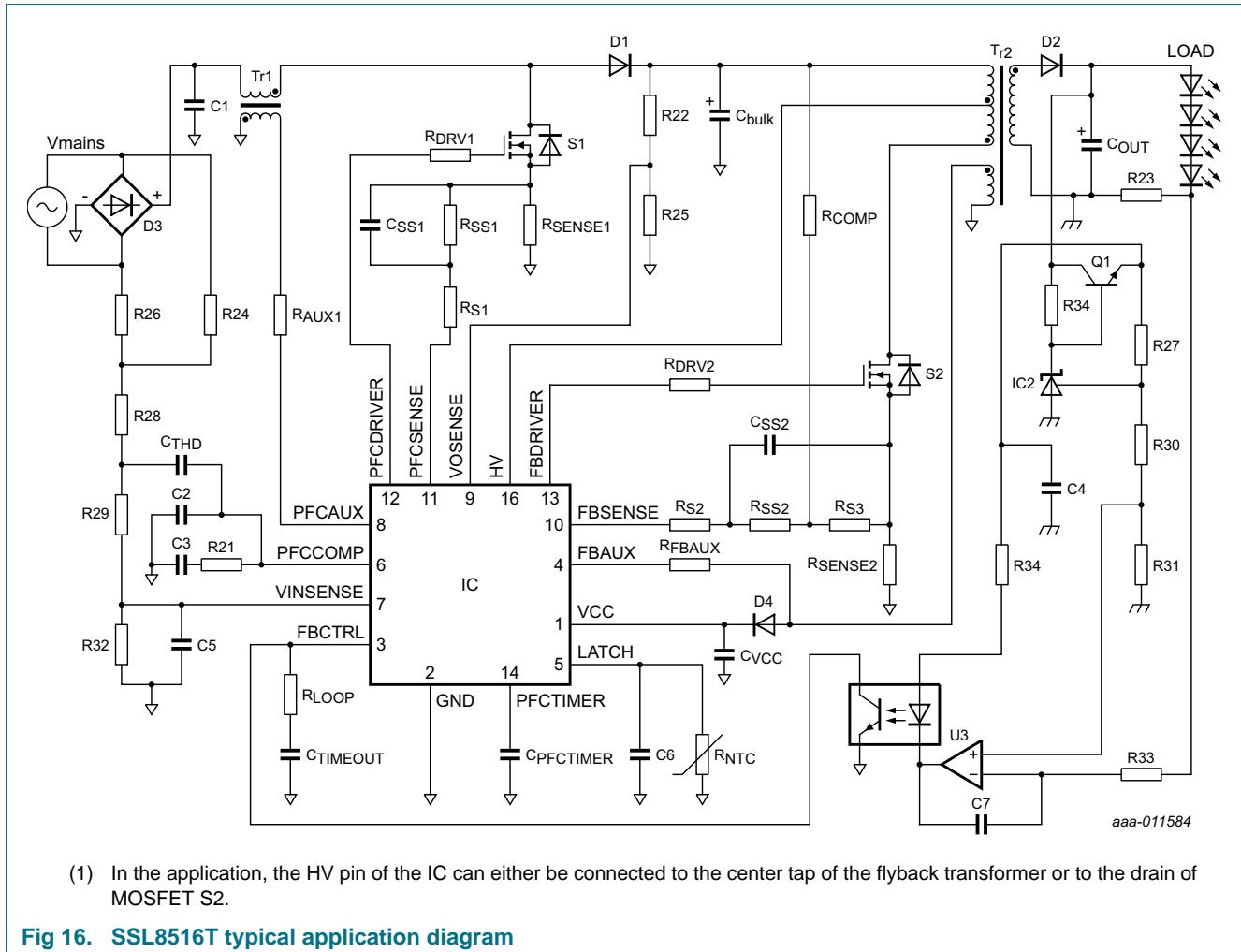
## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**
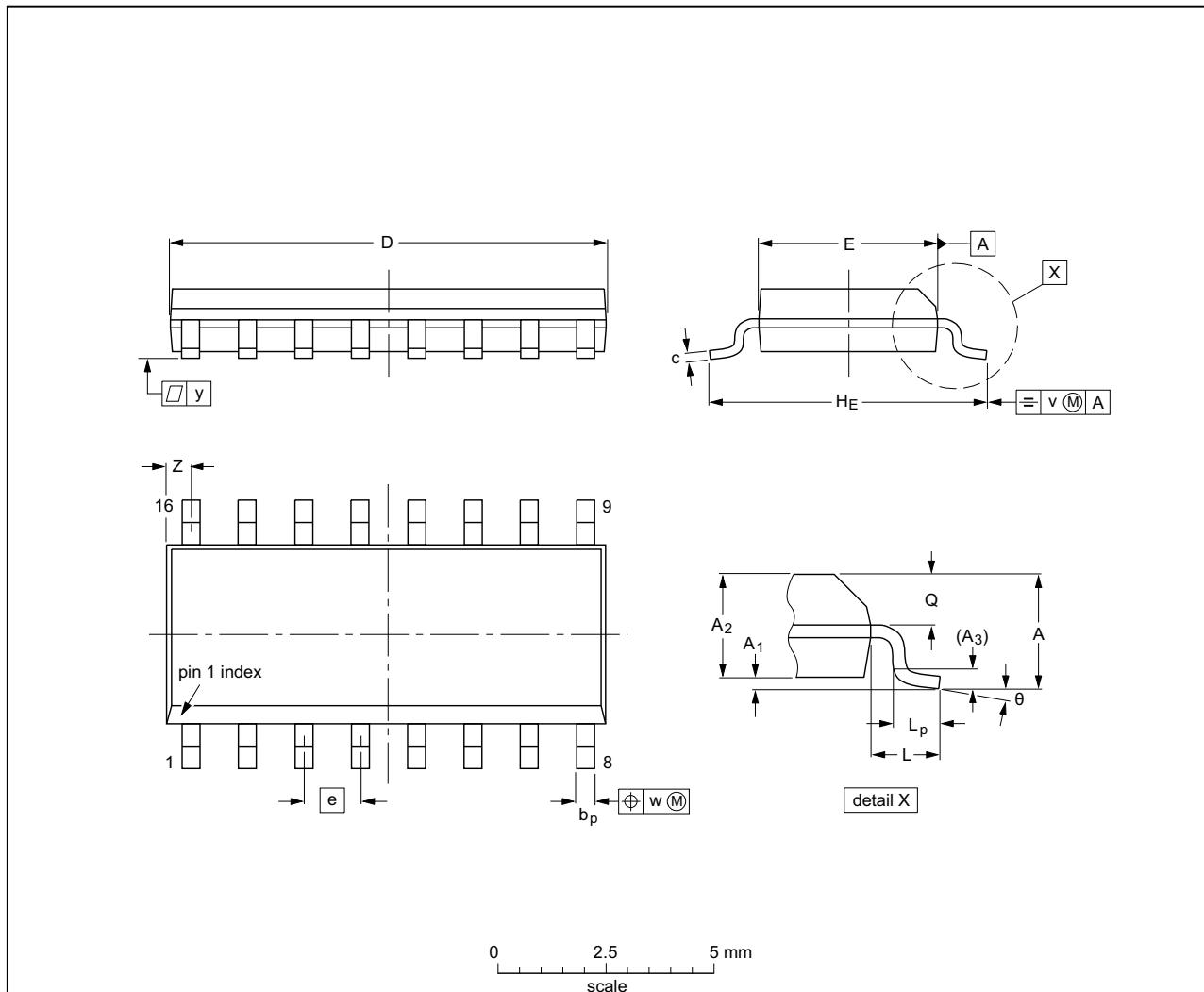


**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D[1] | E[1] | e | Hₑ | L | Lₚ | Q | v | w | y | Z[1] | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | 99-12-27 03-02-19 |

**Fig 17. Package outline SOT109-1 (SO16)**

## 13. Revision history

**Table 6.    Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SSL8516T v.1 | 20140505 | Product data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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