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FEUL620Q150A-02

ML620Q150A Series
User's Manual

16-bit Microcontroller

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Preface

This manual describes the operation of the hardware of the 16-bit microcontroller ML620Q150A Series.

The following manuals are also available. Read them as necessary.

■ nX-U16/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U16/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual
Description about the connection between uEASE.

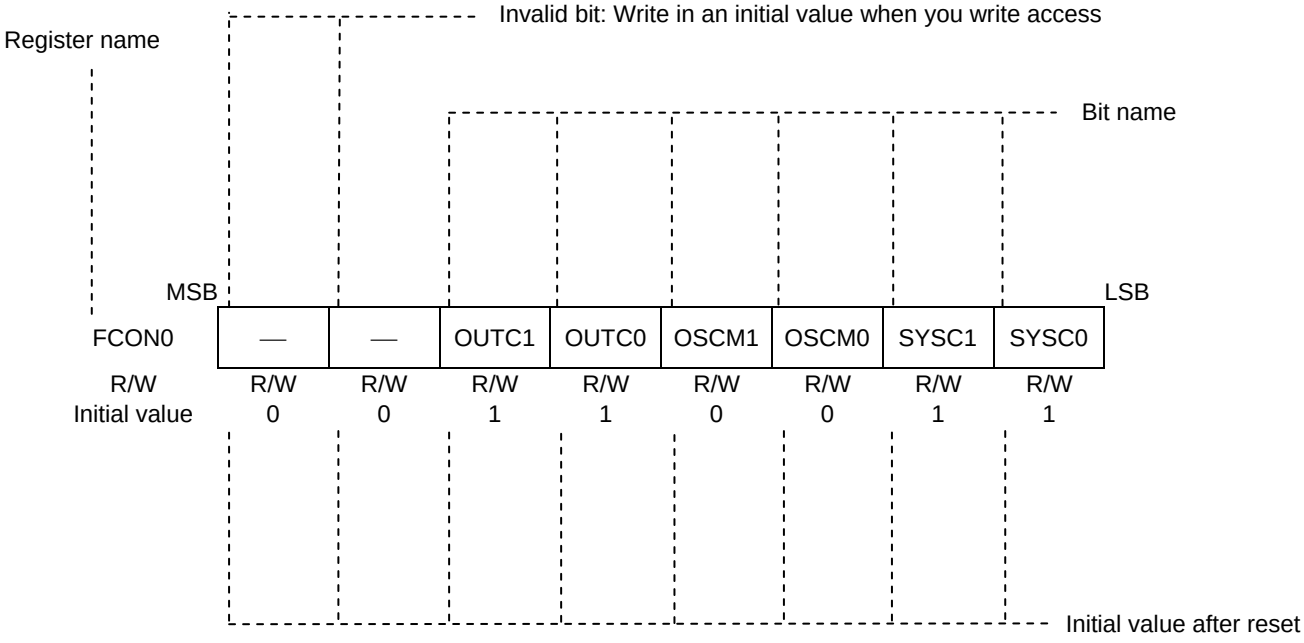
■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1 Overview

1. Overview

1.1 Features

This LSI is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Low level detect circuit, are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel procesing. and, this LSI has a data flash-memory fill area by a software which can be written in. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system:16-bit instructions
  - Instruction set:Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 s (at 32.768kHz system clock)
    Approx 0.122s (at 8.192MHz system clock)

- Internal memory
  - Flash-memory

Product	Program area	Rewrite cycle
ML620Q151A/ML620Q154A/ML620Q157A	32-Kbyte* (16K × 16-bit)	100
ML620Q152A/ML620Q155A/ML620Q158A	48-Kbyte* (24K × 16-bit)	
ML620Q153A/ML620Q156A/ML620Q159A	64-Kbyte* (32K × 16-bit)	

  * including unusable 1KByte TEST area
    Internal 2-Kbyte Data Flash (1-Kbyte × 2) Rewrite cycle: 10,000 times
  - SRAM: Internal 2-Kbyte RAM (2-Kbyte × 8 -bits)

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: BACK-UP CLOCK, WDT)
  - maskable interrupt

Product	Interrupt source
ML620Q151A/ML620Q154A/ML620Q157A	27 (Internal source: 20, External source: 7)
ML620Q152A/ML620Q155A/ML620Q158A	28 (Internal source: 20, External source: 8)
ML620Q153A/ML620Q156A/ML620Q159A	28 (Internal source: 20, External source: 8)

  - 4 steps of interrupt level, and a mask function

- Time base counter
  - Low-speed time base counter × 1 channel

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s @32.768kHz)

- Timers
  - 8 bits x 2ch (16-bits configuration available x 1ch)
  - 16 bits x 4ch

- PWM
  - 16 bits x 4ch
  - The auto reload timer mode / PWM mode
  - Timer start-stop function by the software and an external trigger.
  - A pulse width can be measured using an external-trigger input.
  - An external event can be selected as the counter clock.
  - Complement synchronous PWM

- Synchronous serial port
  - 1ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Full-duplex × 1ch (Half-duplex × 2ch)
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I2C bus interface
  - Master function only
  - Fast mode (400kbit/s), Standard mode (100kbit/s)

- Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 12ch（Maximum）
  - Conversion time: 43us, 13.5 s per channel (conversion-time is selectable)

- Analog Comparator
  1ch
  Edge for the interrupt and sampling function is selectable.

- General-purpose ports (including multiple functions)
  - Input-only ports

Product	Input-only ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	6ch	5ch
ML620Q154A/ML620Q155A/ML620Q156A	7ch	6ch
ML620Q157A/ML620Q158A/ML620Q159A	7ch	6ch

  - Output-only ports : 4ch
  - Input/output ports

Product	Input/output ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	31ch	30ch
ML620Q154A/ML620Q155A/ML620Q156A	34ch	33ch
ML620Q157A/ML620Q158A/ML620Q159A	46ch	45ch

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset by the Low Level Detector (LLD)

- LLD(Low Level Detector) function
  - Threshold voltages: 4values (1.9V/2.55V/3.7V/4.2V)
  - A threshold voltage is selected as Code-Option.
  - LLD is a ready as a supply-voltage supervisory reset.
  - Reset or an interrupt output is selectable as Code-Option.

- Clock
  - Low-speed clock (This LSI can not guarantee the operation without low-speed clock)
  - Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.768kHz)
  - Crystal oscillation or Built-in RC oscillation is selectable as Code-Option.
  - High-speed clock
  - Built-in RC oscillation (2.097MHz) or Built-in PLL oscillation (8.192MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

- Package

Product	Package
ML620Q151A/ML620Q152A/ML620Q153A	48pinTQFP (P-TQFP48-0707-0.50-QK)
ML620Q154A/ML620Q155A/ML620Q156A	52pinTQFP (P-TQFP52-1010-0.65-TK)
ML620Q157A/ML620Q158A/ML620Q159A	64pinQFP (P-QFP64-1414-0.80-UK)

- Guaranteed operating range
  - Operating temperature: –40°C to +105°C
  - Operating voltage: V_{DD} = 1.8V to 5.5V

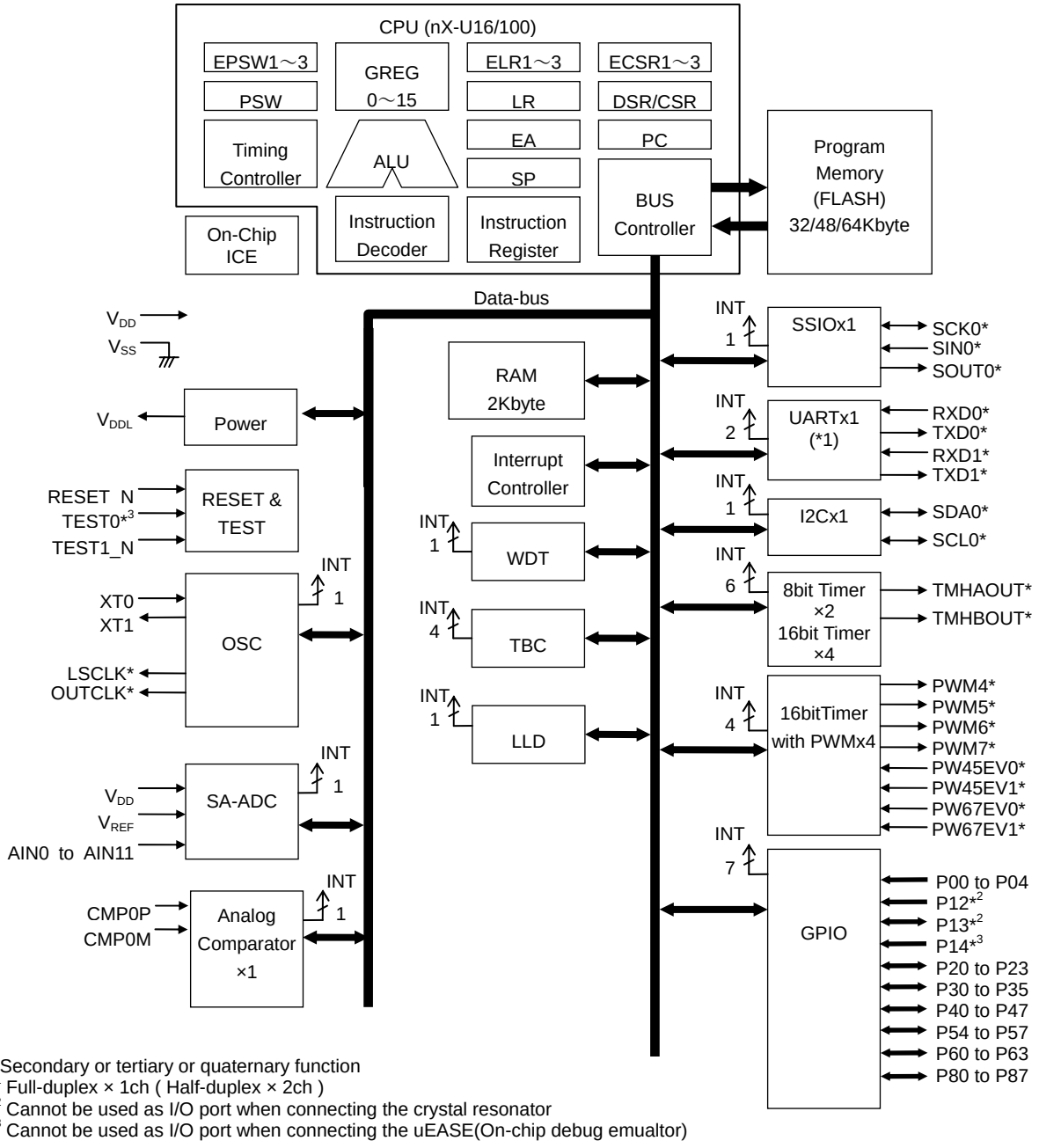
The difference point of this LSI is shown below.

function		ML620Q151A/152A/153A	ML620Q154A/155A/156A	ML620Q157A/158A/159A
Shipment		48pinTQFP	52pinTQFP	64pinQFP
flash capacity (program area)		32Kbyte(ML620Q151A) 48Kbyte(ML620Q152A) 52Kbyte(ML620Q153A)	32Kbyte(ML620Q154A) 48Kbyte(ML620Q155A) 52Kbyte(ML620Q156A)	32Kbyte(ML620Q157A) 48Kbyte(ML620Q158A) 52Kbyte(ML620Q159A)
maskable interrupt		27	28	28
Input-only port (At the case of crystal unused)		6	7	7
	P05 port	–	Available	Available
Input/output port (At the case of crystal unused)		31	34	46
	P36,P53,P64 ports	–	Available	Available
	P37 port	–	–	Available
	P50～P52 ports	–	–	Available
	P65～P67 ports	–	–	Available
	P70～P74 ports	–	–	Available

—:none

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)



* Secondary or tertiary or quaternary function
*1 Full-duplex × 1ch (Half-duplex × 2ch)
*2 Cannot be used as I/O port when connecting the crystal resonator
*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emualtor)

Figure 1-1 Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)

1.2.2 Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)

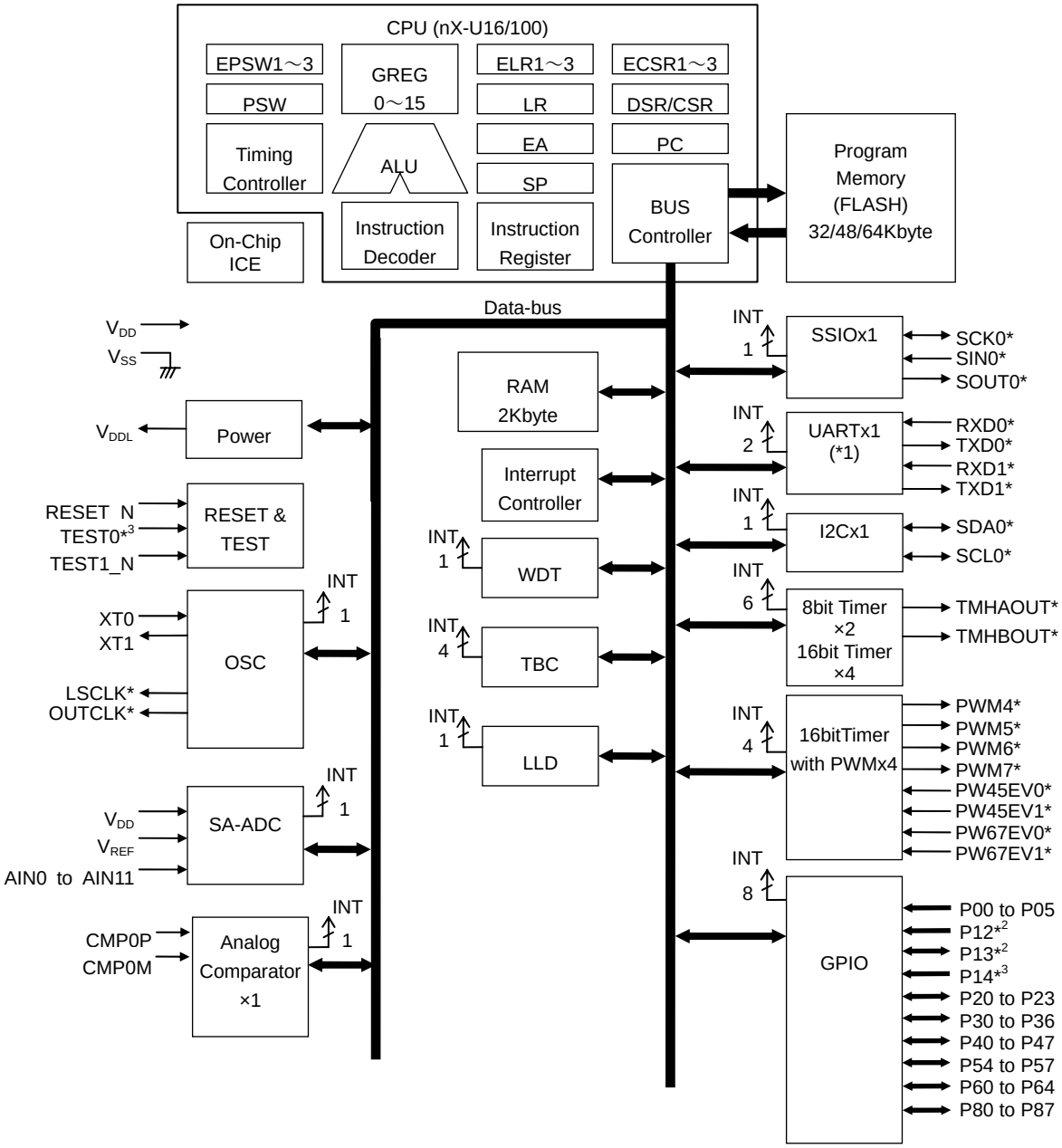


Figure 1-2 Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)

1.2.3 Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)

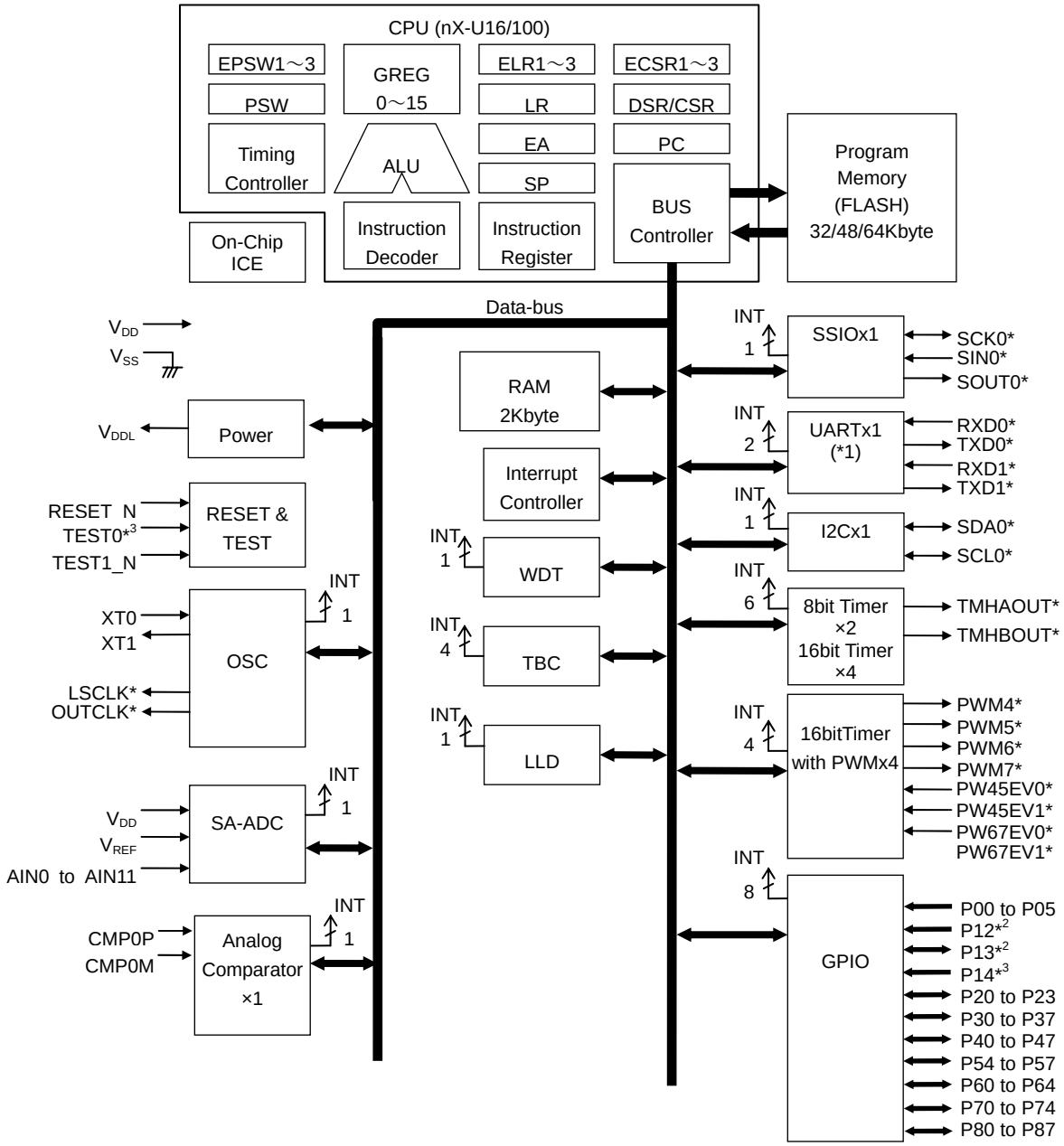


Figure 1-3 Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML620Q151A/ML620Q152A/ML620Q153A TQFP48 package product

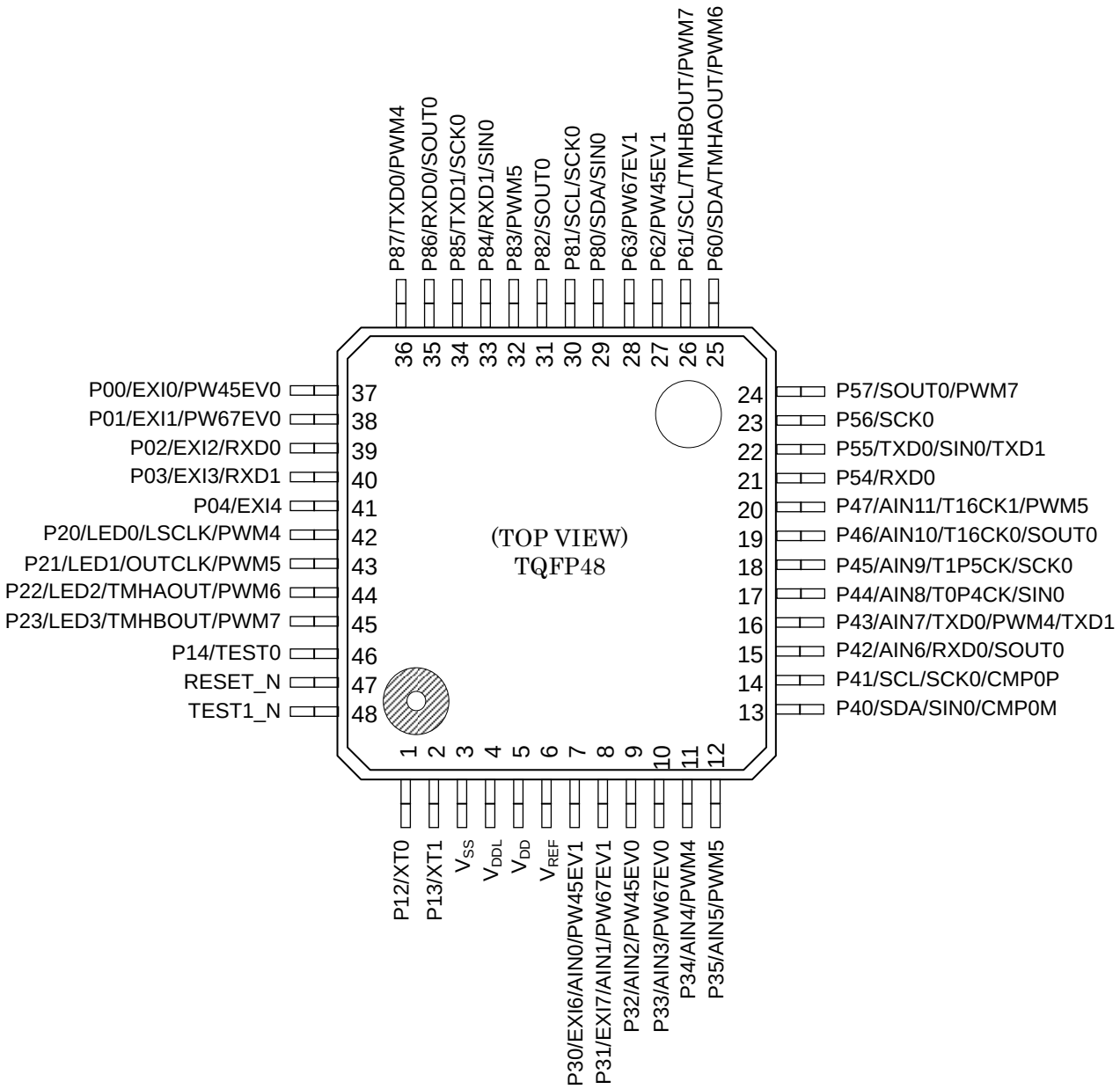


Figure 1-4 Pin Layout of ML620Q151A/ML620Q152A/ML620Q153A TQFP48 Package

1.3.1.2 Pin Layout of ML620Q154A/ML620Q155A/ML620Q156A TQFP52 package product

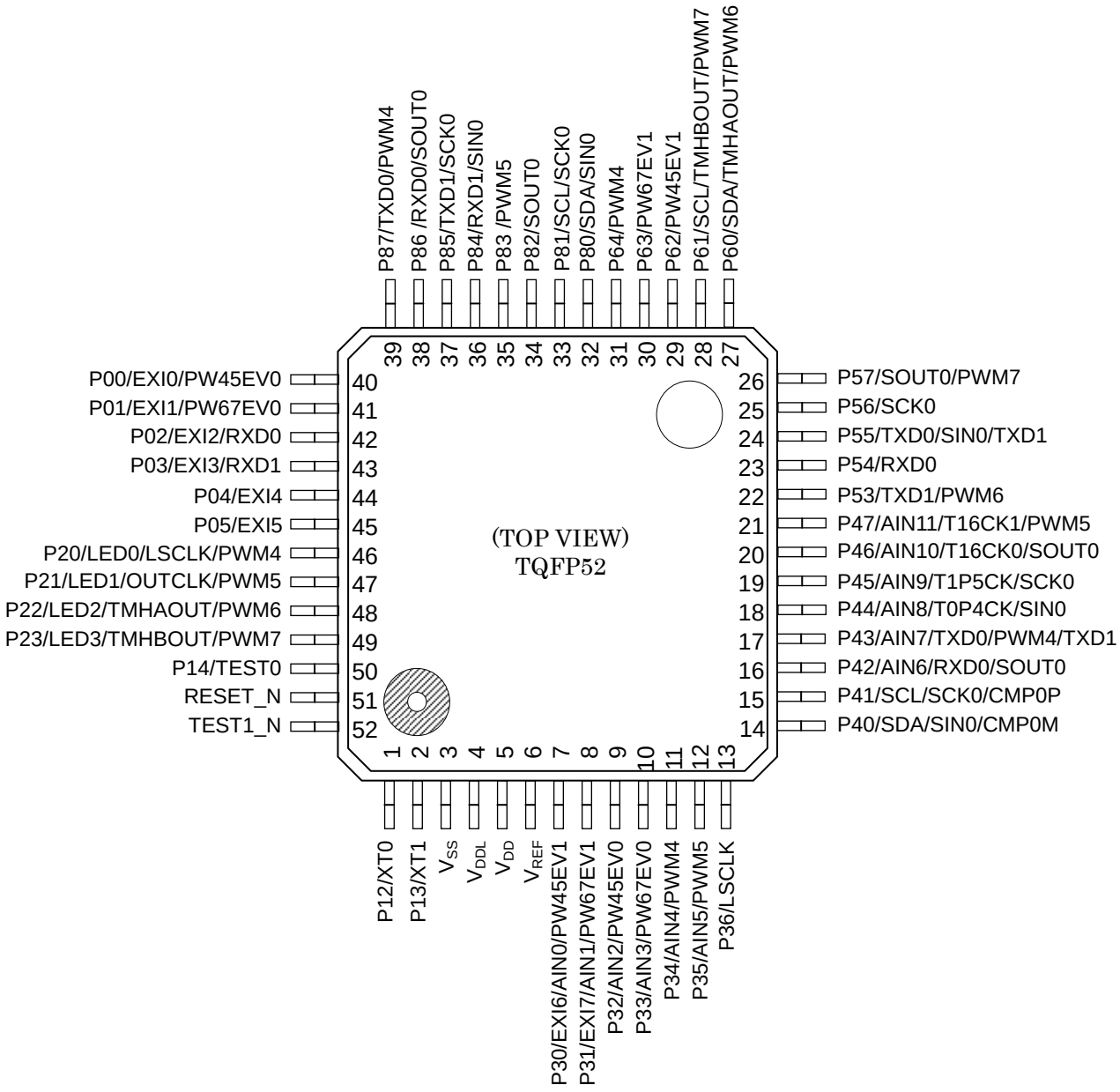


Figure 1-5 Pin Layout of ML620Q154A/ML620Q155A/ML620Q156A TQFP52 Package

1.3.1.3 Pin Layout of ML620Q157A/ML620Q158A/ML620Q159A QFP64 package product

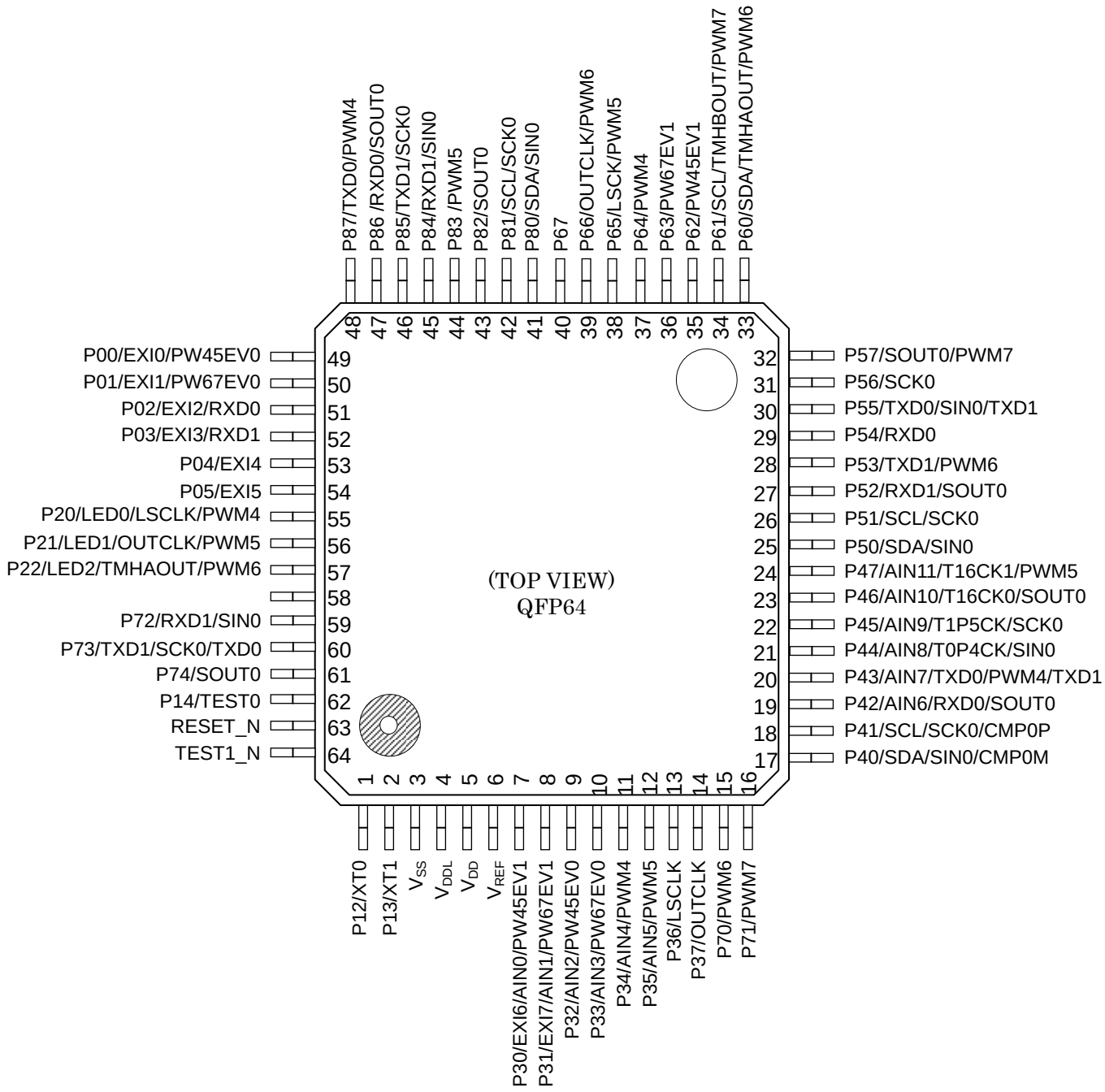


Figure 1-6 Pin Layout of ML620Q157A/ML620Q158A/ML620Q159A QFP64 Package

1.3.2 List of Pins

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
3	3	3	Vss	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
5	5	5	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
4	4	4	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—	—	—	—
46	50	62	P14/ TEST0	I	Input port/ Input pin for testing	—	—	—	—	—	—	—	—	—
47	51	63	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
48	52	64	TEST1_N	I	Input pin for testing	—	—	—	—	—	—	—	—	—
1	1	1	P12/ XT0	I	Input port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
2	2	2	P13/ XT1	I/O	Input/output port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
6	6	6	V_{REF}	—	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—	—	—	—
37	40	49	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—	—	—	—
38	41	50	P01/EXI1/ PW67EV0	I	Input port / External interrupt / PW67EV0 input	—	—	—	—	—	—	—	—	—
39	42	51	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—	—	—	—
40	43	52	P03/EXI3/ RXD1	I	Input port / External interrupt UART1 data input	—	—	—	—	—	—	—	—	—
41	44	53	P04/EXI4	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
—	45	54	P05/EXI5	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
42	46	55	P20/ LED0/	O	Output port / LED drive	LSCLK	O	Low-speed clock output	PWM4	O	PWM4 output	—	—	—
43	47	56	P21/ LED1/	O	Output port / LED drive	OUTCLK	O	Low-speed clock output	PWM5	O	PWM5 output	—	—	—
44	48	57	P22/ LED2/	O	Output port / LED drive	—	—	—	TMHAOUT	O	TimerA output	PWM6	O	PWM6 output
45	49	58	P23/ LED3/	O	Output port / LED drive	—	—	—	TMHBOUT	O	TimerB output	PWM7	O	PWM7 output
7	7	7	P30/EXI6 PW45EV1/ AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
8	8	8	P31/EXI7 PW67EV1/ AIN1	I/O	Input/output port / PW67EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
9	9	9	P32/ PW45EV0/ AIN2	I/O	Input/output port / PW45EV0 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
10	10	10	P33/ PW67EV0/ AIN3	I/O	Input/output port / PW67EV0 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
11	11	11	P34/ AIN4/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM4	O	PWM4 output	—	—	—
12	12	12	P35/ AIN5/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	13	13	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
—	—	14	P37	I/O	Input/output port	OUTCLK	O	Low-speed clock output	—	—	—	—	—	—
13	14	17	P40/ CMP0M	I/O	Input/output port / Comparator0 inverting input	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input	—	—	—
14	15	18	P41/ CMP0P	I/O	Input/output port / Comparator0 non-inverting input	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
15	16	19	P42/ AIN6	I/O	Input/output port / Successive approximation type ADC input	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
16	17	20	P43/ AIN7	I/O	Input/output port / Successive approximation type ADC input	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UART1 data output
17	18	21	P44/ T0P4CK/ AIN8	I/O	Input/output port / PWM4 external clock input/ Successive approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input	—	—	—
18	19	22	P45/ T1P5CK/ AIN9	I/O	Input/output port / PWM5 external clock input/ Successive approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
19	20	23	P46/ T16CK0/ AIN10	I/O	Input/output port / Timer8,A / PWM6 external clock input / Successive approximation type ADC input	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
20	21	24	P47/ T16CK1/ AIN11	I/O	Input/output port / Timer9,B / PWM7 external clock input / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	—	25	P50	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input			
—	—	26	P51	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output			
—	—	27	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT0	O	SSIO0 data output			
—	22	28	P53	I/O	Input/output port	TXD1	O	UART1 data output	PWM6	O	PWM6 output	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
21	23	29	P54	I/O	Input/output port	RXD0	I	UART0 data input	—	—	—	—	—	—
22	24	30	P55	I/O	Input/output port	TXD0	O	UART0 data output	SIN0	I	SSIO0 data input	TXD1	O	UART1 data output
23	25	31	P56	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
24	26	32	P57	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	PWM7	O	PWM7 output
25	27	33	P60	I/O	Input/output port	SDA	I/O	I^2C data input/output	TMHAOUT	O	TimerA output	PWM6	O	PWM6 output
26	28	34	P61	I/O	Input/output port	SCL	I/O	I^2C clock input/output	TMHBOUT	O	TimerB output	PWM7	O	PWM7 output
27	29	35	P62/ PW45EV1	I/O	Input/output port / PW45EV1 input	—	—	—	—	—	—	—	—	—
28	30	36	P63/ PW67EV1	I/O	Input/output port / PW67EV1 input	—	—	—	—	—	—	—	—	—
—	31	37	P64	I/O	Input/output port	—	—	—	PWM4	O	PWM4 output	—	—	—
—	—	38	P65	I/O	Input/output port	LSCLK	O	Low-speed clock output	PWM5	O	PWM5 output	—	—	—
—	—	39	P66	I/O	Input/output port	OUTCLK	O	Low-speed clock output	PWM6	O	PWM6 output	—	—	—
—	—	40	P67	I/O	Input/output port	—	—	—	—	—	—	—	—	—
—	—	15	P70	I/O	Input/output port	—	—	—	PWM6	O	PWM6 output	—	—	—
—	—	16	P71	I/O	Input/output port	—	—	—	PWM7	O	PWM7 output	—	—	—
—	—	59	P72	I/O	Input/output port	RXD1	I	UART1 data input	SIN0	I	SSIO0 data input	—	—	—
—	—	60	P73	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchronous clock input/output	TXD0	O	UART0 data output
—	—	61	P74	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
29	32	41	P80	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input	—	—	—
30	33	42	P81	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
31	34	43	P82	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
32	35	44	P83	I/O	Input/output port	—	—	—	PWM5	O	PWM5 output	—	—	—
33	36	45	P84	I/O	Input/output port	RXD1	I	UART1 data input	SIN0	I	SSIO0 data input	—	—	—
34	37	46	P85	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
35	38	47	P86	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
36	39	48	P87	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	—	—	—

1.3.3 Pin Descriptions

Table 1-2 Pin Descriptions (1/3)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C_L) (see Measuring Circuit 1) between this pin and V_{SS} .	—	—
Test				
TEST0	I	Input/output pin for testing.	—	Positive
TEST1_N	I	Input/output pin for testing. This pin has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and VSS as required.	—	—
XT1	O		—	—
LSCLK*	O	Low-speed clock output. This function is allocated to the secondary function of the P20/P36/P65 pin.	Secondary	—
OUTCLK*	O	High-speed clock output. This function is allocated to the secondary function of the P21/P37/P66 pin.	Secondary	—
General-purpose input port				
P00 to P05*	I	General-purpose input or output ports.	Primary	Positive
P12	I			
P13	I/O			
P14	I			
General-purpose output port				
P20 to P23	O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
General-purpose input/output port				
P30 to P37*	I/O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
P40 to P47				
P50 to P57*				
P60 to P67*				
P70 to P74*				
P80 to P87				

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Table 1-2 Pin Descriptions (2/3)

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
UART				
TXD0*	O	UART0 data output pin. Allocated to the secondary function of the P43, P55 , P87 and the fourthly function of the P73.	Secondary Quaternary	Positive
RXD0*	I	UART0 data input pin. Allocated to the secondary function of the P02, P42, P54 and P86.	Secondary	Positive
TXD1*	O	UART1 data output pin. Allocated to the secondary function of the P53, P73, P85, and the fourthly function of the P43, P55.	Secondary Quaternary	Positive
RXD1*	I	UART1 data input pin. Allocated to the secondary function of the P03, P52, P72 and P84.	Secondary	Positive
I^2C bus interface				
SDA*	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40, P50, P60 and P80. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL*	I/O	I^2C clock output pin. This pin is used as the secondary function of the P41, P51, P61 and P81. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0*	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40, P44, P50, P55, P72, P80 and P84.	Tertiary	Positive
SCK0*	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41, P45, P51, P56, P73, P81 and P85.	Tertiary	—
SOUT0*	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42, P46, P52, P57, P74, P82 and P86.	Tertiary	Positive
PWM				
PWM4*	O	PWM4 output pin. Allocated to the tertiary function of the P34, P43, P64, and P87.	Tertiary	Positive
PWM5*	O	PWM5 output pin. Allocated to the tertiary function of the P35, P47, P65, and P83.	Tertiary	Positive
PWM6*	O	PWM6 output pin. Allocated to the tertiary function of the P53, P66, P70 and fourthly function of the P22 and P60.	Tertiary Quaternary	Positive
PWM7*	O	PWM7 output pin. Allocated to the tertiary function of the P71 and fouthly function of the P23, P57, and P61.	Tertiary Quaternary	Positive
PW45EV0 PW45EV1	I	Control start /stop/clear for PWM4 and PWM5. Allocated to the primary function of the P00, P30, P32 and P62.	Primary	—
PW67EV0 PW67EV1	I	Control start /stop/clear pin for PWM6 and PWM7. Allocated to the primary function of the P01, P31, P33, and P63.	Primary	—
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Table 1-2 Pin Descriptions (3/3)

Pin name	I/O	Description	Primary/ Secondary	Logic
External interrupt				
EXI0～7*	I	External maskable interrupt input pins. The interrupt is enabled and interrupt edge is selectable by the software for each bit. Allocated to the primary function of the P00 to P05 and P30 to P31.	Primary	Positive/ Negative
Timer				
T16CK0	I	External clock input pin for 16bit timer 8, timer A and PWM6. Allocated to the primary function of the P46 pin.	Primary	—
T16CK1	I	External clock input pin for 16bit timer 9, timer B and PWM7. Allocated to the primary function of the P47 pin.	Primary	—
TMHAOUT	O	16bit timer A output pin. Allocated to the tertiary function of the P22 andn P60.	Tertiary	Positive
TMHBOUT	O	16bit timer B output pin. Allocated to the tertiary function of the P23 and P61.	Tertiary	Positive
LED drive				
LED0 to LED3	O	Pins for LED driving. Allocated to the primary function of the P20 to P23 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0 to AIN11	I	Analog inputs to Ch0–Ch11 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P35 and P42 to P47 pins.	—	—
Analog Comparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the P41 pin.	—	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the P40 pin.	—	—

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

1.3.4 Handling of Unused Pins

Table 1-3 shows methods of terminating the unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	open
P14/TEST0	open
TEST1_N	open
V_{REF}	Connect to V_{DD}
P00 to P05*	Connect V_{DD} or V_{SS}
P12	Connect V_{DD} or V_{SS}
P13	open
P20 to P23	open
P30 to P37*	open
P40 to P47	open
P50 to P57*	open
P60 to P67*	open
P70 to P74*	open
P80 to P87	open

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

Chapter 2 CPU and Memory Space

2 CPU and Memory Space

2.1 General Description

This LSI includes 16-bit CPU nX-U16/100 and the memory model is SMALL model.
For details of the CPU nX-U16/100, see “nX-U16/100 Core Instruction Manual”.

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 4-bit Code Segment Register (CSR) and 16-bit Program Counter (PC).
The ROM window area data has a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of one segment. (8-Kword) capacity.
Figure 2-1 shows the configuration of ML620Q151A/ML620Q154A/ML620Q157A program memory space (32-Kbyte).
Figure 2-2 shows the configuration of ML620Q152A/ML620Q155A/ML620Q158A program memory space (48-Kbyte).
Figure 2-3 shows the configuration of ML620Q153A/ML620Q156A/ML620Q159A program memory space (64-Kbyte).

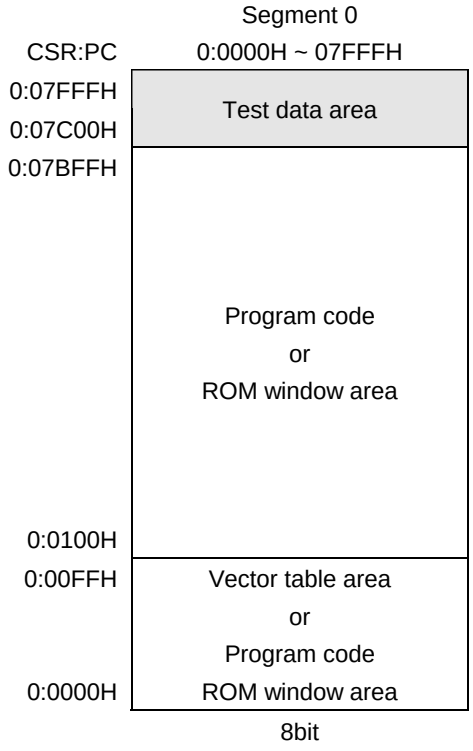


Figure 2-1 Configuration of ML620Q151A/ML620Q154A/ML620Q157A Program Memory Space (32-Kbyte)

Note:
- The 1024 bytes (512 words) test data area from 0:7C00H to 0:7FFFH cannot be used as a program code area. 0:7C00H to 0:7DFFH is rewritable and erasable. 0:7E00H to 0:7FFFH is not rewritable and not erasable. Ensure to write “0FFH” to the rewritable area 0:7C00H to 0:7DFFH. If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code cannot be guaranteed.
- Specify "0FFH" (BRK instruction) to unused are in the program memory space for failsafe purpose.

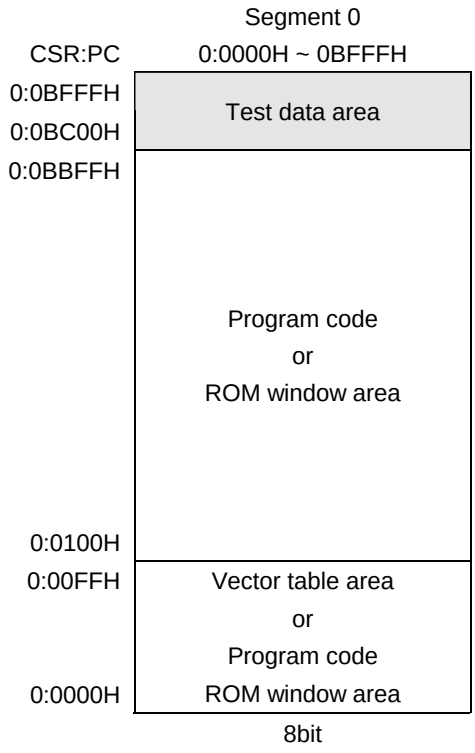


Figure 2-2 Configuration of ML620Q152A/ML620Q155A/ML620Q158A Program Memory Space (48-Kbyte)

Note:

- The 1024 bytes (512 words) test data area from 0:BC00H to 0:BFFFH cannot be used as a program code area. 0:BC00H to 0:BDFFH is rewritable and erasable. 0:BE00H to 0:BFFFH is not rewritable and not erasable. Ensure to write “0FFH” to the rewritable area 0:BC00H to 0:BDFFH. If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code cannot be guaranteed.
- Specify "0FFH" (BRK instruction) to unused are in the program memory space for failsafe purpose.

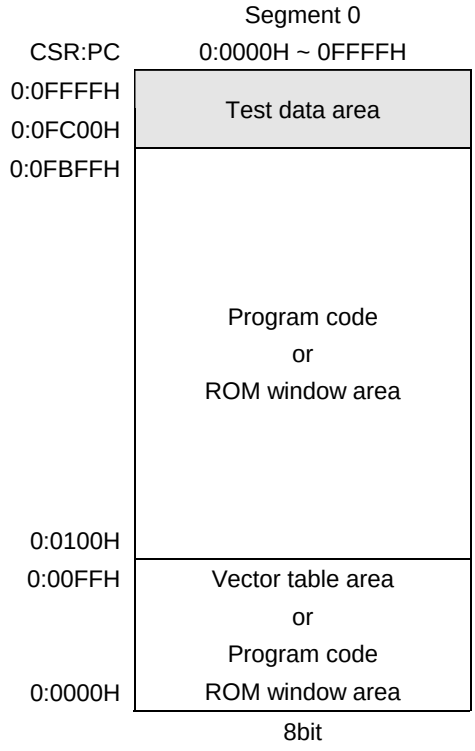


Figure 2-3 Configuration of ML620Q153A/ML620Q156A/ML620Q159A Program Memory Space (64-Kbyte)

Note:

- The 1024 bytes (512 words) test data area from 0:FC00H to 0:FFFFH cannot be used as a program code area. 0:FC00H to 0:FDFFH is rewritable and erasable. 0:FE00H to 0:FFFFH is not rewritable and not erasable. Ensure to write “0FFH” to the rewritable area 0:FC00H to 0:FDFFH. If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code cannot be guaranteed.
- Specify "0FFH" (BRK instruction) to unused are in the program memory space for failsafe purpose.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area of Segment 0, 2KByte RAM area, SFR area, and ROM reference area of segment 8.
The data memory has the 8-bit length and is specified by a 4-bit Data Segment Register (DSR) and 16-bit addressing instructions.

Figure 2-4 shows the configuration of ML620Q151A/ML620Q154A/ML620Q157A data memory space.
Figure 2-5 shows the configuration of ML620Q152A/ML620Q155A/ML620Q158A data memory space.
Figure 2-6 shows the configuration of ML620Q153A/ML620Q156A/ML620Q159A data memory space.

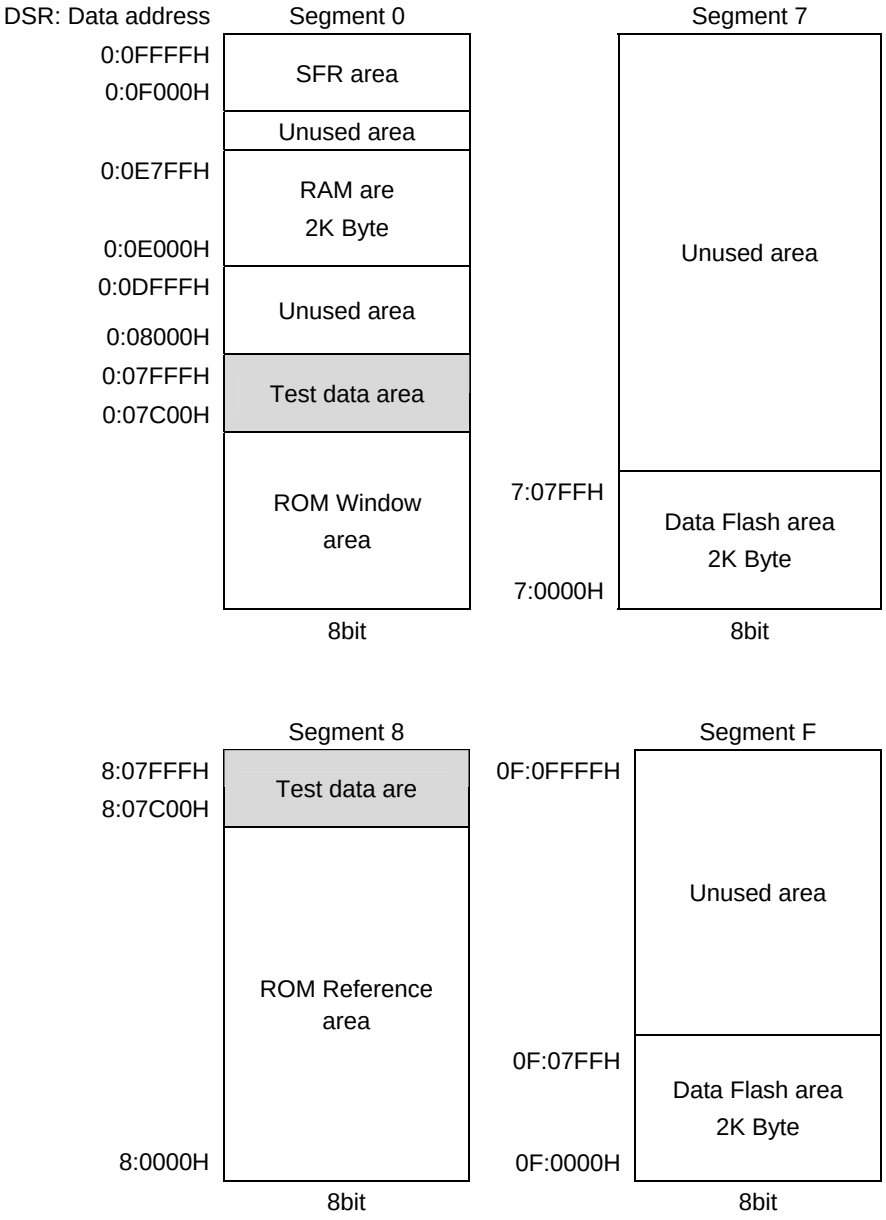


Figure 2-4 Configuration of ML620Q151A/ML620Q154A/ML620Q157A Data Memory Space

Note:
- The contents of the 2K Byte RAM area are undefined at system reset. Initialize this area by software.
- The segment 0 of program memory is readable from the ROM Reference area of segment 8.
- The segment 7 of program memory is readable from the ROM Reference area of segment F.

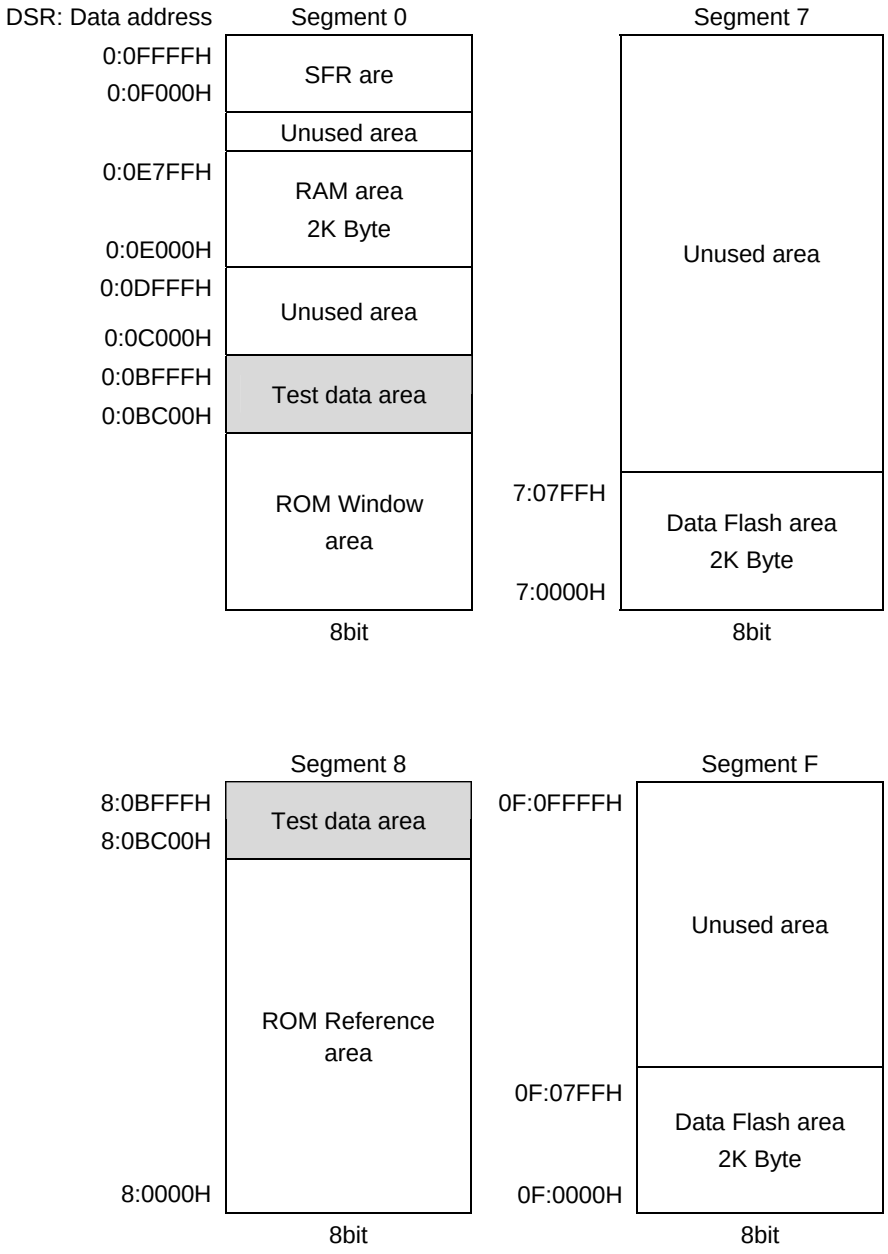


Figure 2-5 Configuration of ML620Q152A/ML620Q155A/ML620Q158A Data Memory Space

Note:

- The contents of the 2K Byte RAM area are undefined at system reset. Initialize this area by software.
- The segment 0 of program memory is readable from the ROM Reference area of segment 8.
- The segment 7 of program memory is readable from the ROM Reference area of segment F.

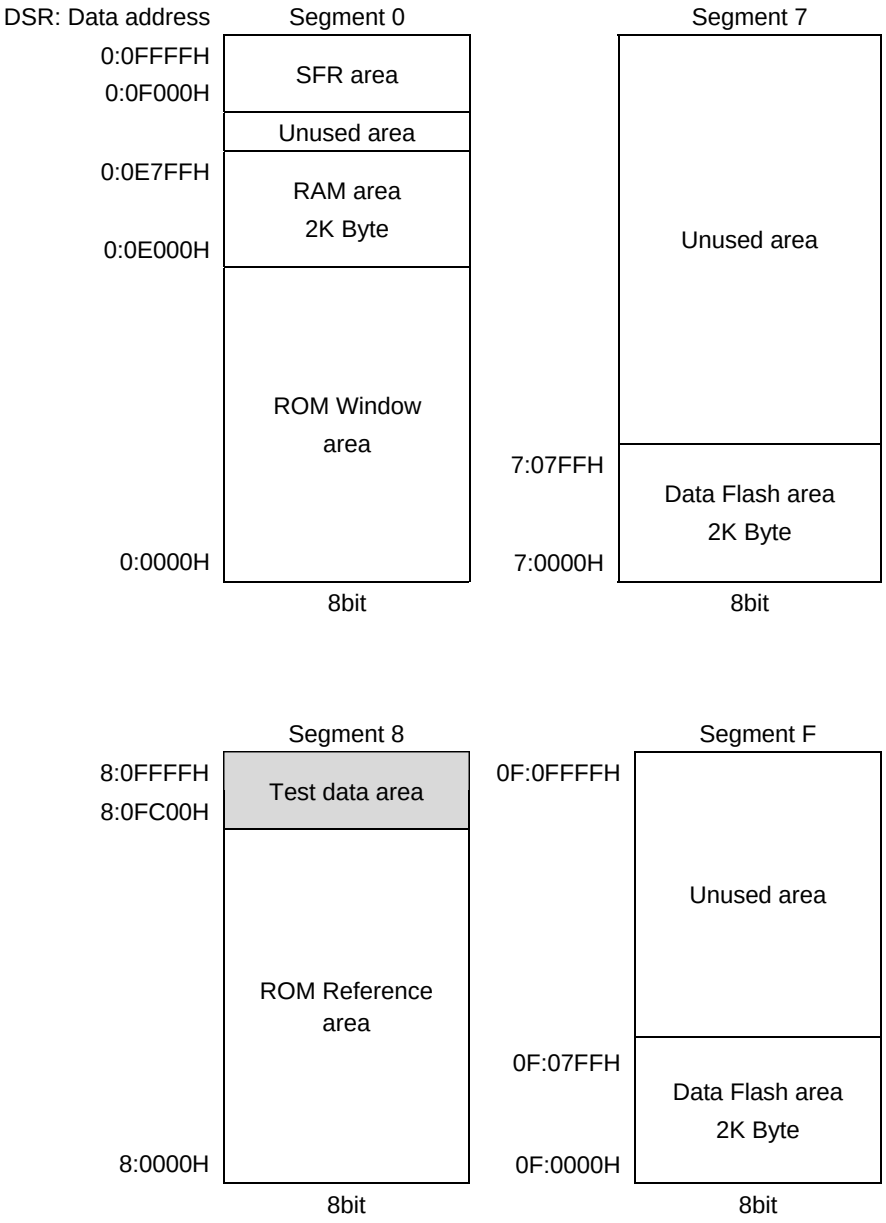


Figure 2-6 Configuration of ML620Q153A/ML620Q156A/ML620Q159A Data Memory Space

Note:

- The contents of the 2K Byte RAM area are undefined at system reset. Initialize this area by software.
- The segment 0 of program memory is readable from the ROM Reference area of segment 8.
- The segment 7 of program memory is readable from the ROM Reference area of segment F.

2.4 Instruction Length

The length of an instruction is 16 bits.

2.5 Data Type

The data types supported include byte (8 bits) and word (16 bits).

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) to retain a data segment.
For details of DSR, see “nX-U16/100 Core Instruction Manual”.

[Description of Bits]

- **DSR3-DSR0** (bits 3 to 0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (Initial value)
0	0	0	1	Prohibited
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	Data segment 7
1	0	0	0	Data segment 8
1	0	0	1	Prohibited
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	Data segment F

Chapter 3 Reset Function

3 Reset Function

3.1 General Description

This LSI has the five reset functions. If any of the four reset conditions is satisfied, this LSI enters system reset mode.

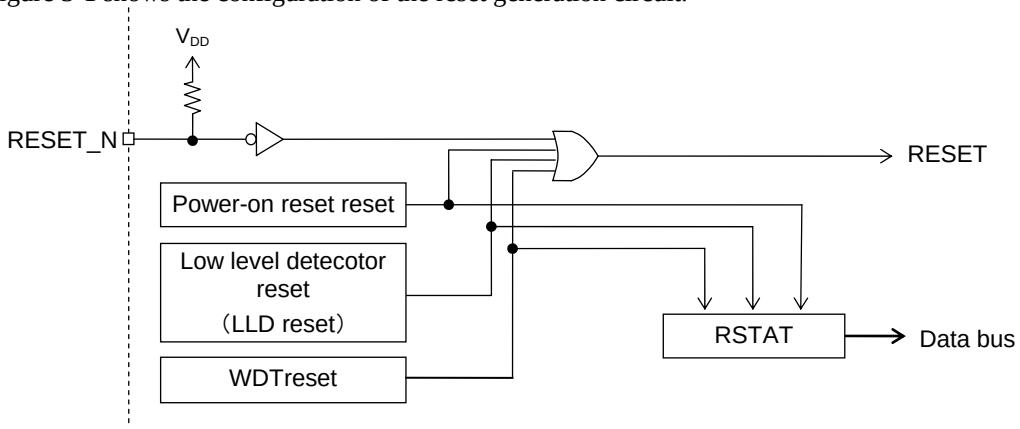
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by Low Level Detector(LLD)
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESER_N pin has an internal pull-up resistor
- 125 ms, 500ms, 2 sec, or 8 sec can be selected as the watchdog timer (WDT) overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT:Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00CH	Reset status register	RSTAT	—	R/W	8	—

3.2.2 Reset Status Register (RSTAT)

Address: 0F00CH
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	RSTR	—	LLDR	—	WDTR	—	POR
R/W	R	R/W	R	R/W	R	R/W	R	R/W
Initial value	0	x	0	0	0	0	0	1

*)The initial value depends on the reset factor

RSTAT is a special function register (SFR) that indicates the causes set to the system reset mode.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to ”1”. When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the each reset cause flag of RSTAT to “0”.

[Description of Bits]

- **PSTR** (bit 6)
  The PSTR bit is a flag that indicates that the RESET_N pin reset is generated. This bit is set to “1” when the RESET_N pin reset is generated.

RSTR	Description
0	RESET_N pin reset not occurred
1	RESET_N pin reset occurred

- **LLDR** (bit 4)
  The LLDR is a flag that indicates that the Low Level Detector reset is generated. This bit is set to “1” when the reset by overflow of the Lowe Level Detector is generated. Also, when the power is turned on is undefind.

LLDR	Description
0	Low Level Detector reset not occurred
1	Low Level Detector reset occurred

- **WDTR** (bit 2)
  The WSDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to “1” when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to “1” when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

3.3 Description of Operation

3.3.1 Operation of System Reset Mode

System reset has the highest priority among all processings and any other processing will be cancelled.
The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by Low Level Detector(LLD)
- Software reset by execution of the BRK instruction

In system reset mode, the following processing is performed.

(1) The power circuit is initialized. However, it is not initialized by the reset by the BRK instruction execution. For the details of the power circuit, refer to Chapter 27, “Power Circuit”.
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A “Registers” for the initial values of the SFRs.
(3) CPU is initialized.
- All the registers in CPU are initialized.
- The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
- The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEVEL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see “nX-U16/100 Core Instruction Manual”.

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 4 MCU Control Function

4 MCU Control Function

4.1 General Description

The operating states of this LSI are classified into the following 4 modes including system reset mode:

(1) System reset mode
(2) Program run mode
(3) HALT mode
(4) STOP mode

For the System reset mode, see Chapter 3, "Reset Function".
Also, the LSI has a block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies) to make even more reducing the current consumption.

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused function blocks (reset registers and stop clock supplies)

4.1.2 Configuration

Figure 4-1 shows an operating state transition diagram.

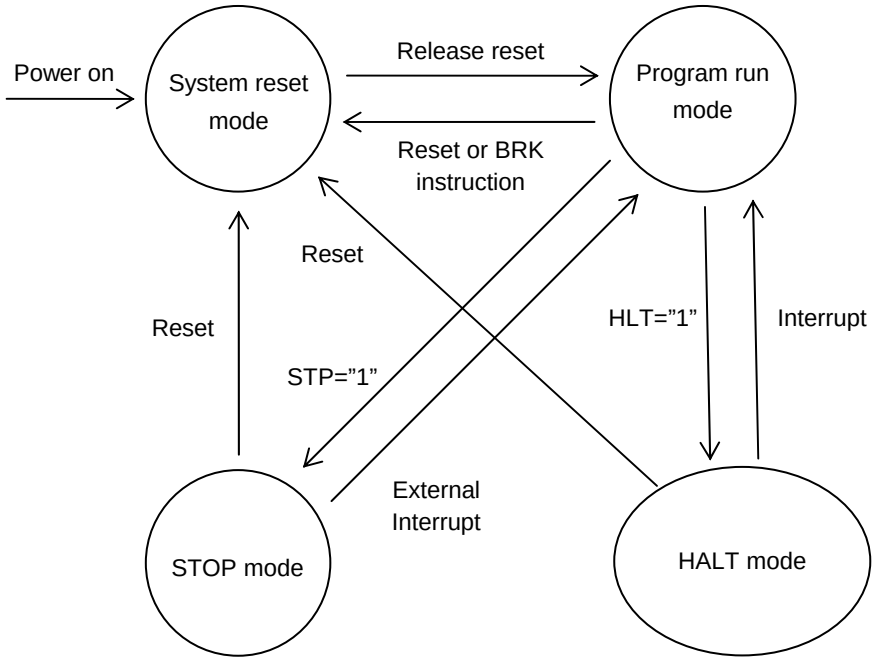


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	-	W	8	-
0F009H	Standby control register	SBYCON	-	W	8	00H
0F068H	Block control register 0	BLKCON0	-	R/W	8	00H
0F06AH	Block control register 2	BLKCON2	-	R/W	8	00H
0F06BH	Block control register 3	BLKCON3	-	R/W	8	00H
0F06CH	Block control register 4	BLKCON4	-	R/W	8	00H
0F06EH	Block control register 6	BLKCON6	-	R/W	8	00H
0F06FH	Block control register 7	BLKCON7	-	R/W	8	04H

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: -(Undefined)

	7	6	5	4	3	2	1	0
STPACP	-	-	-	-	-	-	-	-
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, “00H” is read.
When data is written to STPACP in the order of “5nH” and “0AnH” (where n is 0 to 0FH), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to “1” in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes “5nH” to STPACP and the instruction that writes “0AnH”, the stop code acceptor is enabled after “0AnH” is written. Note that, if data other than “0AnH” is written to STPACP after “5nH” is written, the “5nH” writing process becomes invalid and “5nH” should be written again.
During a system reset, the stop code acceptor is disabled.

[Note]
- The STOP code acceptor cannot be enabled on the condition that any interrupt enable flag and the corresponding interrupt request flag are both “1” (for example, an interrupt request occurs when the MIE flag is ”0”).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	-	-	-	-	HLTH	DHLT	STP	HLT
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control the operation mode of MCU.

Description of Bits

- **HLT** (bit 0)
  The HLT bit is used for setting the HALT mode. When the HLT bit is set to "1", the mode is changed to the HALT mode. Writing "0" to the HLT bit does not change the mode to the HALT mode.

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1", the mode is changed to the STOP mode. Writing "0" to the STP bit does not change the mode to the STOP mode.
  Writing to the STP bit should be performed when the stop code acceptor is enabled by using STPACP.
  If writing to the STP bit is performed when the stop code acceptor is disabled, the writing becomes invalid.

STP	**HLT**	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Setting prohibited

[Note]
•The mode is not changed to the STOP mode or HALT mode on the condition that any interrupt enable flag and the corresponding interrupt request flag are both "1" (for example, an interrupt request occurs when the MIE flag is "0").
•When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U16/100 core is "0", the STOP mode or HALT mode is simply released and interrupt processing is not performed. For details of PSW, see "nX-U16/100 Core Instruction Manual".

4.2.4 Block Control Register 0 (BLKCON0)

Address: 0F068H
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON0	-	-	-	-	-	-	DTM1	DTM0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON0 is a special function register (SFR) to control each block operation.

Description of Bits

- **DTM1** (bits 1)

DTM1	Description
0	Enable operating the timer 1 (initial value)
1	Disable operating the timer 1

- **DTM0** (bits 0)

DTM0	Description
0	Enable operating the timer 0 (initial value)
1	Disable operating the timer 0

[Note]
• When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).
• For more detail about the timer operation, see Chapter 8, "8bit Timer".

4.2.5 Block Control Register 2 (BLKCON2)

Address: 0F06AH
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C0	-	-	-	DUA1	DUA0	-	DSIO0
R/W	R/W	R	R	R	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) to control each block operation.

Description of Bits

- **DI2C0** (bits 7)
  The DI2C0 bit is used to control the I^2C bus interface operation.

DI2C0	Description
0	Enable operating the I^2C bus interface (initial value)
1	Disable operating the I^2C bus interface

- **DUA1** (bits 3)
  The DUA1 bit is used to control the UART1 operation.

DUA1	Description
0	Enable operating UART1 (initial value)
1	Disable operating UART1

- **DUA0** (bits 2)
  The DUA0 bit is used to control the UART0 operation.

DUA0	Description
0	Enable operating UART0 (initial value)
1	Disable operating UART0

- **DSIO0** (bit 0)
  The DSIO0 bit is used to control the operation of the synchronous serial port operation.

DSIO0	Description
0	Enable operating the synchronous serial port 0 (initial value)
1	Disable operating the synchronous serial port 0

[Note]
- When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).
- For more detail about the I^2C operation, see Chapter 14, " I^2C Bus Interface".
- For more detail about the UART operation, see Chapter 13, "UART".
- For more detail about the SSIO operation, see Chapter 12, "Synchronous Serial Port (SSIO)".

4.2.6 Block Control Register 3 (BLKCON3)

Address: 0F06BH(BLKCON3)
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON3	-	DCMP	-	-	-	-	-	-
R/W	R	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

BLKCON3 is a special function register (SFR) to control each block operation.

Description of Bits

- **DCMP** (bit 6)
  The DCMP bit is used to control the operation of the analogue comparator 0.

DCMP	Description
0	Enable operating the analog comparator (initial value)
1	Disable operating the analog comparator

[Note]
• When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).
• For more detail about the comparator operation, see Chapter 25, " Analog Comparator".

4.2.7 Block Control Register 4 (BLKCON4)

Address: 0F06CH(BLKCON4)
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	-	-	-	-	-	-	-	DSAD
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) to control each block operation.

Description of Bits

- **DSAD** (bit 0)
  The DSAD bit is used to control the successive approximation type (SA type) A/D converter operation.

DSAD	Description
0	Enable operating the SA type A/D converter (initial value)
1	Disable operating the SA type A/D converter

[Note]

• When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).

• For more detail about the SA type A/D converter operation, see Chapter 24, " Successive approximation type A/D converter".

4.2.8 Block Control Register 6 (BLKCON6)

Address: 0F06EH(BLKCON6)
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON6	-	-	-	-	DTMB	DTMA	DTM9	DTM8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON6 is a special function register (SFR) to control each block operation.

Description of Bits

- **DTMB** (bit 3)
  The DTMB bit is used to control the timer B.

DTMB	Description
0	Enable operating the timer B (initial value)
1	Disable operating the timer B

- **DTMA** (bit 2)
  The DTMA bit is used to control the timer A.

DTMA	Description
0	Enable operating the timer A (initial value)
1	Disable operating the timer A

- **DTM9** (bit 1)
  The DTM9 bit is used to control the timer 9.

DTM9	Description
0	Enable operating the timer 9 (initial value)
1	Disable operating the timer 9

- **DTM8** (bit 0)
  The DTM8 bit is used to control the timer 8.

DTM8	Description
0	Enable operating the timer 8 (initial value)
1	Disable operating the timer 8

[Note]

• When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).

• For more detail about the timer B to timer 8, see Chapter 9, " 16bit Timer".

4.2.9 Block Control Register 7 (BLKCON7)

Address: 0F06FH(BLKCON7)
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON7	-	-	-	-	DPW7	DPW6	DPW5	DPW4
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON7 is a special function register (SFR) to control each block operation.

Description of Bits

- **DPW7** (bit 3)
  The DPW7 bit is used to control the PWM7.

DPW7	Description
0	Enable operating the PWM7 (initial value)
1	Disable operating the PWM7

- **DPW6** (bit 2)
  The DPW6 bit is used to control the PWM6.

DPW6	Description
0	Enable operating the PWM6 (initial value)
1	Disable operating the PWM6

- **DPW5** (bit 1)
  The DPW5 bit is used to control the PWM5.

DPW5	Description
0	Enable operating the PWM5 (initial value)
1	Disable operating the PWM5

- **DPW4** (bit 0)
  The DPW4 bit is used to control the PWM4.

DPW4	Description
0	Enable operating the PWM4 (initial value)
1	Disable operating the PWM4

[Note]

• When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).

• For more detail about the timer PWM7 to PWM4, see Chapter 11, " PWM".

4.3 Description of Operation

4.3.1 Program Operating Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, low-speed oscillation stop detect reset, WDT overflow reset, or RESET_N pin reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2 HALT Mode

During the HALT mode, the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the mode changes to the HALT mode.
When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE1 to IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK), the HALT mode is released, and the mode returns to the program run mode.
Figure 4-2 shows the operation waveforms in the HALT mode.

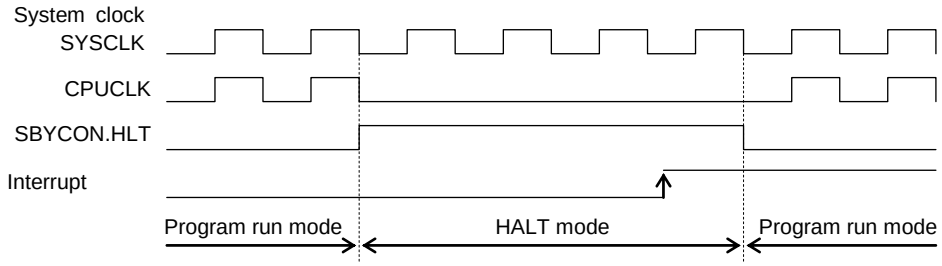


Figure 4-2 Operation Waveforms in HALT Mode

[Note]
• Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3 STOP Mode

During the STOP mode, the low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by successively writing "5nH" and "0AnH" (where n is 0 to 0FH) to the stop code acceptor (STPACP) and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the STOP code acceptor is disabled.
When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 Stop mode when the CPU runs with low-speed clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", and the low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before entering the Stopped state, high-speed oscillation does not start.

After the interrupt request occurs and counting the low-speed clock, , the STOP mode is released to go back to the program run mode and the low-speed clock (LSCLK) restarts supply to the peripheral circuits. If the high-speed clock already started oscillation at this time, the high-speed clocks (OSCLK and HSCLK) also restart supply to the peripheral circuits. In the case of that the low-speed crystal oscillation is selected by Code-Option, the low-speed clock (LSCLK) can be changed from the internal RC oscillation clock to the low-speed crystal oscillation clock after waiting for low-speed oscillation start time (T_{XTL}) and the low-speed crystal oscillation stabilization time (8192-pulse count). At that time, clock backup interrupt (CKCINT) occurs. For the low-speed oscillation start time (T_{XTL}), see Appendix C "Electrical Characteristics". For CKCINT, see Chapter 5, "Interrupts". In the case of that the internal RC oscillation is selected by Code-Option, the low-speed clock (LSCLK) restarts after waiting for the internal RC oscillation stabilization time (16-pulse count).
Figure 4-3 shows the operation waveforms in STOP mode when CPU runs with the low-speed clock.

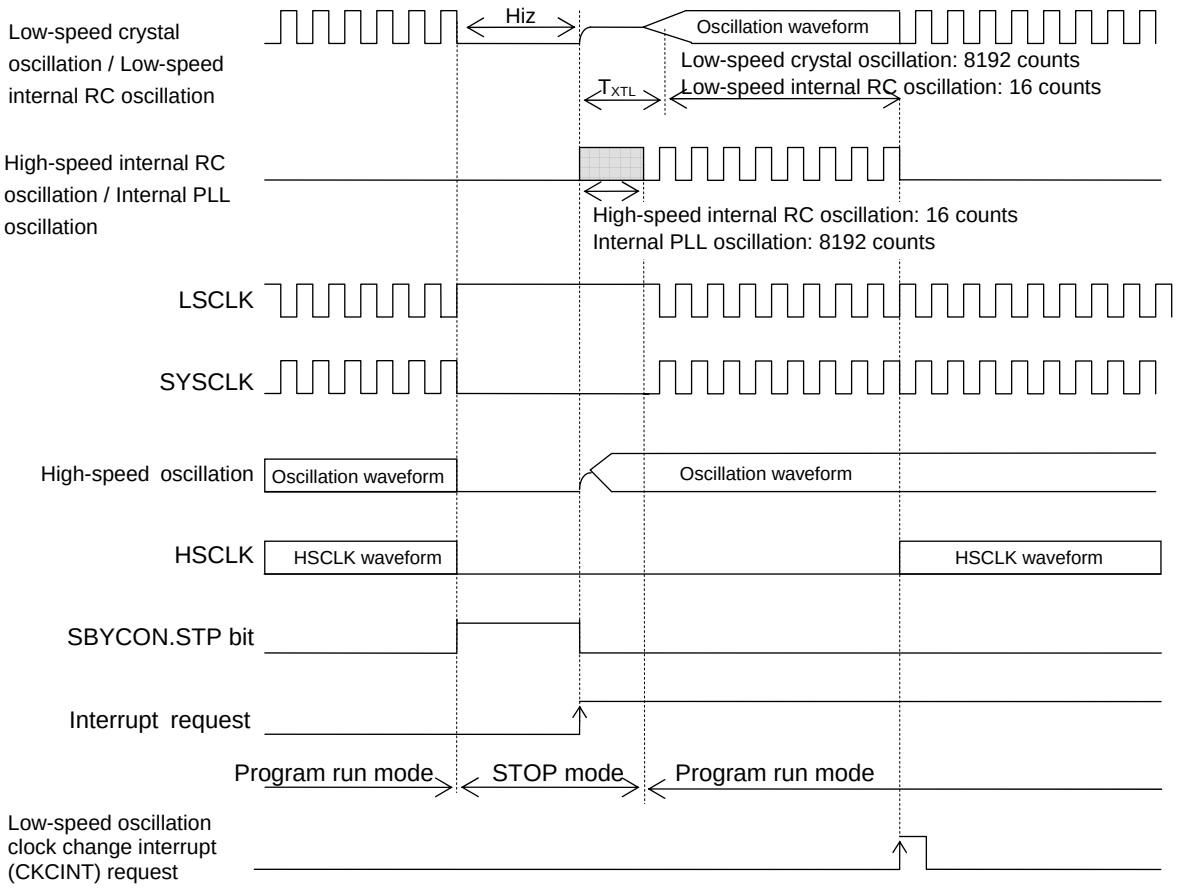


Figure 4-3 Operation Waveforms in STOP Mode When CPU runs with Low-Speed Clock

4.3.3.2 Stop mode when the CPU runs with high-speed clock

When the STP bit of SBYCON is set to "1" with the stop code acceptor enabled while the high-speed clock is operating, the mode changes to the STOP mode and the high-speed oscillation and low-speed oscillation stop.
When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", and the high-speed oscillation and low-speed oscillation restart.

When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (T_{XTH}) and the high-speed clock (OSCLK) oscillation stabilization time (4096-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
The low-speed clock (LSCLK) restarts to be supplied to the peripheral circuits after counting 128-pulse of the low-speed internal RC oscillation clock.
After waiting for the low-speed oscillation start time (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization time (8192 count), the low-speed clock (LSCLK) is changed from the low-speed internal RC oscillation clock to the low-speed crystal oscillation clock. At that time, clock backup interrupt (CKCINT) occurs.
For the high-speed oscillation start time (T_{XTH}) and low-speed oscillation start time (T_{XTL}), see the "Electrical Characteristics" Section in Appendix C. For CKCINT, see Chapter 5, "Interrupts".
Figure 4-4 shows the operation waveforms in STOP mode when CPU runs with the high-speed clock.

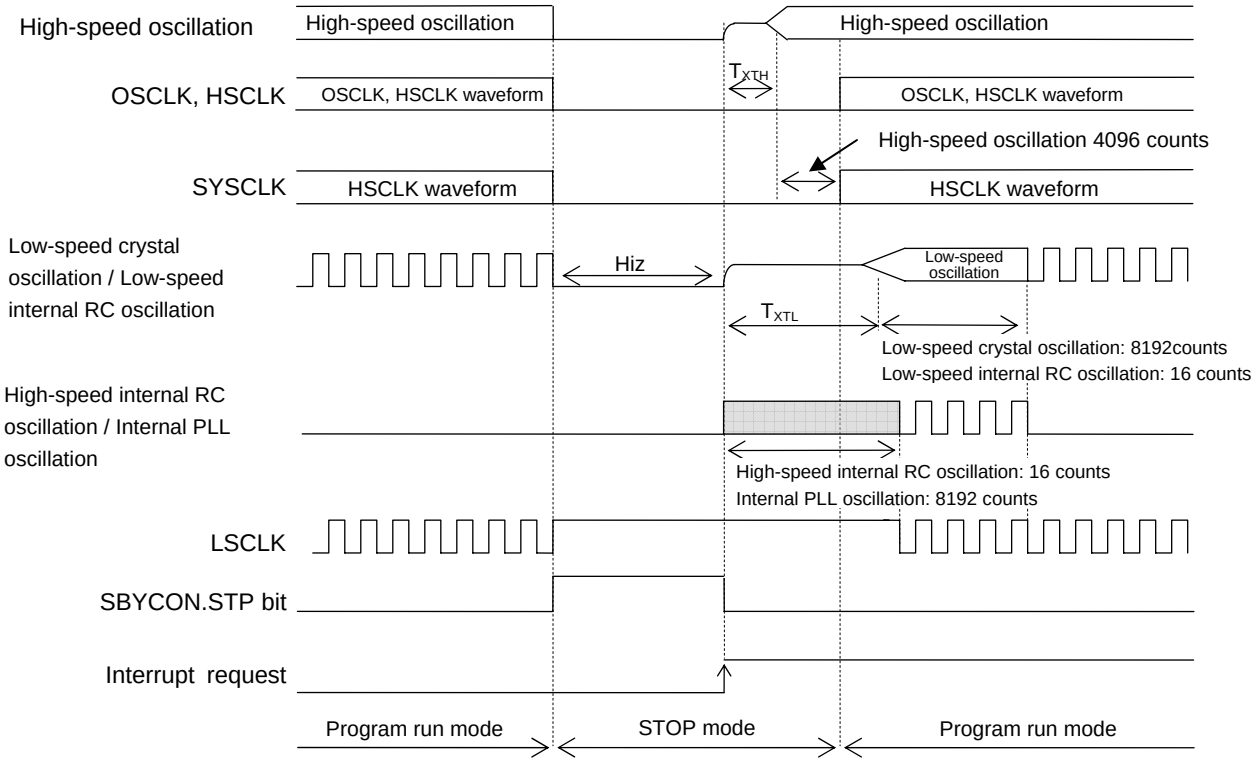


Figure 4-4 Operation Waveforms in STOP Mode When CPU runs with High-Speed Clock

[Note]
•The STOP mode is entered two cycles after the instruction that sets the STP bit to "1" and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to "1".

4.3.3.3 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP or HALT mode depends on the condition of interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE3), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U16/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from the STOP/HALT/DEEP-HALT/HALT-H mode.

Table 4-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	-	0	Not returned from STOP/HALT mode.
3	*	-	1	After the mode is returned from the STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0,1,2	*	-	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT/DEEP-HALT/HALT-H mode
*	*	*	0	Not returned from STOP/HALT/DEEP-HALT/HALT-H mode.
*	*	0	1	
*	0	1	1	After the mode is returned from the STOP/HALT/DEEP-HALT/HALT-H mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT/DHLT/HLTH bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0,1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

[Note]
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither non-maskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.4 Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.
For each block control register, the initial value of each flag is “0”, meaning the operation of each block is enabled. When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to “1”, the writing to all registers in the applicable block becomes invalid. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to “0”, (enable operation).

BLKCON0, 6 register: Controls (enables/disables) the circuit operation of timers.
BLKCON2 register: Controls (enables/disables) the circuit operation of I2C, UART and SSIO.
BLKCON3 register: Controls (enables/disables) the circuit operation of analog comparator.
BLKCON4 register: Controls (enables/disables) the circuit operation of successive approximation type A/D converter.
BLKCON7 register: Controls (enables/disables) the circuit operation of PWMs.

[Note]
- •When certain bits of block control registers are set to ”1”, corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.
- •See each chapter for detail about the operation of each block and relevant notes.

Chapter 5 Interrupts

5 Interrupt

5.1 General Description

This LSI has external interrupts, internal interrupts, and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 7, "Time Base Counter"
Chapter 8, "8-bit Timer"
Chapter 9, "16-bit Timer"
Chapter 10, "Watchdog Timer"
Chapter 11, "PWM"
Chapter 12, "Synchronous Serial Port"
Chapter 13, "UART"
Chapter 14, "I^2C Bus Interface"
Chapter 15, "Port 0"
Chapter 16, "Port 1"
Chapter 17, "Port 2"
Chapter 18, "Port 3"
Chapter 19, "Port 4"
Chapter 20, "Port 5"
Chapter 21, "Port 6"
Chapter 22, "Port 7"
Chapter 23, "Port 8"
Chapter 24, "Successive Approximation Type A/D Converter"
Chapter 25, "Analogue Comparator"
Chapter 26, "LLD Circuit"

5.1.1 Features

- Non-maskable interrupt source: 2 (Internal sources: 2)
- Maskable interrupts (See the table below)

Product	Number of interrupt sources
ML620Q151A/ML620Q152A/ML620Q153A	27 sources (Internal sources: 20, External sources: 7)
ML620Q154A/ML620Q155A/ML620Q156A	28 sources (Internal sources: 20, External sources: 8)
ML620Q157A/ML620Q158A/ML620Q159A	28 sources (Internal sources: 20, External sources: 8)

- Software interrupt (SWI): maximum 64 sources
- External interrupts allow edge selection and sampling selection (see Chapter 15, "Port 0")
- Maskable interrupts allow selection from four interrupt levels for each interrupt source
- The occurrence of interrupts with a specified interrupt level value or less can be masked

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F010H	Interrupt enable register 0	IE0	-	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	-	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	-	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	-	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	-	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	-	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	-	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	-	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	-	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	-	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	-	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	-	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	-	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	-	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	-	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	-	R/W	8	00H
0F020H	Interrupt level control enable register	ILENL	ILEN	R/W	8/16	00H
0F021H	Reserved register	-		-	8	00H
0F022H	Current interrupt request level register	CILL	CIL	R/W	8/16	00H
0F023H	Reserved register	-		-	8	00H
0F024H	Reserved register	-	-	-	-	-
0F025H	Interrupt level control register 01	ILC01	-	R/W	8	00H
0F026H	Interrupt level control register 10	ILC10	ILC1W	R/W	8/16	00H
0F027H	Interrupt level control register 11	ILC11		R/W	8	00H
0F028H	Interrupt level control register 20	ILC20	ILC2W	R/W	8/16	00H
0F029H	Interrupt level control register 21	ILC21		R/W	8	00H
0F02AH	Interrupt level control register 30	ILC30	ILC3W	R/W	8/16	00H
0F02BH	Interrupt level control register 31	ILC31		R/W	8	00H
0F02CH	Interrupt level control register 40	ILC40	ILC4W	R/W	8/16	00H
0F02DH	Reserved register	-		-	8	00H
0F02EH	Reserved register	-	ILC5W	-	8/16	00H
0F02FH	Interrupt level control register 51	ILC51		R/W	8	00H
0F030H	Interrupt level control register 60	ILC60	ILC6W	R/W	8/16	00H
0F031H	Interrupt level control register 61	ILC61		R/W	8	00H
0F032H	Interrupt level control register 70	ILC70	ILC7W	R/W	8/16	00H
0F033H	Reserved register	-		-	8	00H

[Note]
Writing to a reserved register is disabled. "0" is read when reading the register.

5.2.2 Interrupt Enable Register 0 (IE0)

Address: 0F010H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE0	-	ELLD	-	-	-	-	-	-
R/W	R	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE0 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE0 is not reset.

Description of bits

- **ELLD** (bit 6)
  ELLD is the enable flag for the LLD interrupt (LLDINT).

ELLD	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	EP31	EP30	EP05	EP04	EP03	EP02	EP01	EP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

Description of bits

- **EP31** (bit 7)
  EP31 is the enable flag for the input port P31 pin interrupt (P31INT).

EP31	Description
0	Disabled (initial value)
1	Enabled

- **EP30** (bit 6)
  EP30 is the enable flag for the input port P30 pin interrupt (P30INT).

EP30	Description
0	Disabled (initial value)
1	Enabled

- **EP05** (bit 5)
  EP05 is the enable flag for the input port P05 pin interrupt (P05INT).

EP05	Description
0	Disabled (initial value)
1	Enabled

- **EP04** (bit 4)
  EP04 is the enable flag for the input port P04 pin interrupt (P04INT).

EP04	Description
0	Disabled (initial value)
1	Enabled

- **EP03** (bit 3)
  EP03 is the enable flag for the input port P03 pin interrupt (P03INT).

EP03	Description
0	Disabled (initial value)
1	Enabled

- **EP02** (bit 2)
  EP02 is the enable flag for the input port P02 pin interrupt (P02INT).

EP02	Description
0	Disabled (initial value)
1	Enabled

- **EP01** (bit 1)
  EP01 is the enable flag for the input port P01 pin interrupt (P01INT).

EP01	Description
0	Disabled (initial value)
1	Enabled

- **EP00** (bit 0)
  EP00 is the enable flag for the input port P00 pin interrupt (P00INT).

EP00	Description
0	Disabled (initial value)
1	Enabled

[Note]
EP05 is not included in ML620Q151/ML620Q152/ML620Q153.

5.2.4 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	EI2C0	-	-	-	-	ESAD	-	ESIO0
R/W	R/W	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

Description of bits

- **EI2C0** (bit 7)
  EI2C0 is the enable flag for the I^2C bus 0 interrupt (I2C0INT).

EI2C0	Description
0	Disabled (initial value)
1	Enabled

- **ESAD** (bit 2)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

- **ESIO0** (bit 0)
  ESIO0 is the enable flag for the synchronous serial port 0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	-	ECMP0	-	-	ETM9	ETM8	ETM1	ETM0
R/W	R	R/W	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

Description of bits

- **ECMP0** (bit 6)
  ECMP0 is the enable flag for the comparator 0 interrupt (CMP0INT).

ECMP0	Description
0	Disabled (initial value)
1	Enabled

- **ETM9** (bit 3)
  ETM9 is the enable flag for the timer 9 interrupt (TM9INT).

ETM9	Description
0	Disabled (initial value)
1	Enabled

- **ETM8** (bit 2)
  ETM8 is the enable flag for the timer 8 interrupt (TM8INT).

ETM8	Description
0	Disabled (initial value)
1	Enabled

- **ETM1** (bit 1)
  ETM1 is the enable flag for the timer 1 interrupt (TM1INT).

ETM1	Description
0	Disabled (initial value)
1	Enabled

- **ETM0** (bit 0)
  ETM0 is the enable flag for the timer 0 interrupt (TM0INT).

ETM0	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	-	-	-	-	-	-	EUA1	EUA0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

Description of bits

- **EUA1** (bit 1)
  EUA1 is the enable flag for the UART1 interrupt (UA1INT).

EUA1	Description
0	Disabled (initial value)
1	Enabled

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

5.2.7 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	-	-	ETMB	ETMA	-	-	-	-
R/W	R	R	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

Description of bits

- **ETMB** (bit 5)
  ETMB is the enable flag for the timer B interrupt (TMBINT).

ETMB	Description
0	Disabled (initial value)
1	Enabled

- **ETMA** (bit 4)
  ETMA is the enable flag for the timer A interrupt (TMAINT).

ETMA	Description
0	Disabled (initial value)
1	Enabled

5.2.8 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	ELTBC1	-	ELTBC0	-	EPW7	EPW6	EPW5	EPW4
R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

Description of bits

- **ELTBC1** (bit 7)
  ELTBC1 is the enable flag for the time base counter 1 interrupt (LTBC1INT).

ELTBC1	Description
0	Disabled (initial value)
1	Enabled

- **ELTBC0** (bit 5)
  ELTBC0 is the enable flag for the time base counter 0 interrupt (LTBC0INT).

ELTBC0	Description
0	Disabled (initial value)
1	Enabled

- **EPW7** (bit 3)
  EPW7 is the enable flag for the PWM7 interrupt (PW7INT).

EPW7	Description
0	Disabled (initial value)
1	Enabled

- **EPW6** (bit 2)
  EPW6 is the enable flag for the PWM6 interrupt (PW6INT).

EPW6	Description
0	Disabled (initial value)
1	Enabled

- **EPW5** (bit 1)
  EPW5 is the enable flag for the PWM5 interrupt (PW5INT).

EPW5	Description
0	Disabled (initial value)
1	Enabled

- **EPW4** (bit 0)
  EPW4 is the enable flag for the PWM4 interrupt (PW4INT).

EPW4	Description
0	Disabled (initial value)
1	Enabled

5.2.9 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	-	-	-	-	ELTBC2	-	-	-
R/W	R	R	R	R	R/W	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

Description of bits

- **ELTBC2** (bit 3)
  ELTBC2 is the enable flag for the time base counter 2 interrupt (LTBC2INT).

ELTBC2	Description
0	Disabled (initial value)
1	Enabled

5.2.10 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	-	QLLD	-	-	-	QCKC	-	QWDT
R/W	R	R/W	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) used to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) and the clock backup interrupt (CKCINT) are non-maskable interrupts that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
The LLD interrupt (LLDINT) is a maskable interrupt. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE0) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QLLD** (bit 6)
  QLLD is the request flag for the LLD interrupt (LDDINT).

QLLD	Description
0	No request (initial value)
1	Request

- **QCKC** (bit 2)
  QCKC is the request flag for the clock backup interrupt (CKCINT).

QCKC	Description
0	No request (initial value)
1	Request

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	QP31	QP30	QP05	QP04	QP03	QP02	QP01	QP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QP31** (bit 7)
  QP31 is the request flag for the input port P31 pin interrupt (P31INT).

QP31	Description
0	No request (initial value)
1	Request

- **QP30** (bit 6)
  QP30 is the request flag for the input port P30 pin interrupt (P30INT).

QP30	Description
0	No request (initial value)
1	Request

- **QP05** (bit 5)
  QP05 is the request flag for the input port P05 pin interrupt (P05INT).

QP05	Description
0	No request (initial value)
1	Request

- **QP04** (bit 4)
  QP04 is the request flag for the input port P04 pin interrupt (P04INT).

QP04	Description
0	No request (initial value)
1	Request

- **QP03** (bit 3)
  QP03 is the request flag for the input port P03 pin interrupt (P03INT).

QP03	Description
0	No request (initial value)
1	Request

- **QP02** (bit 2)
  QP02 is the request flag for the input port P02 pin interrupt (P02INT).

QP02	Description
0	No request (initial value)
1	Request

- **QP01** (bit 1)
  QP01 is the request flag for the input port P01 pin interrupt (P01INT).

QP01	Description
0	No request (initial value)
1	Request

- **QP00** (bit 0)
  QP00 is the request flag for the input port P00 pin interrupt (P00INT).

QP00	Description
0	No request (initial value)
1	Request

[Note]
- When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.
- QP05 is not included in ML620Q151/ML620Q152/ML620Q153.

5.2.12 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	QI2C0	-	-	-	-	QSAD	-	QSIO0
R/W	R/W	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QI2C0** (bit 7)
  QI2C0 is the request flag for the I^2C bus 0 interrupt (I2C0INT).

QI2C0	Description
0	No request (initial value)
1	Request

- **QSAD** (bit 2)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT).

QSAD	Description
0	No request (initial value)
1	Request

- **QSIO0** (bit 0)
  QSIO0 is the request flag for the synchronous serial port 0 interrupt (SIO0INT).

QSIO0	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	-	QCMP0	-	-	QTM9	QTM8	QTM1	QTM0
R/W	R	R/W	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QCMP0** (bit 6)
  QCMP0 is the request flag for the compare 0 interrupt (CMP0INT).

QCMP0	Description
0	No request (initial value)
1	Request

- **QTM9** (bit 3)
  QTM9 is the request flag for the timer 9 interrupt (TM9INT).

QTM9	Description
0	No request (initial value)
1	Request

- **QTM8** (bit 2)
  QTM8 is the request flag for the timer 8 interrupt (TM8INT).

QTM8	Description
0	No request (initial value)
1	Request

- **QTM1** (bit 1)
  QTM1 is the request flag for the timer 1 interrupt (TM1INT).

QTM1	Description
0	No request (initial value)
1	Request

- **QTM0** (bit 0)
  QTM0 is the request flag for the timer 0 interrupt (TM0INT).

QTM0	Description
0	No request (initial value)
1	Request

[Note]

When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	-	-	-	-	-	-	QUA1	QUA0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QUA1** (bit 1)
  QUA1 is the request flag for the UART1 interrupt (UA1INT).

QUA1	Description
0	No request (initial value)
1	Request

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.15 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	-	-	QTMB	QTMA	-	-	-	-
R/W	R	R	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QTMB** (bit 5)
  QTMB is the request flag for the timer B interrupt (TMBINT).

QTMB	Description
0	No request (initial value)
1	Request

- **QTMA** (bit 4)
  QTMA is the request flag for the timer A interrupt (TMAINT).

QTMA	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.16 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	QLTBC1	-	QLTBC0	-	QPW7	QPW6	QPW5	QPW4
R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QLTBC1** (bit 7)
  QLTBC1 is the request flag for the time base counter 1 interrupt (LTBC1INT).

LTBC1	Description
0	No request (initial value)
1	Request

- **QLTBC0** (bit 5)
  QLTBC0 is the request flag for the time base counter 0 interrupt (LTBC0INT).

QLTBC0	Description
0	No request (initial value)
1	Request

- **QPW7** (bit 3)
  QPW7 is the request flag for the PWM7 interrupt (PW7INT).

QPW7	Description
0	No request (initial value)
1	Request

- **QPW6** (bit 2)
  QPW6 is the request flag for the PWM6 interrupt (PW6INT).

QPW6	Description
0	No request (initial value)
1	Request

- **QPW5** (bit 1)
  QPW5 is the request flag for the PWM5 interrupt (PW5INT).

QPW5	Description
0	No request (initial value)
1	Request

- **QPW4** (bit 0)
  QPW4 is the request flag for the PWM4 interrupt (PW4INT).

QPW4	Description
0	No request (initial value)
1	Request

[Note]

When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.17 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	-	-	-	-	QLTBC2	-	-	-
R/W	R	R	R	R	R/W	R	R	R
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of bits

- **QLTBC2** (bit 3)
  QLTBC2 is the request flag for the time base counter 2 interrupt (LTBC2INT).

QLTBC2	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.18 Interrupt Level Control Enable Register (ILENL)

Address: 0F020H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILENL	—	—	—	—	—	—	—	ILE
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control enable register (ILENL) is a special function register (SFR) used to control enable/disable for the interrupt level control.

Description of bits

- **ILE** (bit 0)

The ILE bit controls enable/disable for the interrupt level control.
Enable this bit setting to use the interrupt level control.
If this bit setting is disabled, do not access the CILL and ILC registers.

[Note]

A write instruction to the interrupt level control enable register (ILENL) should be executed only during the period from the reset release until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7).
Proper operation cannot be guaranteed if a write instruction to the interrupt level control enable register (ILEN or ILENL) is executed at other times.
To disable the interrupt level control function, set both the values of CILL and ILC registers to 00H.

5.2.19 Current Interrupt Request Level Register (CILL)

Address: 0F022H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CILL	CILN	–	–	–	CILM[3:0]			
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The current interrupt request level register (CILL) indicates the interrupt level of the interrupt currently being processed by the processor.
Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

Description of bits

- **CILN** (bit 7)
  Indicates that the processor is currently processing an interrupt request with the highest level. An interrupt with the highest level refers to non-maskable interrupt.

- **CILM** (bits 3-0)
  Indicates that the processor is currently processing a maskable interrupt request with the level corresponding to the bit position set to "1".

CILM[3]	CILM[2]	CILM[1]	CILM[0]
Interrupt level 4	Interrupt level 3	Interrupt level 2	Interrupt level 1

When "1" has been set in any bit position of CILL, the acceptance of interrupt requests is prohibited below the interrupt level indicated by the highest order bit position set to "1". It indicates that the processing is being done for an interrupt with the level corresponding to the bit position.
When "1"s have been set at several bit positions of CILL, it indicates that multiple interrupts are being processed.

<<Condition for setting>>
When the processor accepts an interrupt, "1" is set to the CILN bit if the interrupt request is non-maskable interrupt. If the interrupt request is maskable interrupt, "1" is set to the bit position of CILM corresponding to the level of the interrupt source.

<<Condition for clearing>>
When a write access is made, the highest order bit set to "1" is cleared. After the interrupt handler processing is completed, execute a write access once.

5.2.20 Interrupt Level Control Register 01 (ILC01)

Address: 0F025H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC01	-	-	ILC01[5:4]		-	-	-	-
R/W	R	R	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 01 (ILC01) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC01[n] (n = 5:4) and the levels is as follows:

Table 5-1 Correspondence between Values of ILC01[n] and Levels

ILC01[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 01 (ILC01) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 01 (ILC01) is executed at other times.

5.2.21 Interrupt Level Control Register 10 (ILC10)

Address: 0F026H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC10	ILC10[7:6]		ILC10[5:4]		ILC10[3:2]		ILC10[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 10 (ILC10) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC10[n] (n = 7:6, 5:4, 3:2, 1:0) and the levels is as follows:

Table 5-2 Correspondence between Values of ILC10[n] and Levels

ILC10[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 10 (ILC10) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 10 (ILC10) is executed at other times.

5.2.22 Interrupt Level Control Register 11 (ILC11)

Address: 0F027H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC11	ILC11[7:6]		ILC11[5:4]		ILC11[3:2]		ILC11[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 11 (ILC11) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC11[n] (n = 7:6, 5:4, 3:2, 1:0) and the levels is as follows:

Table 5-3 Correspondence between Values of ILC11[n] and Levels

ILC11[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 11 (ILC11) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 11 (ILC11) is executed at other times.

5.2.23 Interrupt Level Control Register 20 (ILC20)

Address: 0F028H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC20	-	-	ILC20[5:4]		-	-	ILC20[1:0]	
R/W	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 20 (ILC20) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC20[n] (n = 5:4, 1:0) and the levels is as follows:

Table 5-4 Correspondence between Values of ILC20[n] and Levels

ILC20[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 20 (ILC20) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 20 (ILC20) is executed at other times.

5.2.24 Interrupt Level Control Register 21 (ILC21)

Address: 0F029H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC21	ILC21[7:6]		-	-	-	-	-	-
R/W	R/W	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 21 (ILC21) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC21[n] (n = 7:6) and the levels is as follows:

Table 5-5 Correspondence between Values of ILC21[n] and Levels

ILC21[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 21 (ILC21) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 21 (ILC21) is executed at other times.

5.2.25 Interrupt Level Control Register 30 (ILC30)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC30	ILC30[7:6]		ILC30[5:4]		ILC30[3:2]		ILC30[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 30 (ILC05) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC30[n] (n = 7:6, 5:4, 3:2, 1:0) and the levels is as follows:

Table 5-6 Correspondence between Values of ILC30[n] and Levels

ILC30[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 30 (ILC30) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 30 (ILC30) is executed at other times.

5.2.26 Interrupt Level Control Register 31 (ILC31)

Address: 0F02BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC31	-	-	ILC31[5:4]		-	-	-	-
R/W	R	R	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 31 (ILC31) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC31[n] (n = 5:4) and the levels is as follows:

Table 5-7 Correspondence between Values of ILC31[n] and Levels

ILC31[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 31 (ILC31) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 31 (ILC31) is executed at other times.

5.2.27 Interrupt Level Control Register 40 (ILC40)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC40	-	-	-	-	ILC40[3:2]		ILC40[1:0]	
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 40 (ILC40) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC40[n] (n = 3:2, 1:0) and the levels is as follows:

Table 5-8 Correspondence between Values of ILC40[n] and Levels

ILC40[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 40 (ILC40) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 40 (ILC40) is executed at other times.

5.2.28 Interrupt Level Control Register 51 (ILC51)

Address: 0F02FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC51	-	-	-	-	ILC51[3:2]		ILC51[1:0]	
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 51 (ILC51) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC51[n] (n = 3:2, 1:0) and the levels is as follows:

Table 5-9 Correspondence between Values of ILC51[n] and Levels

ILC51[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 51 (ILC51) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 51 (ILC51) is executed at other times.

5.2.29 Interrupt Level Control Register 60 (ILC60)

Address: 0F030H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC60	ILC60[7:6]		ILC60[5:4]		ILC60[3:2]		ILC60[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 60 (ILC60) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC60[n] (n = 7:6, 5:4, 3:2, 1:0) and the levels is as follows:

Table 5-10 Correspondence between Values of ILC60[n] and Levels

ILC60[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 60 (ILC60) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 60 (ILC60) is executed at other times.

5.2.30 Interrupt Level Control Register 61 (ILC61)

Address: 0F031H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC61	ILC61[7:6]		-	-	ILC61[3:2]		-	-
R/W	R/W	R/W	R	R	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 61 (ILC61) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC61[n] (n = 7:6, 3:2) and the levels is as follows:

Table 5-11 Correspondence between Values of ILC61[n] and Levels

ILC61[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 61 (ILC61) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 61 (ILC61) is executed at other times.

5.2.31 Interrupt Level Control Register 70 (ILC70)

Address: 0F032H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
ILC70	ILC70[7:6]		-	-	-	-	-	-
R/W	R/W	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 70 (ILC70) sets the interrupt level for the specific maskable interrupt source. Access to this register is possible only when the interrupt level control is enabled by the ILENL register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

The correspondence between the values of ILC70[n] (n = 7:6) and the levels is as follows:

Table 5-12 Correspondence between Values of ILC70[n] and Levels

ILC70[n]	Level	Interrupt priority level
2'b00	1	Low
2'b01	2	↑
2'b10	3	↓
2'b11	4	High

For the correspondence with interrupt sources, refer to Table 5-13 "Interrupt Sources".

[Note]
A write instruction to the interrupt level control register 70 (ILC70) should be executed only during the period from the reset until the interrupt request signal is allowed by writing "1" to the interrupt enable register (IE1 to IE7). Proper operation cannot be guaranteed if a write instruction to the interrupt level control register 70 (ILC70) is executed at other times.

5.3 Description of Operation

With the exceptions of the watchdog timer interrupt (WDTINT) and clock backup interrupt (CKCINT), interrupt enable/disable for 28 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1 to 7). WDTINT and CKCINT are non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-13 Interrupt Sources

Interrupt source number	Register assignment			Interrupt address	Mask enabled/ disabled	Internal/ external	Interrupt source	Interrupt source symbol
	IRQ	IE	ILC					
1	IRQ0[0]	-	-	0008H	Disabled	Internal source	WDT interrupt	WDTINT
2	IRQ0[2]	-	-	000AH	Disabled		CKC interrupt	CKCINT
3	IRQ0[6]	IE0[6]	ILC01[5:4]	000CH	Enabled		LLD interrupt	LLDINT
4	IRQ1[0]	IE1[0]	ILC10[1:0]	0010H	Enabled	External pin	P00 interrupt	P00INT
5	IRQ1[1]	IE1[1]	ILC10[3:2]	0012H	Enabled		P01 interrupt	P01INT
6	IRQ1[2]	IE1[2]	ILC10[5:4]	0014H	Enabled		P02 interrupt	P02INT
7	IRQ1[3]	IE1[3]	ILC10[7:6]	0016H	Enabled		P03 interrupt	P03INT
8	IRQ1[4]	IE1[4]	ILC11[1:0]	0018H	Enabled		P04 interrupt	P04INT
9	IRQ1[5]	IE1[5]	ILC11[3:2]	001AH	Enabled		P05 interrupt	P05INT
10	IRQ1[6]	IE1[6]	ILC11[5:4]	001CH	Enabled		P30 interrupt	P30INT
11	IRQ1[7]	IE1[7]	ILC11[7:6]	001EH	Enabled		P31 interrupt	P31INT
12	IRQ2[0]	IE2[0]	ILC20[1:0]	0020H	Enabled	Internal source	SIO0 interrupt	SIO0INT
13	IRQ2[2]	IE2[2]	ILC20[5:4]	0024H	Enabled		SA-ADC interrupt	ADCINT
14	IRQ2[7]	IE2[7]	ILC21[7:6]	002EH	Enabled		I2C0 interrupt	I2C0INT
15	IRQ3[0]	IE3[0]	ILC30[1:0]	0030H	Enabled		Timer 0 interrupt	TM0INT
16	IRQ3[1]	IE3[1]	ILC30[3:2]	0032H	Enabled		Timer 1 interrupt	TM1INT
17	IRQ3[2]	IE3[2]	ILC30[5:4]	0034H	Enabled		Timer 8 interrupt	TM8INT
18	IRQ3[3]	IE3[3]	ILC30[7:6]	0036H	Enabled		Timer 9 interrupt	TM9INT
19	IRQ3[6]	IE3[6]	ILC31[5:4]	003CH	Enabled		Compare 0 interrupt	CMP0INT
20	IRQ4[0]	IE4[0]	ILC40[1:0]	0040H	Enabled		UART0 interrupt	UA0INT
21	IRQ4[1]	IE4[1]	ILC40[3:2]	0042H	Enabled		UART1 interrupt	UA1INT
22	IRQ5[4]	IE5[4]	ILC51[1:0]	0058H	Enabled		Timer A interrupt	TMAINT
23	IRQ5[5]	IE5[5]	ILC51[3:2]	005AH	Enabled		Timer B interrupt	TMBINT
24	IRQ6[0]	IE6[0]	ILC60[1:0]	0060H	Enabled		PWM4 interrupt	PWM4INT
25	IRQ6[1]	IE6[1]	ILC60[3:2]	0062H	Enabled		PWM5 interrupt	PWM5INT
26	IRQ6[2]	IE6[2]	ILC60[5:4]	0064H	Enabled		PWM6 interrupt	PWM6INT
27	IRQ6[3]	IE6[3]	ILC60[7:6]	0066H	Enabled		PWM7 interrupt	PWM7INT
28	IRQ6[5]	IE6[5]	ILC61[3:2]	006AH	Enabled		LTBC0 interrupt	LTBC0INT
29	IRQ6[7]	IE6[7]	ILC61[7:6]	006EH	Enabled		LTBC1 interrupt	LTBC1INT
30	IRQ7[3]	IE7[3]	ILC70[7:6]	0076H	Enabled		LTBC2 interrupt	LTBC2INT

[Note]

- If multiple interrupts are generated concurrently when the interrupt level control is disabled, they are processed starting from the interrupt with the highest priority level (lowest interrupt source number), and the lower- priority interrupts (higher interrupt source number) are pending.
- If multiple interrupts are generated concurrently when the interrupt level control is enabled, they are processed starting from the interrupt with the highest interrupt level and the highest priority level, and the lower- priority interrupts are pending.
- Please define vector tables for all unused interrupts for fail safe.

5.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1
(2) Transfer PSW to EPSW1
(3) Set the MIE flag to "0"
(4) Set the ELEVEL field to "1"
(5) Load the interrupt beginning address into PC

5.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2
(2) Transfer PSW to EPSW2
(3) Set the ELEVEL field to "2"
(4) Load the interrupt beginning address into PC

5.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1
(2) Transfer PSW to EPSW1
(3) Set the MIE flag to "0"
(4) Set the ELEVEL field to "1"
(5) Load the interrupt beginning address into PC

[Reference]
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U16/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine (When Interrupt Level Control Disabled)

If ILE of the interrupt level control enable register (ILENL) is set to disable the interrupt level control, notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

Status A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: Status A-1-1

```
Intrpt_A-1-1;          ; A-1-1 state
    DI                 ; Disable interrupt
    :
    :
    :
    RTI                ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: Status A-1-2

```
Intrpt_A-1-2;          ; Start
  PUSH  ELR, EPSW      ; Save ELR and EPSW at the
                         beginning
  EI                   ; Enable interrupt
  :
  :
  :
  :
  :
  POP   PC, PSW        ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: Status A-2-2

```
Intrpt_A-2-2;              ; Start
  PUSH                     ; Save ELR, EPSW, LR
ELR,EPSW,LR                at the beginning

  EI                       ; Enable interrupt
  :
  :
  :

  BL Sub_1                 ; Call subroutine Sub_1
  :
  POP   PC, PSW, LR        ; Return PC from the stack
                           ; Return PSW from the stack
                           ; Return LR from the stack
                           ; End
```

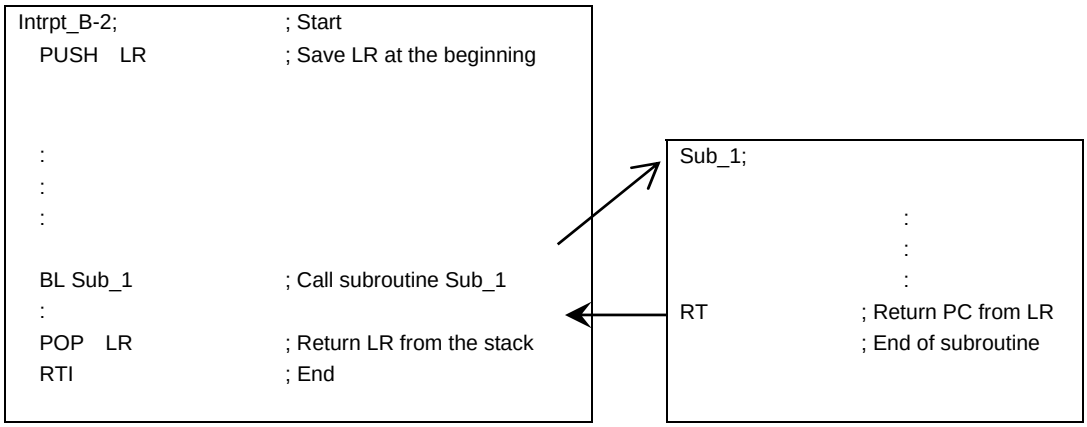
```
Sub_1;          ;
DI              ; Disable interrupt
                    :
                    :
EI              ; Enable interrupt
RT              ; Return PC from LR
                ; End of subroutine
```

Status B: Non-maskable interrupt is being processed

B-1: When a subroutine is not called
- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

B-2: When a subroutine is called
- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

Example of description: Status B-2



5.3.5 Interrupt Processing When Interrupt Level Control Enabled

①Interrupt processing

The interrupt handler carries out the following processing.

i. The following processing is made when multiple interrupts are enabled.
When a higher level interrupt request occurs, that request should be processed with priority. For this reason, the general-purpose registers are saved to memory and the EPW and EPSW registers are pushed in order to retain the processor state at return.

ii. When multiple interrupts are ready to be processed, the EI instruction is executed to enable the processor interrupt.

②Return from interrupt

The interrupt handler carries out the following processing.

i. After the desired processing is completed by the interrupt, the processor interrupt is disabled.

ii. A write access is made to the current interrupt request level register (CILN) to clear the highest current interrupt request level.

iii. If the interrupt is in the highest level, the general-purpose registers are restored from memory, and the RTI instruction is executed to return from the interrupt. Otherwise, the general-purpose registers are restored from memory, and the PC and PSW registers are popped.

The following processing is made on the hardware.

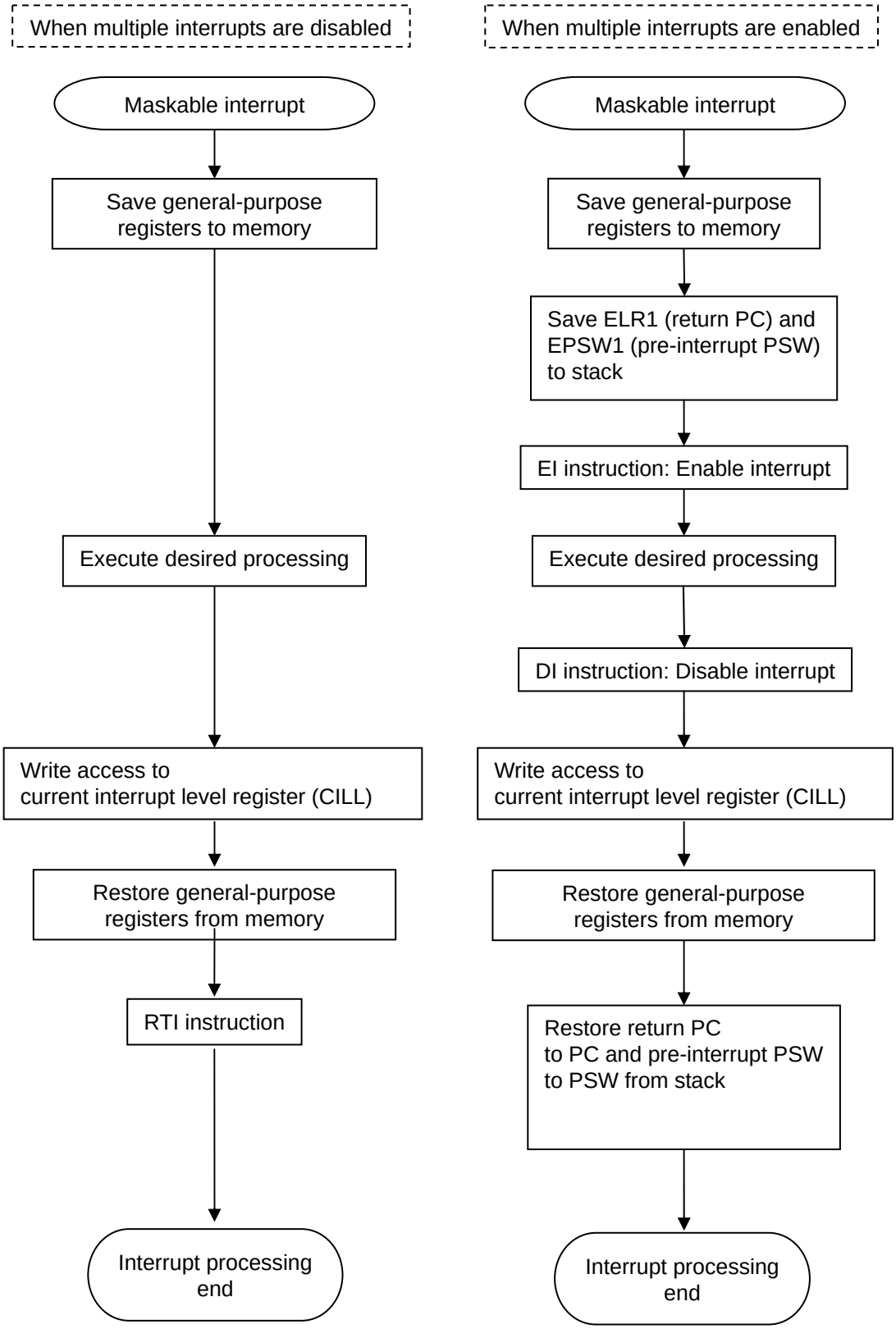
i. When a write access is made to the current interrupt request level register (CILN), the highest order set bit of the CILN register is cleared.

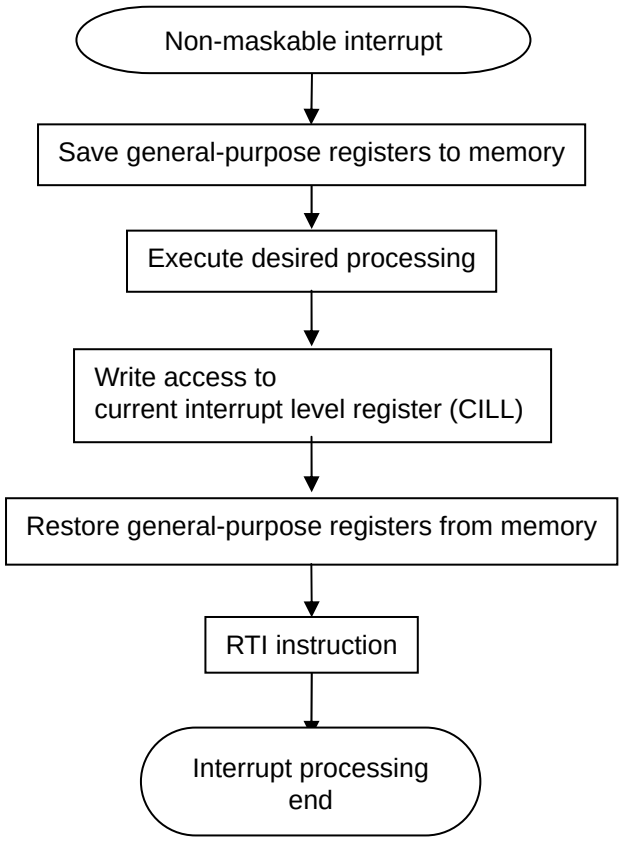
ii. If there is an interrupt request flag with a higher interrupt level than the current interrupt request level of the CILN register among the interrupt request flags which are pending in the interrupt request register (IRQ), an interrupt request is made to the U16 processor. In this case, if there are multiple interrupt request flags with higher interrupt levels than the current interrupt request level of the CILL register, the interrupt with the highest priority (lowest interrupt source number) is requested to the U16 processor.

[Note] For the “interrupt source number”, see Table 5-13 Interrupt Sources.

5.3.6 Flow Chart When Interrupt Level Control Enabled

The figure below shows the flow chart of the software processing of a maskable interrupt when the interrupt level control is enabled. The EI and DI instructions allow the execution of multiple interrupts by a higher-level maskable interrupt request during the "execution of the desired processing". Note that a non-maskable interrupt can be made for a maskable interrupt regardless of the execution of EI and DI instructions due to the specification of U16 processor.




Non-maskable interrupt
Save general-purpose registers to memory
Execute desired processing
Write access to
current interrupt level register (CILL)
Restore general-purpose registers from memory
RTI instruction
Interrupt processing
end

5.3.7 How To Write Interrupt Processing When Interrupt Level Control Enabled

When ILE of the interrupt level control enable register (ILENL) is set to enable the interrupt level control, the interrupt function should be written as below. For more details and notes on how to write the interrupt processing, refer to "CCU8 Programming Guide".

① Writing interrupt function to disable multiple interrupts

When writing an interrupt function to disable multiple interrupts, specify "1" in the category field of the INTERRUPT and SWI pragmas. If the built-in function __EI is called in an interrupt function that disables multiple interrupts, CCU8 generates an error.

After the desired interrupt processing is completed, the highest current interrupt request level (CILN bit) must be cleared by writing to CILL register. Otherwise, the current highest level or lower interrupt will not be accepted.

Example of description

```
static void intr_fn_0A(void);
#pragma interrupt intr_fn_0A 0x0A 1
volatile unsigned short TM1msec;
static void intr_fn_0A(void)
{
      TM1msec++;
        CILL = 0;    /*Clear the highest current interrupt request level*/
}
```

When writing as shown in the example, intr_fn_0A is handled as interrupt processing function that disables multiple interrupts.

CCU8 outputs the assembly code as shown below.

Example of output

```
_intr_fn_0A       :
            push        er0
;;      TM1msec++;
            l           er0,      NEAR _TM1msec
            add         er0,      #1
            st          er0,      NEAR _TM1msec
;;}
;;      CILL = 0;
            mov         r0,       #00h
            st          r0,       0f022h
;;}
            pop         er0
            rti
```

Interrupt functions save registers that may be used in the interrupt processing (here, only ER0) in the stack. To return from an interrupt function that disables multiple interrupts, "RTI" is used.

The example below shows how to call other functions from an interrupt function.

Example of description

```
static void intr_fn_10(void);
#pragma interrupt intr_fn_10 0x10 1
void func(void);
static void intr_fn_10(void)
{
      func();
      CILL = 0;    /*Clear the highest current interrupt request level*/
}
```

Example of output

```
_intr_fn_10       :
            push        lr,       ea
```

```
            push    xr0
            l       r0,     DSR
            push    r0

;;      func();
            bl      _func

;;}
;;      CILL = 0;
            mov     r0,     #00h
            st      r0,     0f022h
;;}
            pop     r0
            st      r0      DSR
            pop     xr0
            pop     ea      lr
            rti
```

When calling other functions from an interrupt function, the output code becomes more redundant, which results in a longer interrupt processing time. This is because CCU8 does not know which register is used by func and thus saves all possible registers that may be changed by calling the func function in the stack.

Note

Ensure that no interrupt is enabled in a function which is called from another function disabling multiple interrupts. If it is enabled, the program may run out of control when multiple interrupts are generated.

② Writing interrupt function to enable multiple interrupts

When writing an interrupt function to enable multiple interrupts, specify "2" in the category field of the INTERRUPT and SWI pragmas. Even when the specification of the category field is omitted, multiple interrupts are enabled. The built-in function __EI can be called in an interrupt function that enables multiple interrupts.

Example of description

```
static void intr_fn_20(void);
volatile unsigned short TM2msec;
#pragma interrupt intr_fn_20 0x20 2
static void intr_fn_20(void)
{
    __EI();         /* Enable multiple interrupts */
    TM2msec++;
    __DI();         /* Disable multiple interrupts */
    CILL = 0;       /* Clear the highest current interrupt request level */
}
```

When writing as shown in the example, intr_fn_20() is handled as interrupt processing function that enables multiple interrupts.
CCU8 outputs the assembly code as shown below.

Example of output

```
_intr_fn_20     :
            push    elr,        epsw
            push    er0
;;      __EI();   /* Enable multiple interrupts */
            ei
;;      TM1msec++;
            l       er0,    NEAR _TM2msec
            add     er0,    #1
            st      er0,    NEAR _TM2msec
;;      __DI();   /* Disable multiple interrupts */
```

```
            di
;;}
;;      CILL = 0;
            mov         r0,         #00h
            st          r0,         0f022h
;;}
            pop         er0
            pop         psw, pc
```

An interrupt function enabling multiple interrupts should save ELR and EPSW in the stack so that ELR and EPSW are not destroyed by multiple interrupts. This is different from the case for interrupt functions disabling multiple interrupts.

Besides, "POP PSW, PC" is used to return from the interrupt function, instead of "RTI".

5.3.8 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1:Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine

When the interrupt conditions are satisfied in this interval, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2:Between the DSR prefix instruction and the next instruction

When the interrupt conditions are satisfied in this interval, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

For the DSR prefix instruction, see "nX-U16/100 Core Instruction Manual".

Chapter 6 Clock Generation Circuit

6 Clock Generation Circuit

6.1 General Description

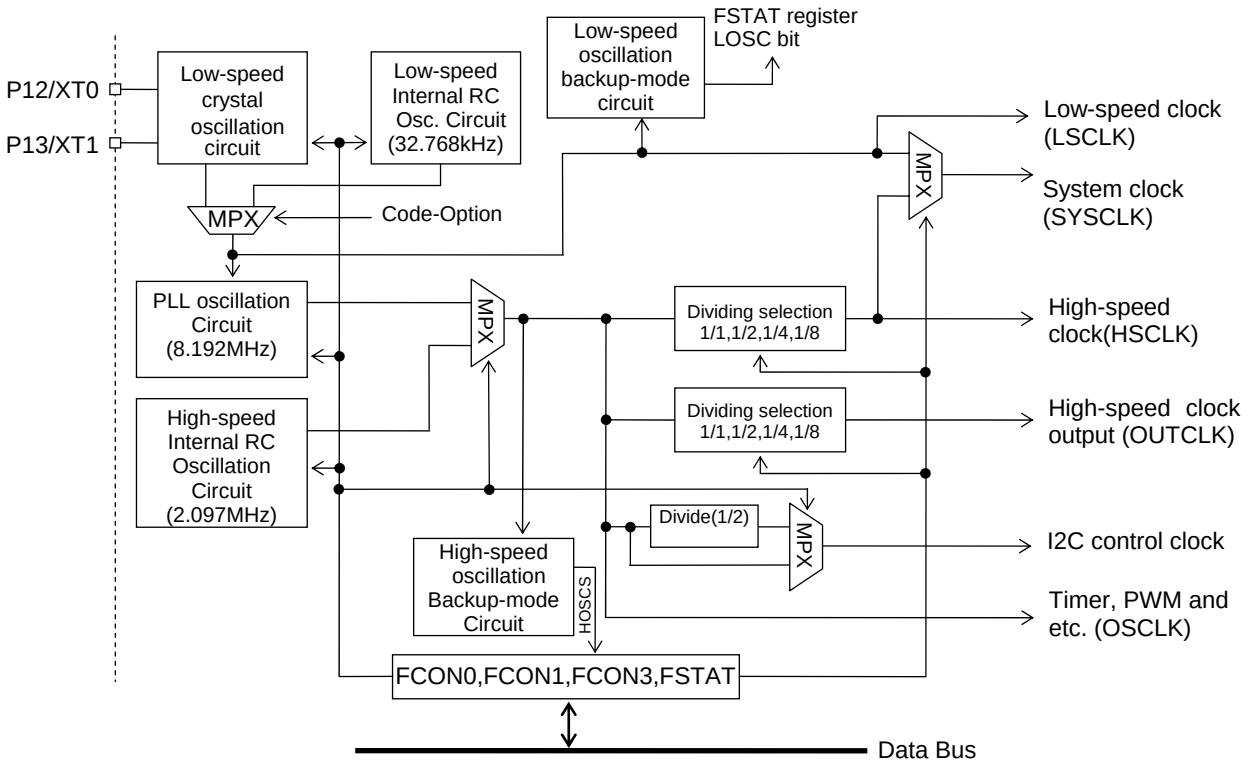
The clock generation circuit generates and provides the low-speed clock (LSCLK), the high-speed clock (HSCLK), the system clock (SYSCLK), and the high-speed output clock (OUTCLK). LSCLK and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and OUTCLK is a clock that is output from a port.
For the OUTCLK output port, see Chapter 17, "Port 2".
For the STOP mode described in this chapter, see Chapter 4, "MCU Control Function".

6.1.1 Features

- Low-speed clock generation circuit:
  - Crystal oscillation mode (32.738kHz)
  - Built-in RC oscillation mode (32.768kHz)
- High-speed clock generation circuit:
  - Built-in PLL oscillation mode (8.192MHz)
  - Built-in RC oscillation mode (2.097MHz)
- Low-speed /High-Speed Clock backup-mode function:
  - The backup function for the low-speed clock is available when selecting the low-speed crystal oscillation by Code-Option. A divided clock of the high-speed internal RC oscillation clock is used for the backup clock(Approx. 30kHz).
  - The backup function for the high-speed clock is available when selecting the low-speed crystal oscillation by Code-Option and selecting the internal PLL oscillation by FCON registers. The high-speed internal RC oscillation clock is used for the backup clock (The rrequency depends on the setting of FCON0 register).

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1
FCON3 : Frequency control register 3
FSTAT : Frequency status register

Figure 6-1 Configuration of Clock Generation Circuit

[Note]
After power-on or system reset, the operation starts by the clock supplied from the built-in high-speed clock generation circuit with the frequency divided by 8. Change it as needed by setting the FCON0, FCON1 and FCON2 register.

6.1.3 List of Pins

Pin Name	I/O	Function
P12/XT0	I	Pin for connecting a crystal for low-speed clock.
P13/XT1	I/O	Pin for connecting a crystal for low-speed clock.

6.1.4 Clock Configuration Diagram

Figure 6-2 shows the clock system diagram.

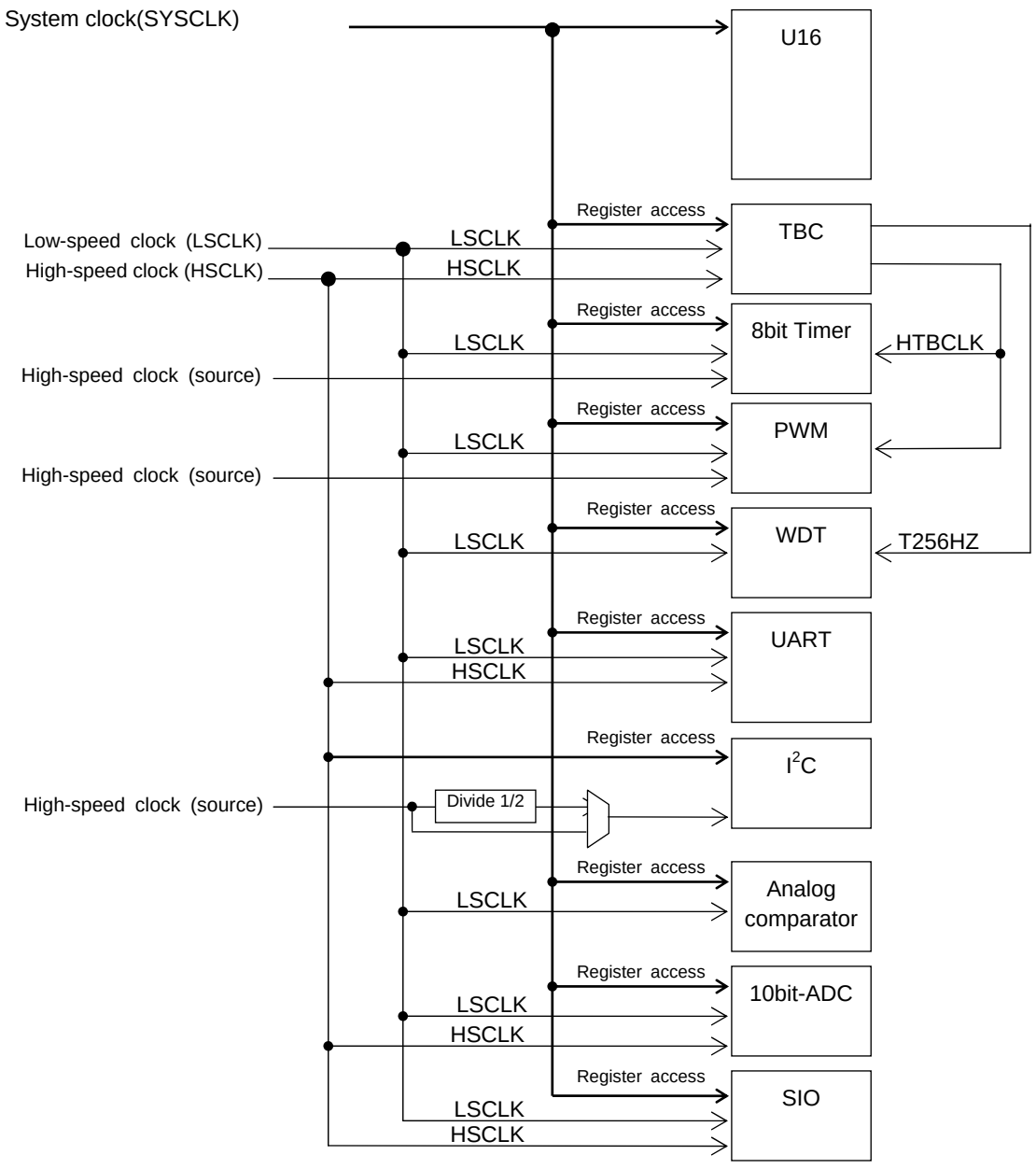


Figure 6-2 Clock System Diagram

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON01	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	03H
0F005H	Frequency control register 3	FCON3	-	R/W	8	00H
0F00AH	Frequency status register	FSTAT	-	R	8	04H

6.2.2 Frequency Control Register 0 (FCON0)

Address: 0F002H (FCON0)
Access: R/W
Access size: 8/16 bit
Initial value: 33H

	7	6	5	4	3	2	1	0
FCON0	-	-	OUTC1	OUTC0	OSCM1	OSCM0	SYSC1	SYSC0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	0	0	1	1

FCON0 is a special function register (SFR) used to control the high-speed clock generation circuit and to select system clock.

Description of Bits

- **OUTC 1, OUTC 0** (bits 5,4)
  The OUTC1 and OUTC0 bits select the frequency of the high-speed output clock (OUTCLK) output when the secondary function of the port is used. 1/1OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	1/1OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

- **OSCM1, OSCM0** (bits 3, 2)
  The OSCM1 and OSCM0 bits are used to select the high-speed clock mode, Built-in RC oscillation mode, or Built-in PLL oscillation mode.
  OSCM1 and OSCM0 can be rewritten only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0").
  At system reset, the built-in RC oscillation mode is selected.
  When switching the high-speed clock mode, please first switch the system clock back to the low-speed clock before switching to other high-speed clock (set the ENOSC and SYSCLK bits of the FCON1 register to "0").

OSCM1	OSCM0	Description
0	0	Built-in RC oscillation mode (initial value)
0	1	Do not use
1	0	Built-in PLL oscillation mode
1	1	Do not use

- **SYSC1, SYSC0** (bits 1, 0)
  The SYSC1, and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits. OSCLK, 1/2OSCLK, 1/4OSCLK or 1/8OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

SYSC2	SYSC1	SYSC0	Description
0	0	0	OSCLK
0	0	1	1/2OSCLK
0	1	0	1/4OSCLK
0	1	1	1/8OSCLK (initial value)

[Note]
•To switch the high-speed clock mode using the OSCM1 and OSCM0 bits, stop the high-speed oscillation and set the system clock to the low-speed clock (set the ENOSC and SYSCLK bits of the FCON1 register to "0").
• Supply 2.2V or higher to VDD pin when driving the 8.192MHz to the ports.

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H (FCON1)
Access: R/W
Access size: 8 bit
Initial value: 03H

	7	6	5	4	3	2	1	0
FCON1	LPLL	-	-	-	-	-	ENOSC	SYSCLK
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	1	1

FCON01 is a special function register (SFR) used to control the high-speed clock generation circuit and to select system clock.

Description of Bits

- **LPLL** (bit 7)
  The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
  When the LPLL bit is set to "1", this indicates that the PLL oscillation frequency is locked within ±2.5%.
  When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillation frequency is not within ±2.5%. LPLL is a read-only bit.

LPLL	Description
0	PLL oscillation is inactive or the PLL oscillation frequency is not within ±2.0% (initial value)
1	PLL oscillation frequency is locked within ±2.0%.

- **ENOSC** (bit 1)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator circuit.

ENOSC	Description
0	Disables high-speed oscillation
1	Enables high-speed oscillation (initial value)

- **SYSCLK** (bit 0)
  The SYSCLK bit is used to select system clock. The low-speed clock (LSCLK) or the HSCLK (1/nOSCLK: n = 1,2, 4, 8) selected by the FCON0 high-speed clock frequency selection bit (SYSC1,0) can be selected.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

6.2.4 Frequency Control Register 3(FCON3)

Address: 0F005H(FCON3)
Access: R/W
Access size: 8 bits
Initial Value: 00H

	7	6	5	4	3	2	1	0
FCON3	-	-	-	-	-	LOSCB	HOSCB	-
R/W	R	R	R	R	R	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

FCON3 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock. FCON3 works only when the low-speed crystal oscillation circuit is selected by Code-Option. No need to use when selecting the low-speed internal RC oscillation circuit by Code-Option.

Description of Bits

- **LOSCB** (bit 2)

The LOSCB bit shows the low-speed clock backup mode, and it is used to cancel the backup mode by clearing the LOSCB bit(by writing "1" to the LOSCB bit).
The LOSCB bit works only when the low-speed crystal oscillation circuit is selected by Code-Option.
When the LOSCB bit is "1" it indicates that the low-speed clock works in the backup mode. The backup mode means that external low-speed crystal oscillation stopped for a reason and instead a divided clock of the high-speed internal RC oscillation clock (Approx. 30kHz) is supplied as the low-speed clock.

The status of external low-speed crystal oscillation can be checked by LOSCS bit of Frequency Status (FSTAT) register. The LOSCS bit becomes "1" after the powering-up the LSI, .when the external low-speed crystal oscillation has stopped, or the LSI has entered into STOP mode. "0" in LOSCS bit means the external low-speed crystal oscillation normally works, therefore, check the LOSCS bit is "0" before cancelling the backup mode.

The cancelling the backup mode can be executed by writing "1" to the LOSCB bit, change the low-speed clock to the crystal oscillation clock and the LOSCB bit also changes to "0". Writing "0" to the LOSCB bit does not work to change the mode.

LOSCB	Description
0	The low-speed clock is running by the low-speed 32.768kHz crystal oscillation clock (initial value)
1	The low-speed clock is running by the divided clock of high-speed internal RC oscillation clock (Approx. 30kHz).

- **HOSCB** (bit 1)
  The HOSCB bit shows the high-speed clock backup mode, and it is used to cancel the backup mode by clearing the HOSCB bit(by writing "1" to the HOSCB bit).
  The HOSCB bit works only when the low-speed crystal oscillation circuit is selected by Code-Option and PLL oscillation is selected as the high-speed clock by FCON registers. When the HOSCB bit is "1" it indicates that the high-speed clock works in the backup mode. The backup mode means that PLL oscillation stopped for a reason and instead the high-speed internal RC oscillation clock is supplied as the high-speed clock.

  The status of PLL oscillation can be checked by HOSCS bit of Frequency Status (FSTAT) register. The HOSCS bit becomes "1" when the PLL oscillation has stopped, or the LSI has entered into STOP mode. "0" in HOSCS bit means the PLL oscillation normally works, therefore, check the HOSCS bit is "0" before cancelling the backup mode.
  The cancelling the backup mode can be executed by writing "1" to the HOSCB bit, change the high-speed clock to the PLL oscillation clock and the HOSCB bit also changes to "0". Writing "0" to the HOSCB bit does not work to change the mode.
  The HOSCB bit remains "1" after STOP mode is released, need to have a process to cancel the backup-mode.

HOSCB	Description
0	The high-speed clock is running by the PLL oscillation clock (initial value)
1	The high-speed clock is running by the high-speed internal RC oscillation backup clock (2.097MHz)

[Note]
• When the low-speed crystal oscillation circuit is selected by Code-Option, the LSI always enters to the RC oscillation backup mode after the power-up, therefore, make sure to cancel the backup mode.

6.2.5 Frequency Status Register (FSTAT)

Address: 0F00AH
Access: R
Access size: 8 bits
Initial value: 06H

	7	6	5	4	3	2	1	0
FSTAT	-	-	-	-	-	LOSCS	HOSCS	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	1	0

FSTAT is a special function register (SFR) used to show the clock generation circuit state.

Description of Bits

- **LOSCS** (bit 2)
  LOSCS indicates the oscillation status of the low-speed oscillation circuit. LOSCS changes when the clock backup interrupt (CKCINT) occurs. The LOSCS bit becomes "1" when the LSI enters the STOP mode, but the CKCINT does not occur. For CKCINT, see Chapter 5, “Interrupts”.

LOSCS	Description
0	The low-speed crystal oscillation circuit is supplying the clock after counting 8192-pulse.
1	Indicates one of following status. (initial value) The low-speed crystal oscillation is stopped or oscillation circuit is counting the oscillation stabilization time. The low-speed clock is working by the internal RC oscillation backup clock.

- **HOSCS** (bit 1)
  HOSCS indicates the oscillation status of the PLL oscillation circuit. The HOSCS bit works only when the low-speed crystal oscillation circuit is selected by Code-Option and PLL oscillation is selected as the high-speed clock by FCON registers.

HOSCS	Description
0	The PLL oscillation normally works or the PLL oscillation is disabled.
1	After the PLL oscillation enabled, the PLL oscillation has stopped for a reason or the LSI has entered into the STOP mode.

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Crystal Oscillation Circuit

Figure 6-3 shows the low-speed clock generation circuit configuration.
The low-speed clock generation circuit requires an external 32.768 kHz crystal to work. To match the oscillation frequency by using a trimmer capacitor, connect external capacitors (C_{GL} and C_{DL}) as required.
The 32.768kHz crystal oscillation is selectable by Code-Option, in which low-speed backup-mode function is available.

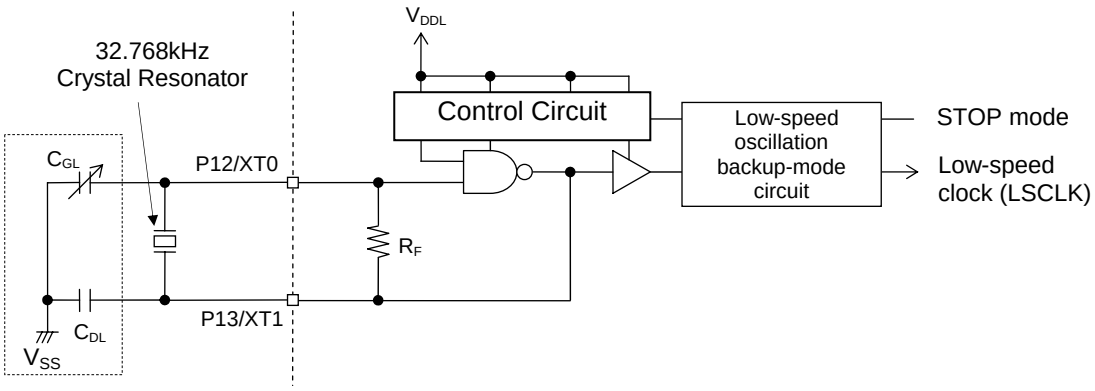


Figure 6-3 Circuit Configuration of the Low-Speed Crystal Oscillation

[Note]
- Install a crystal as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.
- Note that oscillation may stop due to condensation.

6.3.1.2 Low-Speed Built-In RC Oscillation Circuit

Figure 6-4 shows the block diagram of the built-in low-speed clock RC oscillation.
When the RC oscillation clock is counted to 16, the low-speed oscillation clock (LSCLK) starts to be supplied.
The low-speed RC oscillation circuit is always selected after the power-up or after the STOP mode is released.
When the low-speed RC oscillation is selected by Code-Option, the backup-mode function is not available.

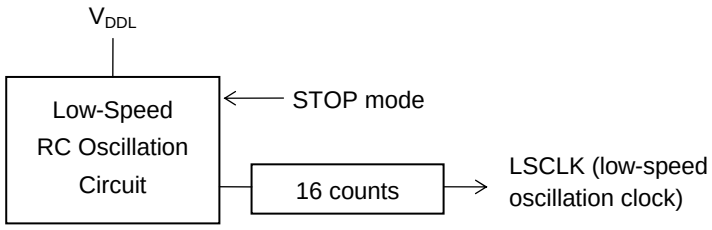


Figure 6-4 Block Diagram of the Built-in Low-Speed RC Oscillation

6.3.1.3 Operation of Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power ON reset.
After the power-on, it waits for the low-speed oscillation start time (T_{XTL}) and the low-speed clock (LSCLK) oscillation stabilization time (8192 counts). Then, the low-speed clock (LSCLK) is supplied to the peripheral circuits.
The low-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software.
When oscillation is resumed by releasing of the STOP mode by external interrupt, after the high-speed RC oscillation clock is counted to 16, a divided clock of the RC oscillation (approx. 30kHz) is supplied to the peripheral as the LSCLK.
In parallel, after the elapse of the low-speed oscillation start period (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization time (8192 counts), the clock backup interrupt CKCINT occurs. Change from the RC oscillation clock to the crystal oscillation clock by writing "1" to LOSCB bit of Frequency Control register 3 (FCON3).
For STOP mode and CKCINT, see Chapter 4, "MCU Control Function" and Chapter 5, "Interrupts".
Figure 6-3 shows the timing chart of the low-speed clock generation circuit. For the low-speed oscillation start time (T_{XTL}), see Appendix C, "Electrical Characteristics".

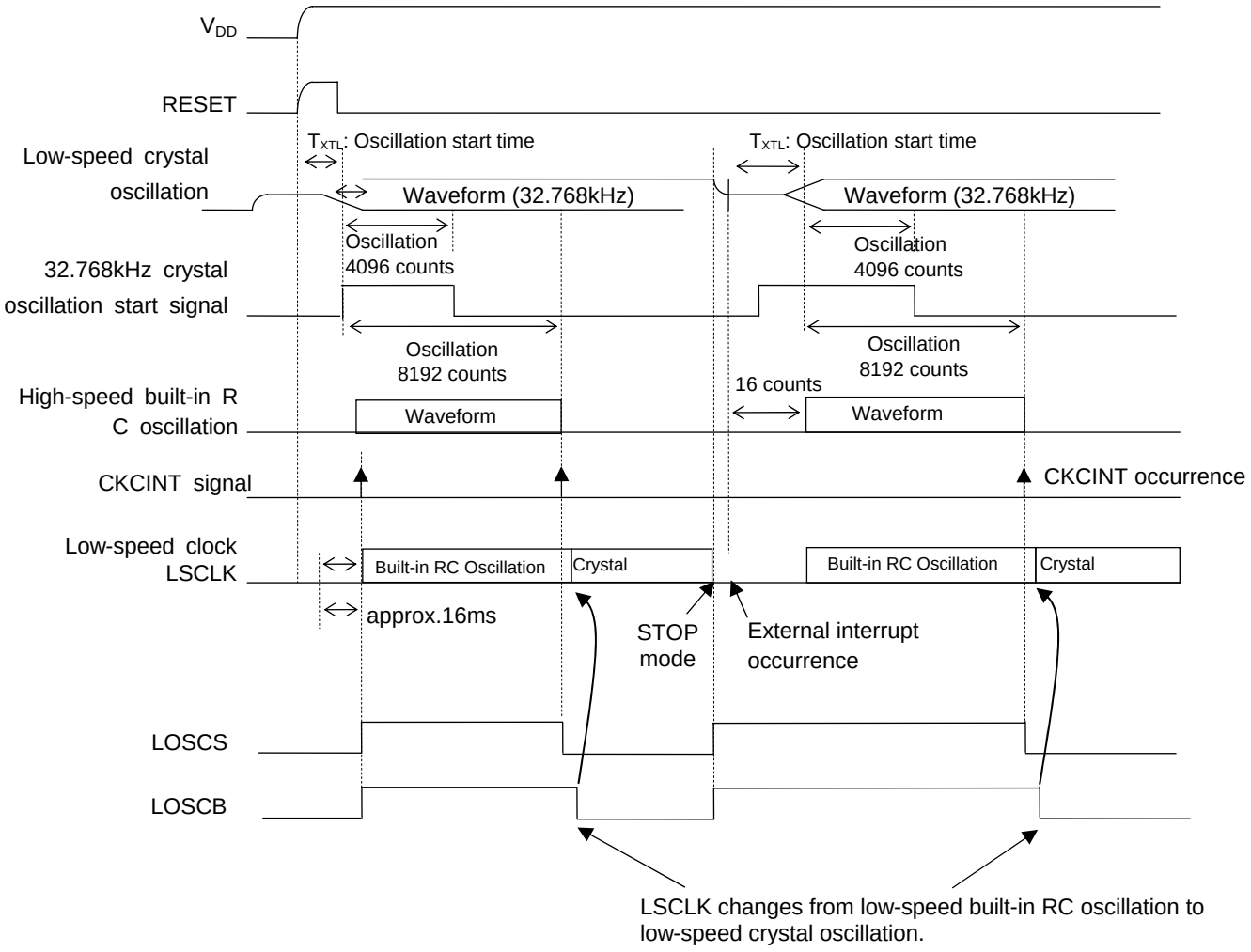


Figure 6-5 Operation of Low-Speed Clock Generation Circuit

6.3.2 High-Speed Clock

For the high-speed clock generation circuit, the built-in RC oscillation mode or the PLL (Phase Locked Loop) oscillation mode can be selected.

6.3.2.1 High-Speed Built-in RC Oscillation Circuit

Figure 6-6 shows the block diagram of high-speed built-in RC oscillation circuit.
When the RC oscillation clock is counted to 16, the high-speed oscillation clock (HSCLK) starts to be supplied.
The high-speed RC oscillation circuit is always selected after the power-up.
When the high-speed RC oscillation is selected by the software, the high-speed backup-mode function is not available.

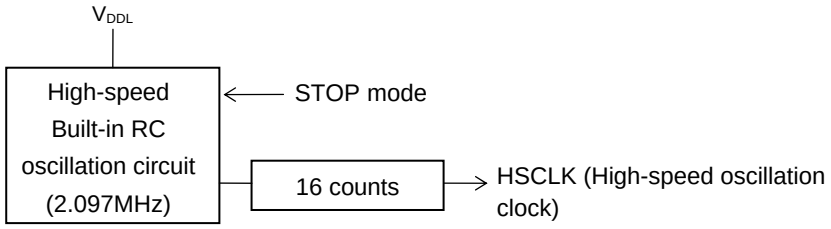


Figure 6-6 Block diagram of High-speed Built-In RC Oscillation Circuit

6.3.2.2 PLL Oscillation Circuit

The PLL oscillation circuit generates a clock of 16MHz (LSCLK × 500).
In built-in PLL oscillation mode (OSCM0 = “0”, OSCM1 = “1”), supply of OSCLK (high-speed oscillation clock) is started when PLL oscillation clock pulse count reaches 8192 after oscillation is enabled (ENOSC is set to “1”).
When the low-speed crystal oscillation circuit is selected by Code-Option and PLL oscillation is selected as the high-speed clock by FCON registers, the high-speed backup-mode is available.
Figure 6-7 shows the block diagram of PLL oscillation circuit.

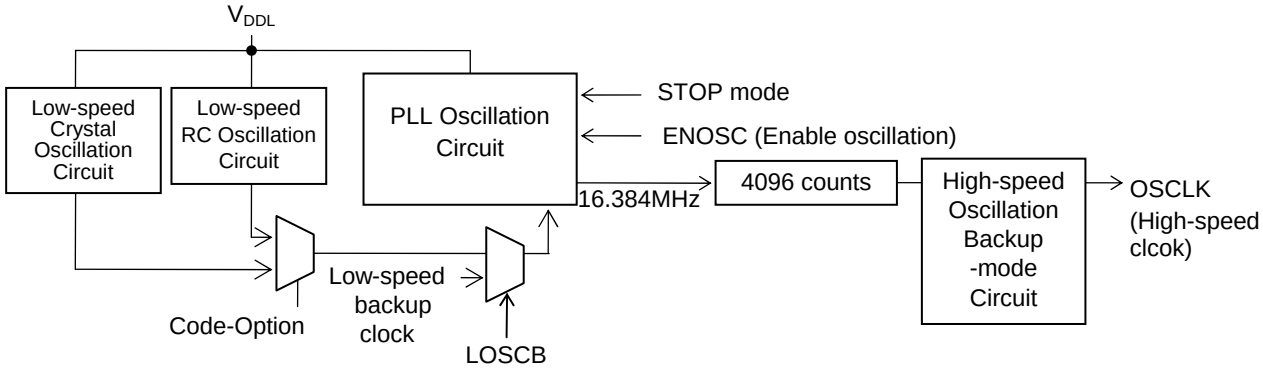


Figure 6-7 Block diagram of PLL Oscillation circuit

6.3.2.3 Operation of High-Speed Clock

The high-speed clock generation circuit is activated in the built-in RC oscillation mode (2.097MHz) by power-on reset generation.
As a result of the occurrence of power-on reset, the circuit goes into system reset mode and then shifts to program operating mode after the elapse of the high-speed oscillation start time (T_{XTH}) and the oscillation stabilization time (Count: 32,768) of the high-speed RC oscillation clock (OSCLK) and at the same time, a high-speed clock (HSCLK) is supplied to the peripheral circuits.
Figure 6-8 shows the waveforms of the high-speed clock generation circuit at power on. For the high-speed oscillation start time (T_{XTH}), see Appendix C, “Electrical Characteristics”.

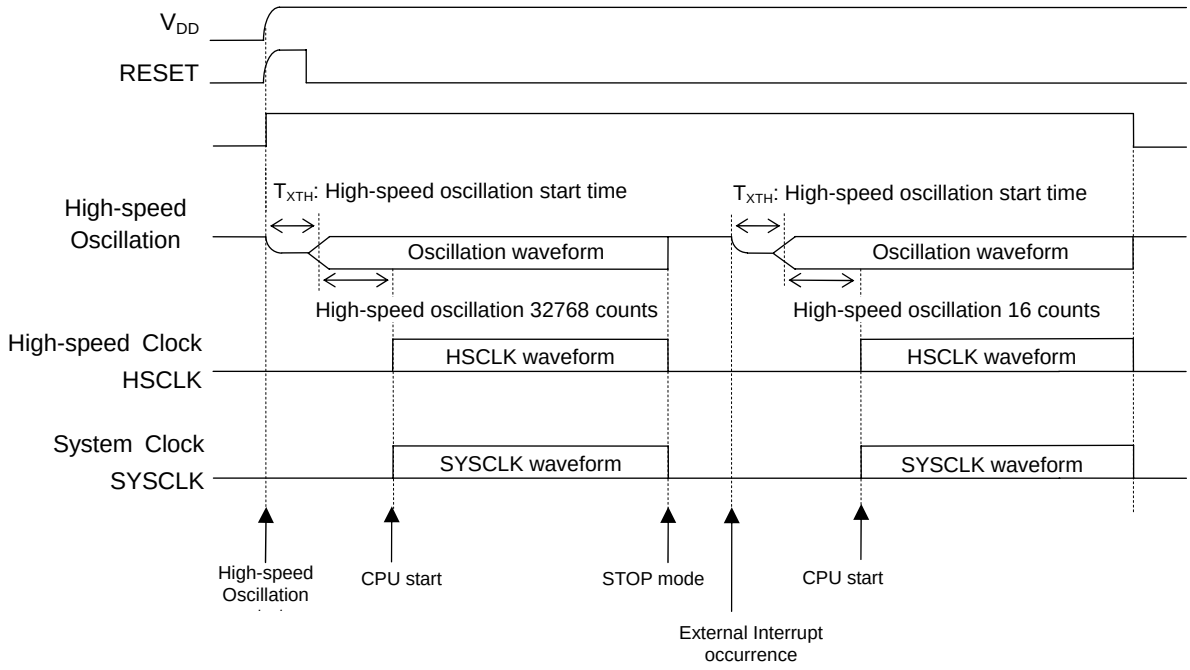


Figure 6-8 Operation of High-Speed Clock when Powering-up

The high-speed clock generation circuit allows the start/stop control of oscillation by using the frequency control registers 1 (FCON1). Oscillation can be started by setting the ENOSC bit of FCON1 to "1". After the start of oscillation, HSCLK starts supply of a clock to the peripheral circuits following the elapse of the high-speed oscillation start time in each mode (T_{XTH}/T_{EXT}) and the oscillation stabilization time.
The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. When the STOP mode is released by external interrupt, HSCLK supplies clocks to peripheral circuits following the elapse of the high-speed oscillation start time in each mode (T_{XTH}/T_{EXT}) and the oscillation stabilization time. The oscillation stabilization time is for 4096 clocks in the case of PLL oscillation mode and 16 clocks in the case of built-in RC oscillation mode.

Figure 6-9 shows the waveforms of the high-speed clock generation circuit in the mode of “external low-speed crystal oscillation + built-in PLL oscillation”.
Figure 6-10 shows the waveforms of the high-speed clock generation circuit in the mode of “internal low-speed RC oscillation + built-in PLL oscillation”.

[Note]
• In the PLL oscillation mode, note that the LSI behaves differently, depending on the type of low-speed clock.
• In the mode of “external low-speed crystal oscillation + built-in PLL oscillation” and after releasing the STOP mode, the high-speed RC oscillation clock is selected as the high-speed backup clock, therefore as needed, change the clock to the PLL oscillation clock by the software.

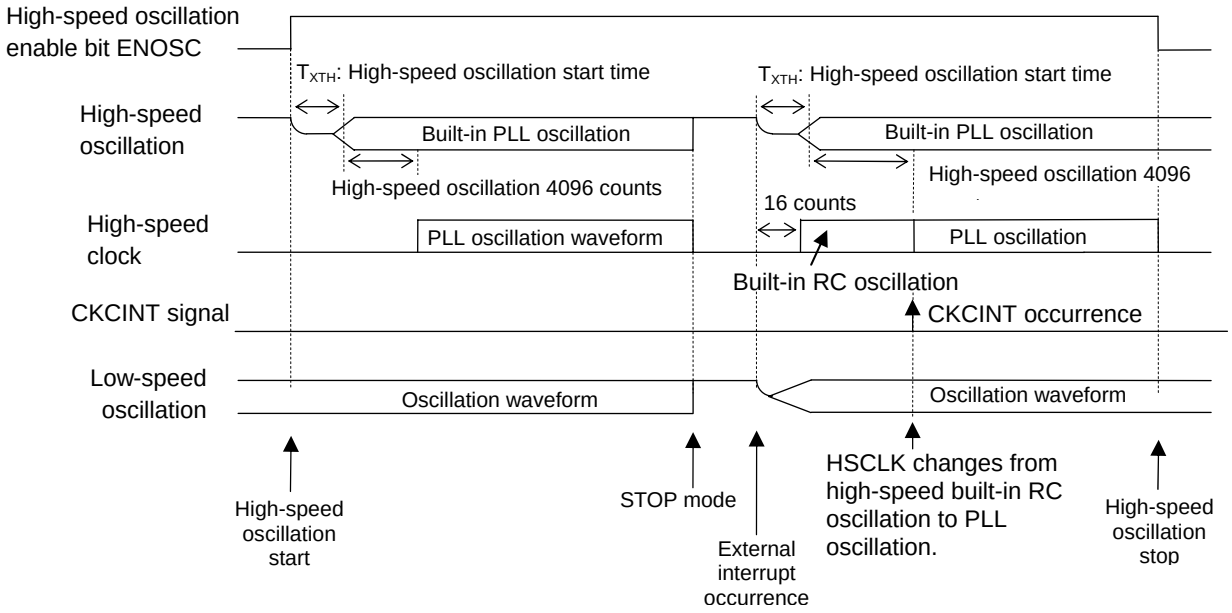


Figure 6-9 High-speed built-in PLL oscillation behavior (External low-speed crystal oscillation selected)

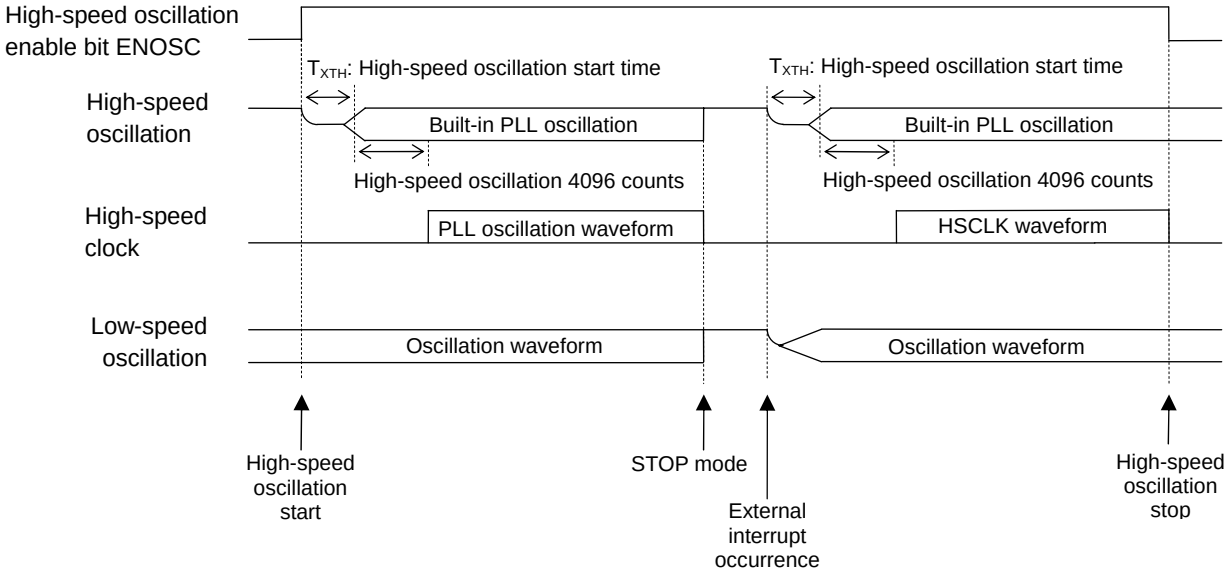


Figure 6-10 High-speed built-in PLL oscillation behavior (Internal low-speed RC oscillation selected)

6.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-11 shows the flow chart of the system clock switching processing (HSCLK→LSCLK), and Figure 6-12 shows the flow chart of the system clock switching processing (LSCLK→HSCLK).

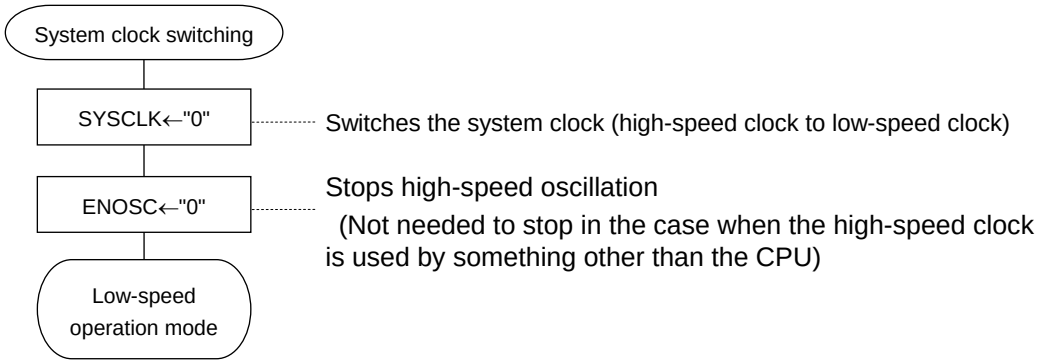


Figure 6-11 Flow Chart of System Clock Switching Processing (HSCLK→LSCLK)

[Note]
Immediately after the recovery from the STOP mode, if the system clock is switched from HSCLK to LSCLK, the CPU becomes inactive until LSCLK starts clock supply to the peripheral circuits. Therefore, It is recommended to switch to LSCLK after confirming that the LSCLK is oscillating by checking that the time base counter interrupt request bit (Select T128H for QLTBC0-2) is “1”.

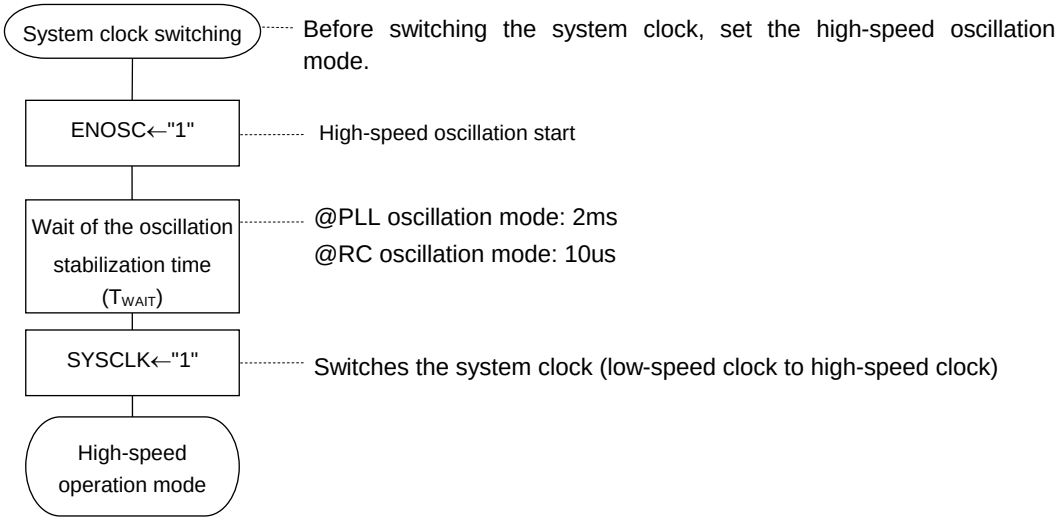


Figure 6-12 Flow Chart of System Clock Switching Processing (LSCLK→HSCLK)

[Note]
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Specifying Port Registers

To enable the clock output function, each related port register bit needs to be set. See Chapter 17, "Port 2" and Chapter 18, "Port 3" for detail about the port registers.

6.4.1 Functioning P21(OUTCLK) as the high-speed clock output

Set P21MD bit (bit1 of P2MOD register) to “1” for specifying the high-speed clock output as the secondary function of P21.

Register name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	P23MD	P22MD	**P21MD**	P20MD
Setting value	-	-	-	-	*	*	**1**	*

Set the P21C1 bit (P2CON1 register's bit 1) to "1" and the P21C0 bit (P2CON0 register's bit 1) to "1" for specifying the state mode of the P21 pin to CMOS output.

Register name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	P23C1	P22C1	**P21C1**	P20C1
Setting value	-	-	-	-	*	*	**1**	*

Register name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	P23C0	P22C0	**P21C0**	P20C0
Setting value	-	-	-	-	*	*	**1**	*

The P21D bit (P2D register bit 1) data can either be "0" or "1".

Register name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	P23D	P22D	**P21D**	P20D
Setting value	-	-	-	-	*	*	******	*

- : Bit that does not exist
* : Bit not related to the high-speed clock function
** : Don’t care

[Note]
P21 (Port 2) is an output-only port and does not have the register to select the data direction(input or output).

6.4.2 Functioning P20 (LSCLK) as the low-speed clock output

Set P20MD bit (bit0 of P2MOD register) to “1” for specifying the low-speed clock output as the secondary function of P20.

Register name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	P23MD	P22MD	P21MD	**P20MD**
Setting value	-	-	-	-	*	*	*	**1**

Set the P20C1 bit (P2CON1 register bit 0) to "1" and the P20C0 bit (P2CON0 register bit 0) to "1" for selecting the P20 pin state mode to CMOS output.

Register name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	P23C1	P22C1	P21C1	**P20C1**
Setting value	-	-	-	-	*	*	*	**1**

Register name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	P23C0	P22C0	P21C0	**P20C0**
Setting value	-	-	-	-	*	*	*	**1**

Data of P20D bit (bit0 of P2D register) does not affect to the low speed clock output function, so don’t care the data for the function.

Register name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	P23D	P22D	P21D	**P20D**
Setting value	-	-	-	-	*	*	*	******

- : Bit that does not exist
* : Bit not related to the low-speed clock function
** : Don’t care

[Note]
P20 (Port 2) is an output-only port and does not have the register to select the data direction(input or output).

6.4.3 Functioning P36 (LSCLK) as the low-speed clock output

Set P36MD1 bit (bit6 of P3MOD1 register) to “0” and Set P36MD0 bit (bit6 of P3MOD0 register) to “1”for specifying the low-speed clock output as the secondary function of P36.

Register name	P3MOD1 register (Address: 0F21DH)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36MD1**	P35MD1	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
Setting value	-	**0**	*	*	*	*	*	*

Register name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36MD0**	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
Setting value	-	**1**	*	*	*	*	*	*

Set the P36C1 bit (P3CON1 register bit 6) to "1" and the P36C0 bit (P3CON0 register bit 6) to "1" for selecting the P36 pin state mode to CMOS output.

Register name	P3CON1 register (Address: 0F21AH)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36C1**	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
Setting value	-	**1**	*	*	*	*	*	*

Register name	P3CON0 register (Address: 0F21BH)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36C0**	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
Setting value	-	**1**	*	*	*	*	*	*

Set the P36DIR bit (P3DIR register bit 6) to "0" for selecting the I/O direction of P36 pin to output.

Register name	P3DIR register (Address: 0F219H)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36DIR**	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
Setting value	-	**0**	*	*	*	*	*	*

Data of P36D bit (bit6 of P3D register) does not affect to the low speed clock output function, so don’t care the data for the function.

Register name	P3D register (Address: 0F218H)							
Bit	7	6	5	4	3	2	1	0
Bit name	-	**P36D**	P35D	P34D	P33D	P32D	P31D	P30D
Setting value	-	******	*	*	*	*	*	*

- : Bit that does not exist
* : Bit not related to the low-speed clock function
** : Don’t care

Chapter 7 Time Base Counter

7 Time Base Counter

7.1 General Description

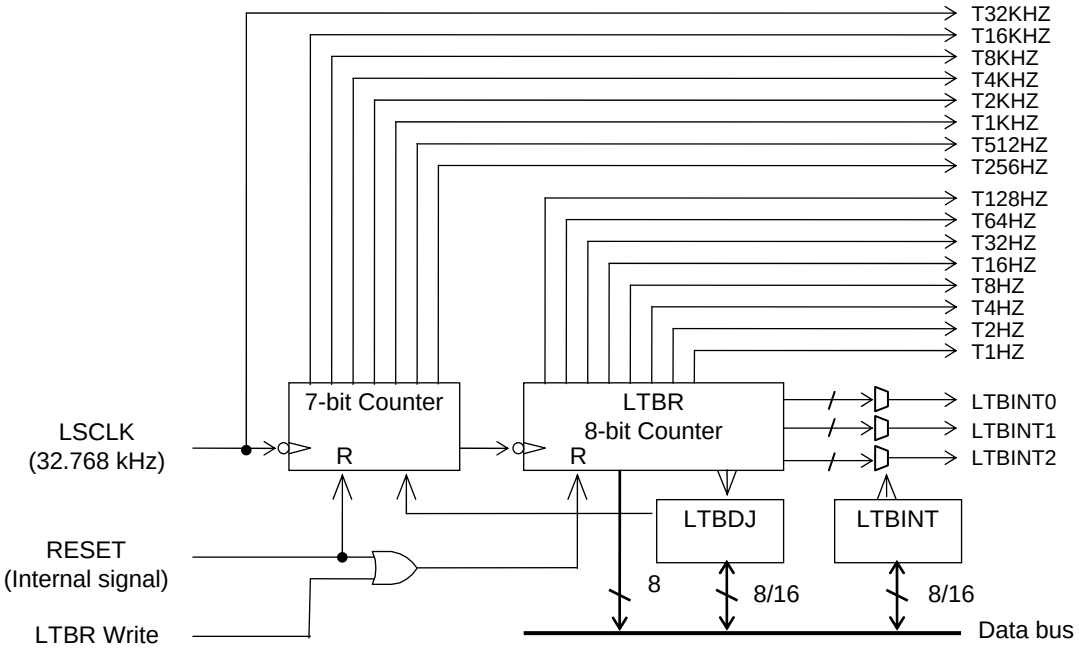
This LSI includes a low-speed time base counter (LTBC) that generate base clocks for peripheral circuits and periodical interrupts. For the input clock, see Chapter 6, “Clock Generation Circuit”. For interrupt permission, interrupt request flags, etc. described in this chapter, see Chapter 5, “Interrupt”.

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK).
- LTBC allows frequency adjustment (Adjustment range: Approx. 488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) by using the low-speed time base counter frequency adjustment registers (LTBADJH and LTBADJL).
- 3clocks between 128Hz and 1Hz can be used as interrupt signal.

7.1.2 Configuration

Figure 7-1 show the configuration of a low-speed time base counter respectively.



LTBR : Low-speed time base counter register
LTBADJ : Low-speed time base counter frequency adjust register
LTBINT : Low-speed time base counter interrupt select

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F060H	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F062H	Low-speed time base counter frequency adjustment register 0	LTBADJL	LTBADJ	R/W	8/16	00H
0F063H	Low-speed time base counter frequency adjustment register 1	LTBADJH		R/W	8	00H
0F064H	Low speed time base counter interrupt select resister 0	LTBINTL	LTBINT	R/W	8/16	30H
0F065H	Low speed time base counter interrupt select resister 1	LTBINTH		R/W	8	06H

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F060H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter.
The T128HZ-T1HZ outputs are set to “0” when write operation is performed for LTBR.

[Note]
• LTBC interrupts may occur depending on the LTBR write timing. See the notes on software programming described in the section 7.3.1 “Low-Speed Time Base Counter”.

7.2.3 Low-Speed Time Base Counter Frequency Adjustment Registers (LTBADJ)

Address: 0F062H(LTBADJL), 0F063H(LTBADJH)
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
LTBADJL	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
LTBADJH	—	—	—	—	—	LADJ10	LADJ9	LADJ8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBADJL and LTBADJH are special function registers (SFRs) to set the frequency adjustment values of the low-speed time base clock.

[Description of Bits]

- **LADJ10-LADJ0** (bits 10-0)
  The LADJ10 to LADJ0 bits are used to adjust frequency.
  Adjustment range: Approx. –488ppm to +488ppm.
  Adjustment accuracy: Approx. 0.48ppm

Table 7-1 Correspondence between Frequency Adjustment Values (LTBADJH, LTBADJL) and Adjustment Ratio

LADJ10 to 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	–0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	–0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	–487.80
1	0	0	0	0	0	0	0	0	0	0	400H	–488.28

The adjustment values (LADJ10 to LADJ0) to be set in LTBADJH and LTBADJL can be obtained by using the following equations:

Adjustment value = Frequency adjustment ratio × 2097152 (decimal)
= Frequency adjustment ratio × 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (gaining time)
Adjustment value = +15.0ppm × 2097152 (decimal)
$= +15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≅ 01Fh (hexadecimal)

Example 2: When adjusting −25.5ppm (losing time)
Adjustment value = −25.5ppm × 2097152 (decimal)
$= -25.5 \times 10^{-6} \times 2097152$
= −53.477376 (decimal)
≅ 7CCh (hexadecimal)

[Note]
• The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function. The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

7.2.4 Low-Speed Time Base Counter Interrupt select Registers (LTBINT)

Address: 0F064H(LTBINTL), 0F065H(LTBINTH)
Access: R/W
Access size: 8/16 bits
Initial value: 0630H

	7	6	5	4	3	2	1	0
LTBINTL	—	LTI1S2	LTI1S1	LTI1S0	—	LTI0S2	LTI0S1	LTI0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	0	0	0	0

	15	14	13	12	11	10	9	8
LTBINTH	—	—	—	—	—	LTI2S2	LTI2S1	LT2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	1	0

LTBINT is a special function register(SFR) which specify low speed time base clock which is used as an interrupt signal.

[Description of Bits]

- **LADJ10-LADJ0** (bits 10-0)s

- **LTI2S2～LTI2S0** (bit 10 ~8)
  The bits specify an assignable clock to LTBINT2. Initical value is T2HZ.

- **LTI1S2～LTI1S0** (bit 6 ~4)
  The bits specify an assignable clock to LTBINY1. Initial value is T16HZ.

- **LTI0S2～LTI0S0** (bit 2 ~0)
  The bits specify an assignable clock to LTBINT0. Initial value is T128HZ.。

LTInS2	**LTInS1**	**LTInS0**	Assignable clock
0	0	0	T128HZ
0	0	1	T64HZ
0	1	0	T32HZ
0	1	1	T16HZ
1	0	0	T8HZ
1	0	1	T4HZ
1	1	0	T2HZ
1	1	1	T1HZ

* an interrupt may occur at setting.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T64HZ, T32HZ, T16HZ, T8HZ, T4HZ, T2HZ, and T1HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-2 shows an example of program to read LTBR.

```
        LEA     offset LTBR         ; EA←LTBR address
MARK:
        L       R0,     [EA]        ; 1st read
        L       R1,     [EA]        ; 2nd read
;
        CMP     R0,     R1          ; Comparison for LTBR
        BNE     MARK                ; To MARK when the values do not coincide
;
          :
```

Figure 7-2 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to “0”. At this time, Interrupt occurs when clock is assigned to LTBC interrupt changing from “1” to “0”. Therefore, when LTBR is reset, After prohibits each TBC interrupts of interrupt controller, LTBR is reset and the processing which clears LTBR interrupt request which occurred by reset is needed. Figure 7-3 shows the sequence to clear the LTBC interrupt request.

One CPU cycle is needed after LTBR interrupt occurs until LTBC interrupt request flag of interrupt controller is set. When LTBC interrupt request is cleared after the writing LTBR, Please do not put the instruction that clears the interrupt request flag just after the instruction that writes to LTBR, and place an NOP instruction to have time before clearing the interrupt request flag.

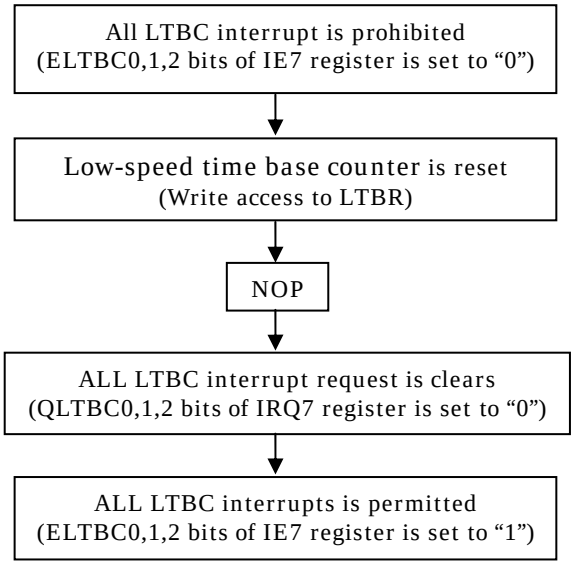


Figure 7-3 Sequence to Clear the LTBC Interrupt Request which Occurred by LTBR Reset

Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

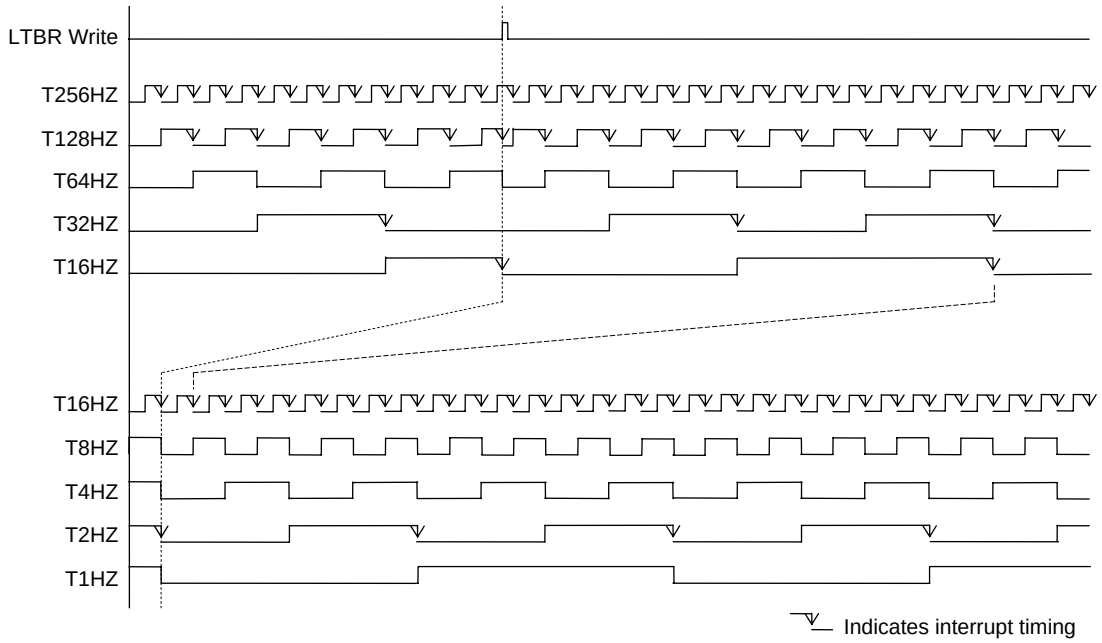


Figure 7-4 Interrupt Timing and Reset Timing by Writing to LTBR

Chapter 8 8bit Timer

8 8bit Timer

8.1 General Description

This LSI includes two channels of 8-bit timers.
For the input clock, see Chapter 6, “Clock Generation Circuit”.

8.1.1 Features

- The timer interrupt (TMnINT, n=0 to 7) is generated when the values of timer counter register (TMnC) and timer data register (TMnD) coincide.
- A timer configured by combining timer 0 and timer 1 can be used as a 16-bit timer.
- Low-speed clock (LSCLK) or high-speed clock (OSCLK) is selectable for the timer clock.
- Dividing of the timer clock is selectable(1/2, 1/4, 1/8, 1/16 1/32 and 1/64).
- Auto-reload timer mode or one shot timer mode is selectable.

8.1.2 Configuration

Figure 8-1 show the configuration of the timer.

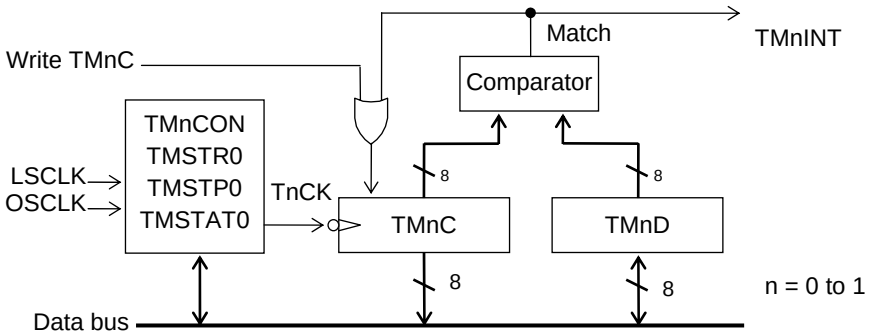


Figure 8-1 (a) 8-bit Timer Mode (Timers 0 to 1)

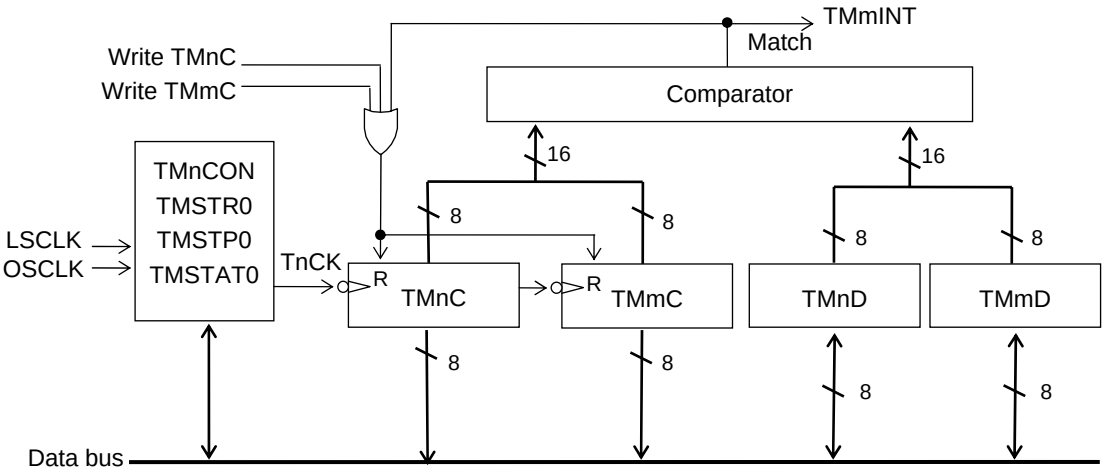


Figure 8-1 (b) 16-bit Timer Mode (Timers 0 to 1)

TMnCON:	Timer control register	TMSTR0:	Timer start register 0
TMmD, TMnD:	Timer data registers	TMSTP0:	Timer stop register 0
TMmC, TMnC:	Timer counter registers	TMSTAT0:	Timer status register 0

Figure 8-1 Configuration of Timers

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F300H	Timer 0 data register	TM0D	TM01D	R/W	8/16	0FFH
0F301H	Timer 1 data register	TM1D		R/W	8	0FFH
0F310H	Timer 0 counter register	TM0C	TM01C	R/W	8/16	00H
0F311H	Timer 1 counter register	TM1C		R/W	8	00H
0F320H	Timer 0 control register	TM0CON	TM01CON	R/W	8/16	00H
0F321H	Timer 1 control register	TM1CON		R/W	8	00H
0F330H	Timer start register 0	TMSTR0	-	R/W	8	00H
0F332H	Timer stop register 0	TMSTP0	-	R/W	8	00H
0F334H	Timer status register 0	TMSTAT0	-	R/W	8	00H

8.2.2 Timer n Data Register (TM0D)

Address: 0F300H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM0D	T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM0D is a special function register (SFR) to set the value to be compared with the timer n counter register (TM0C) value.

[Note]
Set TM0D when the timer stops(when T0STAT bit of TMSTAT0 register is “0”).
When “00H” is written in TM0D, TM0D is set to “01H”.

8.2.3 Timer n Data Register (TM1D)

Address: 0F300H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM1D	T1D7	T1D6	T1D5	T1D4	T1D3	T1D2	T1D1	T1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM1D is a special function register (SFR) to set the value to be compared with the timer n counter register (TM1C) value.

[Note]
Set TM1D when the timer stops(when T1STAT bit of TMSTAT0 register is “0”).
When “00H” is written in TM1D, TM1D is set to “01H”.

8.2.4 Timer 0 Counter Register (TM0C)

Address: 0F308H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0C	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM0C is performed, TM0C is set to “00H”. The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TM0C or high-order TM1C, both the low-order and the high-order are set to “0000H”.

During timer operation, the contents of TM0C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TM0C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-1 TM0C Read Enable/Disable during Timer Operation

Timer clock T0CK	System clock SYSCLK	TM0C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM0C twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

8.2.5 Timer 1 Counter Register (TM1C)

Address: 0F309H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1C	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM1C is performed, TM0C is set to “00H”. The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TM0C or high-order TM1C, both the low-order and the high-order are set to “0000H”.

During timer operation, the contents of TM1C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TM1C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-2 TM1C Read Enable/Disable during Timer Operation

Timer clock T1CK	System clock SYSCLK	TM1C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM1C twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

8.2.6 Timer 0 Control Register

Address: 0F320H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON	T0OST	T01M16	T0DIV2	T0DIV1	T0DIV0	—	—	T0CS0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON is a special function register (SFR) to control timer 0.
Write the TM0CON after clearing the TM0C when the timer stops(when the T0STAT bit of TMSTAT0 register is “0”).

[Description of Bits]

- **T0OST** (bit 7)
  The T0OST bit is used for selecting a normal timer mode or a one-shot timer mode. When the T0OST bit is set to “1”, timer 0 is selected as a one-shot timer mode.

T0OST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **T01M16** (bit 6)
  The T01M16 bit is used for selecting a 8-bit timer mode or a 16-bit timer mode. When the T01M16 bit is set to “1”, timer 0 and timer 1 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 1 is incremented by a timer 0 overflow signal. At that time, the timer 0 interrupt (TM0INT) is not generated.

T01M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **T0DIV2 to T0DIV0** (bit 5 to 3)
  T0DIV2 ~ T0DIV0 bits determines dividing rate of operation clock .
  The timer 0 works with the divided clock in 8bit timer mode.

TnDIV2	TnDIV1	TnDIV0	Description
0	0	0	Clock selected by T0CS0 bit (initial value)
0	0	1	Clock selected by T0CS0 bit divide by 2
0	1	0	Clock selected by TnCS0 bit divide by 4
0	1	1	Clock selected by TnCS0 bit divide by 8
1	0	0	Clock selected by TnCS0 bit divide by 16
1	0	1	Clock selected by TnCS0 bit divide by 32
1	1	0	Clock selected by TnCS0 bit divide by 64
1	1	1	Do not use (Clock selected by T0CS0 bit)

- **T0CS0** (bit 0)
  The T0CS0 bits is used for selecting the operation clock of timer 0.

T0CS0	Description
0	LSCLK (initial value)
1	OSCLK

8.2.7 Timer 1 Control Register

Address: 0F321H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON	T1OST	—	T1DIV2	T1DIV1	T1DIV0	—	—	T10CS0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON is a special function register (SFR) to control timer 1.
Write the TM1CON after clearing the TM1C when the timer stops(when the T1STAT bit of TMSTAT0 register is “0”).

[Description of Bits]

- **T1OST** (bit 7)
  The T1OST bit is used for selecting a normal timer mode or a one-shot timer mode. When the T1OST bit is set to “1”, timer 1 is selected as a one-shot timer mode.

T1OST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **T1DIV2 to T1DIV0** (bit 5 to 3)
  T1DIV2 ~ T1DIV0 bits determines dividing rate of operation clock .
  The timer 1 works with the divided clock in 8bit timer mode.

TnDIV2	TnDIV1	TnDIV0	Description
0	0	0	Clock selected by T0CS1 bit (initial value)
0	0	1	Clock selected by T0CS1 bit divide by 2
0	1	0	Clock selected by TnCS1 bit divide by 4
0	1	1	Clock selected by TnCS1 bit divide by 8
1	0	0	Clock selected by TnCS1 bit divide by 16
1	0	1	Clock selected by TnCS1 bit divide by 32
1	1	0	Clock selected by TnCS1 bit divide by 64
1	1	1	Do not use (Clock selected by T0CS1 bit)

- **T1CS0** (bit 0)
  The T1CS0 bits is used for selecting the operation clock of timer 1.
  When 16bit timer mode is selected (when T01M16 bit of TM0CON is “1”), data in T0CS0 bit has priority.

T1CS0	Description
0	LSCLK (initial value)
1	OSCLK

8.2.8 Timer Start Register 0 (TMSTR0)

Address: 0F330H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTR0	—	—	—	—	—	—	T1RUN	T0RUN
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMSTR0 is a special function register (SFR) to control starting the count-up of timer 0 and timer 1.

[Description of Bits]

- **T1RUN** (bit 1)
  T1RUN bit controls starting the Timer 1.
  In 8bit timer mode, the timer 1 starts counting up by setting the T1RUN bit to "1".
  In 16bit timer mode, setting the T1RUN bit is invalid and the timer 1 counts up by overflow signal of timer 0.

T1RUN	Description
0	Keep current status (initial)
1	Start count

- **T0RUN** (bit 0)
  T0RUN bit controls starting the Timer 0.
  In 8bit timer mode and 16bit timer mode, the timer 0 starts counting up by setting the T0RUN bit to "1".

T0RUN	Description
0	Keep current status (initial)
1	Start count

8.2.9 Timer Stop Register 0 (TMSTP0)

Address: 0F332H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTP0	—	—	—	—	—	—	T1STP	T0STP
R/W	RW	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMSTP0 is a special function register (SFR) to control stopping the count-up of timer 0 and timer 1.

[Description of Bits]

- **T1STP** (bit 1)
  T1STP bit controls stopping the Timer 1.
  In 8bit timer mode, the timer 1 stops counting up by setting the T1STP bit to "1".
  In 16bit timer mode, setting the T1STP bit is invalid and the timer stops the count-up by setting T0STP bit to "1".
  The timer stops at intial state after power on. Setting to the T1STP is invalid while the counter stops.

T1STP	Description
0	Keep current status (initial)
1	Stop count

- **T0STP** (bit 0)
  T0STP bit controls stopping the Timer 0.
  In 8bit timer mode and 16bit timer mode, the timer stops counting up by setting the T0STP bit to "1".
  The timer stops at intial state after power on. Setting to the T0STP is invalid while the counter stops.

T0STP	Description
0	Keep current status (initial)
1	Stop count

8.2.10 Timer Status Register 0 (TMSTAT0)

Address: 0F334H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTAT0	—	—	—	—	—	—	T1STAT	T0STAT
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

TMSTAT0 is a special function register (SFR) that shows the status of timer 0 and timer 1.

[Description of Bits]

- **T1STAT** (bit 1)
  T1STAT bit indicate status of timer 1(counting/stopping) in 8-bit timer mode. “0” is read in 16-bit timer mode.

T1STAT	Description
0	Stopping
1	counting

- **T0STAT** (bit 0)
  T0STAT bit indicate status of timer 0(counting/stopping) in 8-bit timer mode and 16-bit timer mode.

T0STAT	Description
0	Stopping
1	counting

8.3 Description of operation

The timer counters(TMnC) starts the falling edge of the timer clock(TnCK) that are selected by the Timer control register(TMnCON) when the TnRUN bit of timer n register0(TMSTR0) are set to 1.
When the count value of TMnC and the timer data register (TMnD) coincide, timer interrupt (TMnINT) occurs on the next timer clock falling edge, TMnC are reset to “00H” and incremental counting continues.

When the TnSTP bits are set to “1”, TMnC stop counting after counting once the falling of the timer clock (TnCK) and timer status regoster 0(TMSTAT0) TnSTAT bit becomes “0”.

When the TnRUN bits are set to “1” again, TMnC restart incremental counting from the previous values. To initialize TMnC to “00H”, perform write operation in TMnC.

The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n=0\sim1)$$

TMnD: Timer 0 to 1 data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 0 to 1 control register 0 (TMnCON)

After TnRUN bit are set to "1", timer counter are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 8-2 shows the normal timer mode operation timing diagram of Timer 0 to 1

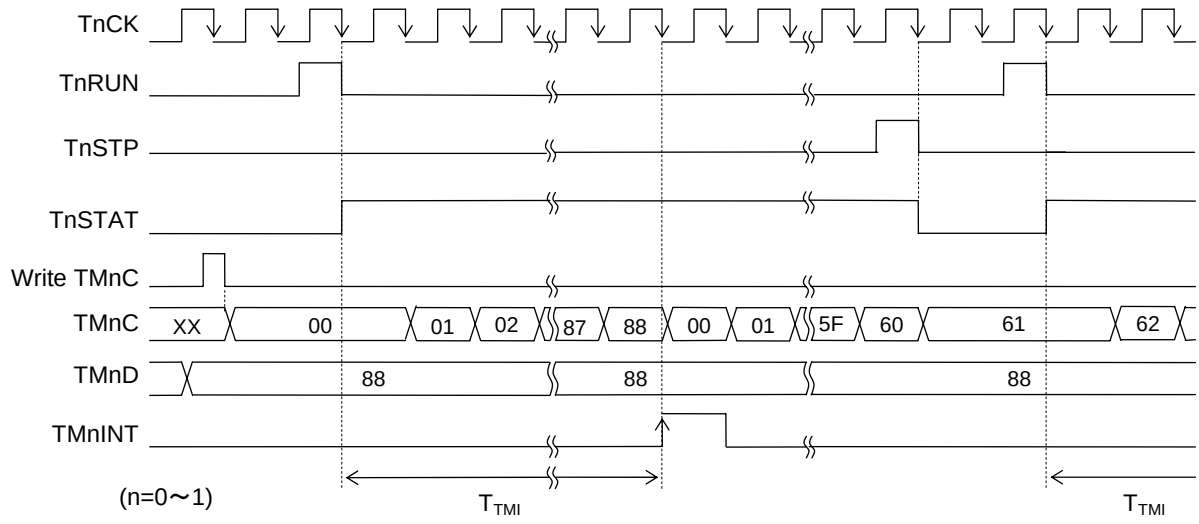


Figure 8-2 Normal Timer Mode Operation Timing Diagram of Timer 0 to 1

[Note]
Even if “1” is written to the TnSTP bit, counting operation continues up to the falling edge of the next timer clock pulse(the timer 0 to 1 status flag TnSTA is in a “1” state). Therefore, the timer 0 to 1 interrupt (TMnINT) may occur.

Figure 8-3 shows the one-shot timer mode operation timing diagram

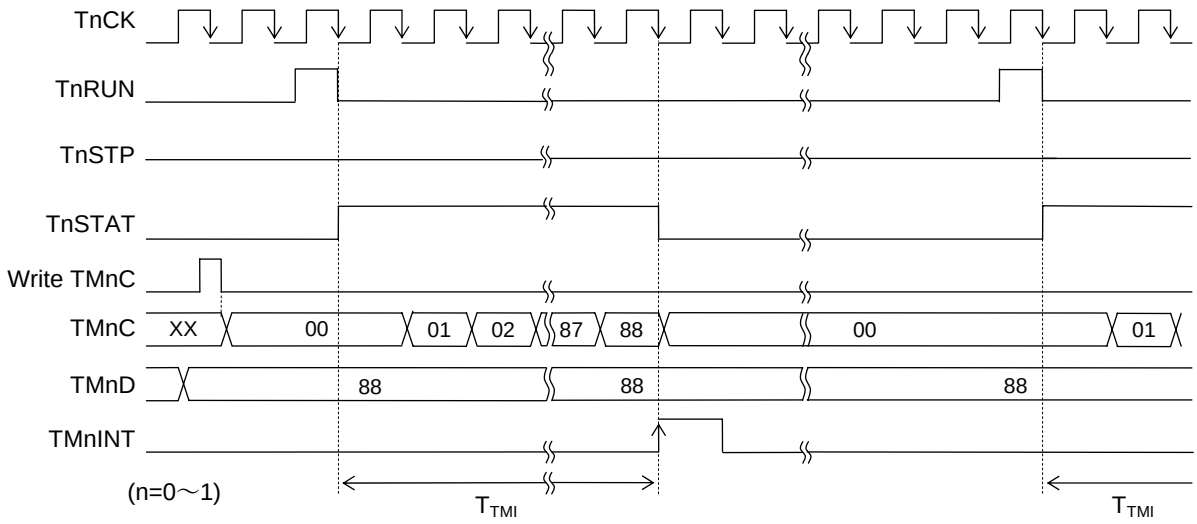


Figure 8-3 One-Shot Timer Mode Operation Timing Diagram

[Note]
TnSTAT bit is automatically cleared when the data of TMnC and TMnD matches.

Chapter 9 16bit Timer

9 16bit Timer

9.1 General Description

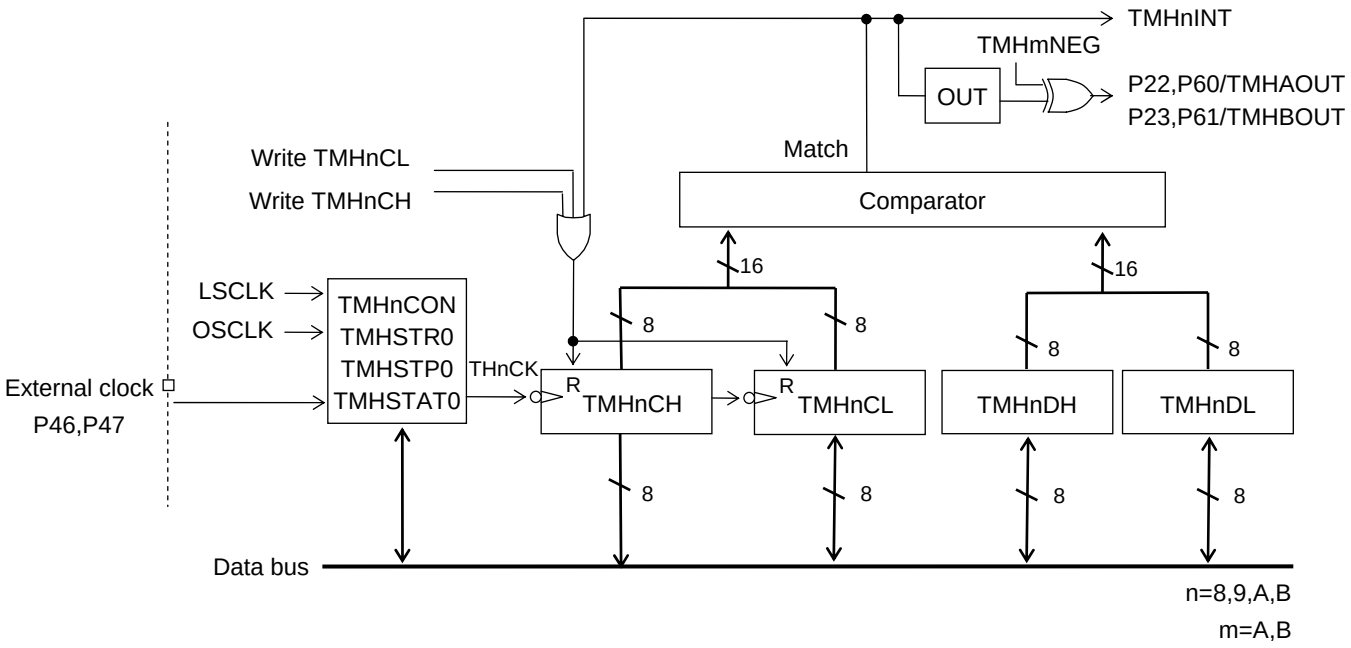
This LSI includes four channels of 16-bit timers.
For the input clock, see Chapter 6, “Clock Generation Circuit”.

9.1.1 Features

- The timer interrupt (TMnINT, n=0 to 7) is generated when the values of timer counter register (TMHnCH,TMHnCL n=8,9,A,B) and timer data register (TMHnDH,TMHnDL) coincide.
- Low-speed clock (LSCLK) or high-speed clock (OSCLK) is selectable for the timer clock.
- Dividing of the timer clock is selectable(1/2, 1/4, 1/8, 1/16 1/32 and 1/64).
- Timer outputs (TMHAOUT, TMHBOUT) are available.
- Auto-reload timer mode or one shot timer mode is selectable.

9.1.2 Configuration

Figure 9-1 show the configuration of the timer.



TMHnCON	：16bit timer control register
TMHSTR0	：16bit timer start register 0
TMHSTP0	：16bit timer stop register 0
TMHSTAT0	：16bit timer status register 0
TMHnDH、TMHnDL	：16bit timer data register
TMHnCH、TMHnCL	：16bit timer counter register

Figure 9-1 Configuration of 16bit timer (Timer 8, 9, A,B)

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F340H	16bit timer 8 data register L	TMH8DL	TMH8D	R/W	8	0FFH
0F341H	16bit timer 8 data register H	TMH8DH		R/W	8/16	0FFH
0F342H	16bit timer 9 data register L	TMH9DL	TMH9D	R/W	8	0FFH
0F343H	16bit timer 9 data register H	TMH9DH		R/W	8/16	0FFH
0F344H	16bit timer A data register L	TMHADL	TMHAD	R/W	8	0FFH
0F345H	16bit timer A data register H	TMHADH		R/W	8/16	0FFH
0F346H	16bit timer B data register L	TMHBDL	TMHBD	R/W	8	0FFH
0F347H	16bit timer B data register H	TMHBDH		R/W	8/16	0FFH
0F350H	16bit timer 8 counter register L	TMH8CL	TMH8C	R/W	8	00H
0F351H	16bit timer 8 counter register H	TMH8CH		R/W	8/16	00H
0F352H	16bit timer 9 counter register L	TMH9CL	TMH9C	R/W	8	00H
0F353H	16bit timer 9 counter register H	TMH9CH		R/W	8/16	00H
0F354H	16bit timer A counter register L	TMHACL	TMHAC	R/W	8	00H
0F355H	16bit timer A counter register H	TMHACH		R/W	8/16	00H
0F356H	16bit timer B counter register L	TMHBCL	TMHBC	R/W	8	00H
0F357H	16bit timer B counter register H	TMHBCH		R/W	8/16	00H
0F360H	16bit timer 8 control register	TMH8CON	—	R/W	8	00H
0F361H	Reserve	—	—	—	—	—
0F362H	16bit timer 9 control register	TMH9CON	—	R/W	8	00H
0F363H	Reserve	—	—	—	—	—
0F364H	16bit timer A control register	TMHACON	—	R/W	8	00H
0F365H	Reserve	—	—	—	—	—
0F366H	16bit timer B control register	TMHBCON	—	R/W	8	00H
0F367H	Reserve	—	—	—	—	—
0F370H	16bit timer start register 0	TMHSTR0	—	R/W	8	00H
0F372H	16bit timer stop register 0	TMHSTP0	—	R/W	8	00H
0F374H	16bit timer status register 0	TMHSTAT0	—	R/W	8	00H

9.2.2 16bit timer 8 data register L,H (TMH8DL,H)

Address: 0F340H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMH8DL	TH8D7	TH8D6	TH8D5	TH8D4	TH8D3	TH8D2	TH8D1	TH8D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F341H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMH8DH	TH8D15	TH8D14	TH8D13	TH8D12	TH8D11	TH8D10	TH8D9	TH8D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMH8DL,H is a special function register (SFR) to set the value to be compared with the 16bit timer 8 counter register L, H(TMH8CL,H) value.

[Note]
Set TMH8DL, H when the 16bit timer 8 stops(when TH8STAT bit of TMHSTAT0 register is “0”).
When “0000H” is written to TMH8DL, H, TMH8DL, H is set to “0001H”.

9.2.3 16bit timer 9 data register L,H (TMH9DL,H)

Address: 0F342H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMH9DL	TH9D7	TH9D6	TH9D5	TH9D4	TH9D3	TH9D2	TH9D1	TH9D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F343H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMH9DH	TH9D15	TH9D14	TH9D13	TH9D12	TH9D11	TH9D10	TH9D9	TH9D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMH9DL,H is a special function register (SFR) to set the value to be compared with the 16bit timer 9 counter register L, H(TMH9CL,H) value.

[Note]
Set TMH9DL, H when the 16bit timer 8 stops(when TH9STAT bit of TMHSTAT0 register is “0”).
When “0000H” is written to TMH9DL, H, TMH9DL, H is set to “0001H”.

9.2.4 16bit timer A data register L,H (TMHADL,H)

Address: 0F344H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMHADL	THAD7	THAD6	THAD5	THAD4	THAD3	THAD2	THAD1	THAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F345H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMHADH	THAD15	THAD14	THAD13	THAD12	THAD11	THAD10	THAD9	THAD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMHADL,H is a special function register (SFR) to set the value to be compared with the 16bit timer A counter register L, H(TMHACL,H) value.

[Note]
Set TMHADL, H when the 16bit timer 8 stops(when THASTAT bit of TMHSTAT0 register is “0”).
When “0000H” is written to TMHADL, H, TMHADL, H is set to “0001H”.

9.2.5 16bit timer B data register L,H (TMHBDL,H)

Address: 0F346H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMHBDL	THBD7	THBD6	THBD5	THBD4	THBD3	THBD2	THBD1	THBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F347H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMHBDH	THBD15	THBD14	THBD13	THBD12	THBD11	THBD10	THBD9	THBD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMHBDL,H is a special function register (SFR) to set the value to be compared with the 16bit timer B counter register L, H(TMHBCL,H) value.

[Note]
Set TMHBDL, H when the 16bit timer 8 stops(when THBSTAT bit of TMHSTAT0 register is “0”).
When “0000H” is written to TMHBDL, H, TMHBDL, H is set to “0001H”.

9.2.6 16bit timer 8 counter register L,H (TMH8CL,H)

Address: 0F350H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH8CL	TH8C7	TH8C6	TH8C5	TH8C4	TH8C3	TH8C2	TH8CH	TH8CL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F351H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH8CH	TH8C15	TH8C14	TH8C13	TH8C12	TH8C11	TH8C10	TH8C9	TH8C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMH8CL,H is a special function register (SFR) that functions as an 16-bit binary counter.
If write operation is performed to either the low-order TMH8CL or high-order TMH8CH, both the low-order and the high-order are set to “0000H”. The written data is meaningless.
During timer operation, the contents of TMH8CL,H may not be read depending on the conditions of the timer clock and the system clock.
Table 9-1 shows whether reading TMH8CL,H is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-1 TMH8CL,H Read Enable/Disable during Timer Operation

Timer clock TH8CK	System clock SYSCLK	TMH8CL,H read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMH8CL,H twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

9.2.7 16bit timer 9 counter register L,H (TMH9CL,H)

Address: 0F352H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH9CL	TH9C7	TH9C6	TH9C5	TH9C4	TH9C3	TH9C2	TH9CH	TH9CL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F353H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH9CH	TH9C15	TH9C14	TH9C13	TH9C12	TH9C11	TH9C10	TH9C9	TH9C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMH9CL,H is a special function register (SFR) that functions as an 16-bit binary counter.
If write operation is performed to either the low-order TMH9CL or high-order TMH9CH, both the low-order and the high-order are set to “0000H”. The written data is meaningless.
During timer operation, the contents of TMH9CL,H may not be read depending on the conditions of the timer clock and the system clock.
Table 9-1 shows whether reading TMH9CL,H is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-1 TMH9CL,H Read Enable/Disable during Timer Operation

Timer clock TH9CK	System clock SYSCLK	TMH9CL,H read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMH9CL,H twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

9.2.8 16bit timer A counter register L,H (TMHACL,H)

Address: 0F354H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHACL	THAC7	THAC6	THAC5	THAC4	THAC3	THAC2	THACH	THACL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F355H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHACH	THAC15	THAC14	THAC13	THAC12	THAC11	THAC10	THAC9	THAC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMHACL,H is a special function register (SFR) that functions as an 16-bit binary counter.
If write operation is performed to either the low-order TMHACL or high-order TMHACH, both the low-order and the high-order are set to “0000H”. The written data is meaningless.
During timer operation, the contents of TMHACL,H may not be read depending on the conditions of the timer clock and the system clock.
Table 9-1 shows whether reading TMHACL,H is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-1 TMHACL,H Read Enable/Disable during Timer Operation

Timer clock THACK	System clock SYSCLK	TMHACL,H read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMHACL,H twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

9.2.9 16bit timer B counter register L,H (TMHBCL,H)

Address: 0F356H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHBCL	THBC7	THBC6	THBC5	THBC4	THBC3	THBC2	THBCH	THBCL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F357H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHBCH	THBC15	THBC14	THBC13	THBC12	THBC11	THBC10	THBC9	THBC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMHBCL,H is a special function register (SFR) that functions as an 16-bit binary counter.
If write operation is performed to either the low-order TMHBCL or high-order TMHBCH, both the low-order and the high-order are set to “0000H”. The written data is meaningless.
During timer operation, the contents of TMHBCL,H may not be read depending on the conditions of the timer clock and the system clock.
Table 9-1 shows whether reading TMHBCL,H is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-1 TMHBCL,H Read Enable/Disable during Timer Operation

Timer clock THBCK	System clock SYSCLK	TMHBCL,H read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TMHBCL,H twice until the last data coincides the previous data.
OSCLK	LSCLK	Read disabled
OSCLK	HSCLK	Read enabled

9.2.10 16bit timer 8 control register (TMH8CON)

Address: 0F360H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH8CON	TH8OST	—	TH8DIV2	TH8DIV1	TH8DIV0	—	TH8CS1	TH8CS0
R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMH8CON is a special function (SFR) to control the 16bit timer 8.
Write the TMH8CON after clearing the TMH8CON when the timer stops(when the TH8STAT bit of TMHSTAT0 register is “0”).

[Description of Bits]

- **TH8OST** (bit 7)
  The TH8OST bit is used for selecting a normal timer mode or a one-shot timer mode. When the TH8OST bit is set to “1”, timer 8 works in the one-shot timer mode.

TH8OST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **TH8DIV2~TH8DIV0** (bit 5 to 3)
  TH8DIV2~TH8DIV bits determine dividing rate of operation clock .

TH8DIV2	TH8DIV1	TH8DIV0	Description
0	0	0	Clock selected by TH8CS1~TH8CS0 bit (initial value)
0	0	1	Clock selected by TH8CS1~TH8CS0 bit divide by 2
0	1	0	Clock selected by TH8CS1~TH8CS0 bit divide by 4
0	1	1	Clock selected by TH8CS1~TH8CS0 bit divide by 8
1	0	0	Clock selected by TH8CS1~TH8CS0 bit divide by 16
1	0	1	Clock selected by TH8CS1~TH8CS0 bit divide by 32
1	1	0	Clock selected by TH8CS1~TH8CS0 bit divide by 64
1	1	1	Do not use (Clock selected by TH8CS1~TH8CS0 bit)

- **TH8CS1~TH8CS0** (bit 1 to 0)
  The TH8CS1~TH8CS0 bits are used for selecting the operation clock of timer 8. One of LSCLK, OSCLK or the external clock (supplied from P46) is selectable.

TH8CS1	TH8CS0	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use (LSCLK)
1	1	External clock (supplied from P46)

9.2.11 16bit timer 9 control register (TMH9CON)

Address: 0F362H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMH9CON	TH9OST	—	TH9DIV2	TH9DIV1	TH9DIV0	—	TH9CS1	TH9CS0
R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMH9CON is a special function (SFR) to control the 16bit timer 9.
Write the TMH9CON after clearing the TMH9CON when the timer stops(when the TH9STAT bit of TMHSTAT0 register is “0”).

[Description of Bits]

- **TH9OST** (bit 7)
  The TH9OST bit is used for selecting a normal timer mode or a one-shot timer mode. When the TH9OST bit is set to “1”, timer 8 works in the one-shot timer mode.

TH9OST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **TH9DIV2~TH9DIV0** (bit 5 to 3)
  TH9DIV2~TH9DIV bits determine dividing rate of operation clock .

TH9DIV2	**TH9DIV1**	**TH9DIV0**	Description
0	0	0	Clock selected by TH9CS1~TH9CS0 bit (initial value)
0	0	1	Clock selected by TH9CS1~TH9CS0 bit divide by 2
0	1	0	Clock selected by TH9CS1~TH9CS0 bit divide by 4
0	1	1	Clock selected by TH9CS1~TH9CS0 bit divide by 8
1	0	0	Clock selected by TH9CS1~TH9CS0 bit divide by 16
1	0	1	Clock selected by TH9CS1~TH9CS0 bit divide by 32
1	1	0	Clock selected by TH9CS1~TH9CS0 bit divide by 64
1	1	1	Do not use (Clock selected by TH9CS1~TH9CS0 bit)

- **TH9CS1~TH9CS0** (bit 1 to 0)
  The TH9CS1~TH9CS0 bits are used for selecting the operation clock of timer 8. One of LSCLK, OSCLK or the external clock (supplied from P46) is selectable.

TH9CS1	**TH9CS0**	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use (LSCLK)
1	1	External clock (supplied from P46)

9.2.12 16bit timer A control register (TMHACON)

Address: 0F364H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHACON	THAOST	THANEG	THADIV2	THADIV1	THADIV0	—	THACS1	THACS0
R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMHACON is a special function (SFR) to control the 16bit timer A.
Write the TMHACON after clearing the TMHACON when the timer stops(when the THASTAT bit of TMHSTAT0 register is "0").

[Description of Bits]

- **THAOST** (bit 7)
  The THAOST bit is used for selecting a normal timer mode or a one-shot timer mode. When the THAOST bit is set to "1", timer 8 works in the one-shot timer mode.

THAOST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **THANEG** (bit 6)
  The THANEG bit is used for selecting the logic of output signal TMHAOUT. When the THANEG bit is "0", the initial logic of TMHAOUT is "0"

THANEG	Description
0	Positive logic (initial value)
1	Negative logic

- **THADIV2~THADIV0** (bit 5 to 3)
  THADIV2~THADIV bits determine dividing rate of operation clock .

THADIV2	**THADIV1**	**THADIV0**	Description
0	0	0	Clock selected by THACS1~THACS0 bit (initial value)
0	0	1	Clock selected by THACS1~THACS0 bit divide by 2
0	1	0	Clock selected by THACS1~THACS0 bit divide by 4
0	1	1	Clock selected by THACS1~THACS0 bit divide by 8
1	0	0	Clock selected by THACS1~THACS0 bit divide by 16
1	0	1	Clock selected by THACS1~THACS0 bit divide by 32
1	1	0	Clock selected by THACS1~THACS0 bit divide by 64
1	1	1	Do not use (Clock selected by THACS1~THACS0 bit)

- **THACS1~THACS0** (bit 1 to 0)
  The THACS1~THACS0 bits are used for selecting the operation clock of timer 8. One of LSCLK, OSCLK or the external clock (supplied from P46) is selectable.

THACS1	**THACS0**	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use (LSCLK)
1	1	External clock (supplied from P46)

9.2.13 16bit timer B control register (TMHBCON)

Address: 0F366H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHBCON	THBOST	THBNEG	THBDIV2	THBDIV1	THBDIV0	—	THBCS1	THBCS0
R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMHBCON is a special function (SFR) to control the 16bit timer B.
Write the TMHBCON after clearing the TMHBCON when the timer stops(when the THBSTAT bit of TMHSTAT0 register is “0”).

[Description of Bits]

- **THBOST** (bit 7)
  The THBOST bit is used for selecting a normal timer mode or a one-shot timer mode. When the THBOST bit is set to “1”, timer 8 works in the one-shot timer mode.

THBOST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **THBNEG** (bit 6)
  The THBNEG bit is used for selecting the logic of output signal TMHBOUT. When the THBNEG bit is “0”, the initial logic of TMHBOUT is “0”

THBNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **THBDIV2~THBDIV0** (bit 5 to 3)
  THBDIV2~THBDIV bits determine dividing rate of operation clock .

THBDIV2	**THBDIV1**	**THBDIV0**	Description
0	0	0	Clock selected by THBCS1~THBCS0 bit (initial value)
0	0	1	Clock selected by THBCS1~THBCS0 bit divide by 2
0	1	0	Clock selected by THBCS1~THBCS0 bit divide by 4
0	1	1	Clock selected by THBCS1~THBCS0 bit divide by 8
1	0	0	Clock selected by THBCS1~THBCS0 bit divide by 16
1	0	1	Clock selected by THBCS1~THBCS0 bit divide by 32
1	1	0	Clock selected by THBCS1~THBCS0 bit divide by 64
1	1	1	Do not use (Clock selected by THBCS1~THBCS0 bit)

- **THBCS1~THBCS0** (bit 1 to 0)
  The THBCS1~THBCS0 bits are used for selecting the operation clock of timer 8. One of LSCLK, OSCLK or the external clock (supplied from P46) is selectable.

THBCS1	**THBCS0**	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use (LSCLK)
1	1	External clock (supplied from P46)

9.2.14 16bit timer start register 0 (TMHSTR0)

Address: 0F370H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHSTR0	—	—	—	—	THBRUN	THARUN	TH9RUN	TH8RUN
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMHSTR0 is a special function (SFR) to control starting count of 16bit timer 8, 9, A and B.

[Description of Bits]

- **THBRUN** (bit 3)
  THBRUN bit controls starting the timer B.
  The timer B starts counting up by setting the THBRUN bit to "1".

THBRUN	Description
0	Keep current status (initial)
1	Stop count

- **THARUN** (bit 2)
  THARUN bit controls starting the timer A.
  The timer A starts counting up by setting the THARUN bit to "1".

THARUN	Description
0	Keep current status (initial)
1	Stop count

- **TH9RUN** (bit 1)
  TH9RUN bit controls starting the timer 9.
  The timer 9 starts counting up by setting the TH9RUN bit to "1".

TH9RUN	Description
0	Keep current status (initial)
1	Stop count

- **TH8RUN** (bit 0)
  TH8RUN bit controls starting the timer 8.
  The timer 8 starts counting up by setting the TH8RUN bit to "1".

TH8RUN	Description
0	Keep current status (initial)
1	Stop count

9.2.15 16bit timer stop register 0 (TMHSTP0)

Address: 0F372H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHSTP0	—	—	—	—	THBSTP	THASTP	TH9STP	TH8STP
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMHSTR0 is a special function (SFR) to control stopping count of 16bit timer 8, 9, A and B.

[Description of Bits]

- **THBSTP** (bit 3)
  THBSTP bit controls stopping the timer B.
  The timer B stops counting up by setting the THBSTP bit to "1".
  The timer stops at intial state after power on. Setting to the THBSTP is invalid while the counter stops.

THBSTP	Description
0	Keep current status (initial)
1	Stop count

- **THASTP** (bit 2)
  THASTP bit controls stopping the timer A.
  The timer A stops counting up by setting the THASTP bit to "1".
  The timer stops at intial state after power on. Setting to the THASTP is invalid while the counter stops.

THASTP	Description
0	Keep current status (initial)
1	Stop count

- **TH9STP** (bit 1)
  TH9STP bit controls stopping the timer 9.
  The timer 9 stops counting up by setting the TH9STP bit to "1".
  The timer stops at intial state after power on. Setting to the TH9STP is invalid while the counter stops.

TH9STP	Description
0	Keep current status (initial)
1	Stop count

- **TH8STP** (bit 0)
  THASTP bit controls stopping the timer 8.
  The timer 8 stops counting up by setting the TH8STP bit to "1".
  The timer stops at intial state after power on. Setting to the TH8STP is invalid while the counter stops.

TH8STP	Description
0	Keep current status (initial)
1	Stop count

9.2.16 16bit timer status register 0 (TMHSTAT0)

Address: 0F374H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMHSTAT0	—	—	—	—	THBSTAT	THASTAT	TH9STAT	TH8STAT
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

TMHSTAT0 is a special function (SFR) that shows status of 16bit timer 8, 9, A and B.

[Description of Bits]

- **THBSTAT** (bit 3)
  THBSTAT bit indicates the status of timer B(counting/stopping).

THBSTAT	Description
0	Stopping
1	counting

- **THASTAT** (bit 2)
  THASTAT bit indicates the status of timer A(counting/stopping).

THASTAT	Description
0	Stopping
1	counting

- **TH9STAT** (bit 1)
  TH9STAT bit indicates the status of timer 9(counting/stopping).

TH9STAT	Description
0	Stopping
1	counting

- **TH8STAT** (bit 0)
  TH8STAT bit indicates the status of timer 8(counting/stopping).

TH8STAT	Description
0	Stopping
1	counting

9.3 Description of operation

The timer counters(TMHnC) starts the falling edge of the timer clock(THnCK) that are selected by the Timer control register(TMHnCON) when the THnRUN bit of timer n register0(TMHSTR0) are set to 1.
When the count value of TMHnC and the timer data register (TMHnD) coincide, timer interrupt (TMHnINT) occurs on the next timer clock falling edge, TMHnC are reset to “0000H” and incremental counting continues.

When the THnSTP bits are set to “1”, TMHnC stop counting after counting once the falling of the timer clock (THnCK) and timer status regoster 0(TMHSTAT0) THnSTAT bit becomes “0”.

When the THnRUN bits are set to “1” again, THMnC restart incremental counting from the previous values. To initialize TMHnC to “0000H”, perform write operation in TMHnC.

The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMHnD + 1}{THnCK\ (Hz)} \quad (n=8,9,A,B)$$

TMHnD: Timer 8, 9, A, B data register (TMHnD) setting value (0001H to 0FFFFH)
THnCK: Clock frequency selected by the Timer 8, 9, A, B control register 0 (TMHnCON)

After THnRUN bit are set to "1", timer counter are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 9-2 shows the normal timer mode operation timing diagram of Timer 8, 9, A and B.

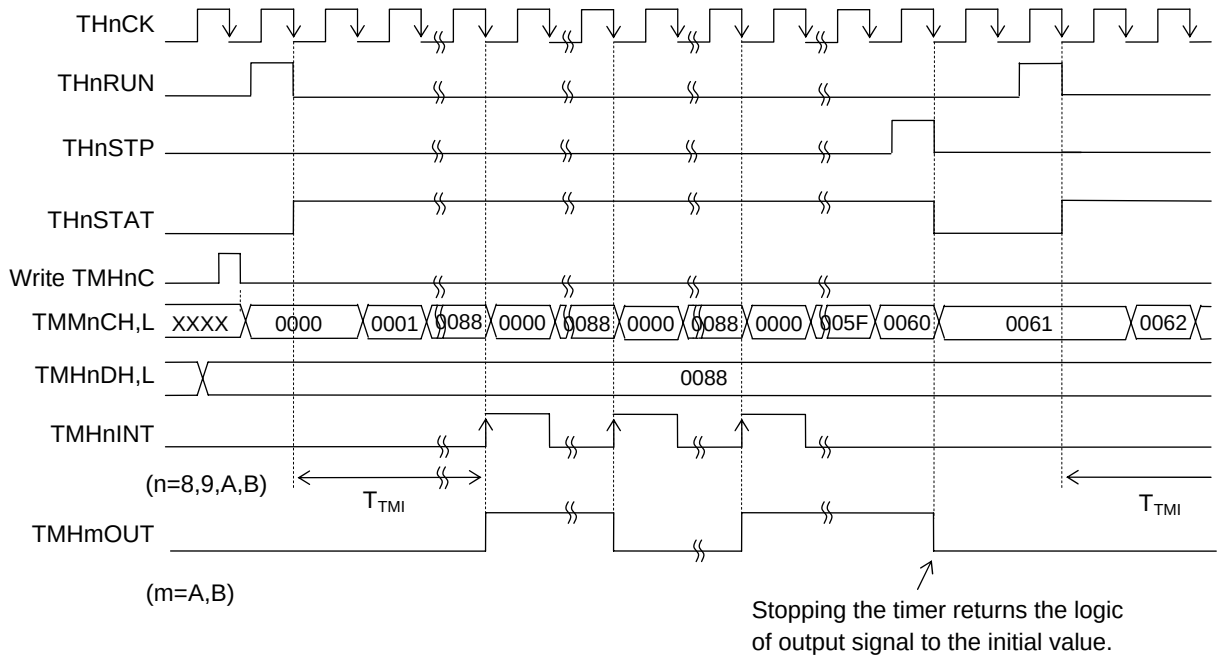


Figure 9-2 Normal Timer Mode Operation Timing Diagram of Timer 8, 9, A, B

[Note]
Even if “1” is written to the THnSTP bit, counting operation continues up to the falling edge of the next timer clock pulse(the timer 0 to 1 status flag THnSTA is in a “1” state). Therefore, the 16bit timer 8, 9, A and B interrupt (TMHnINT) may occur.

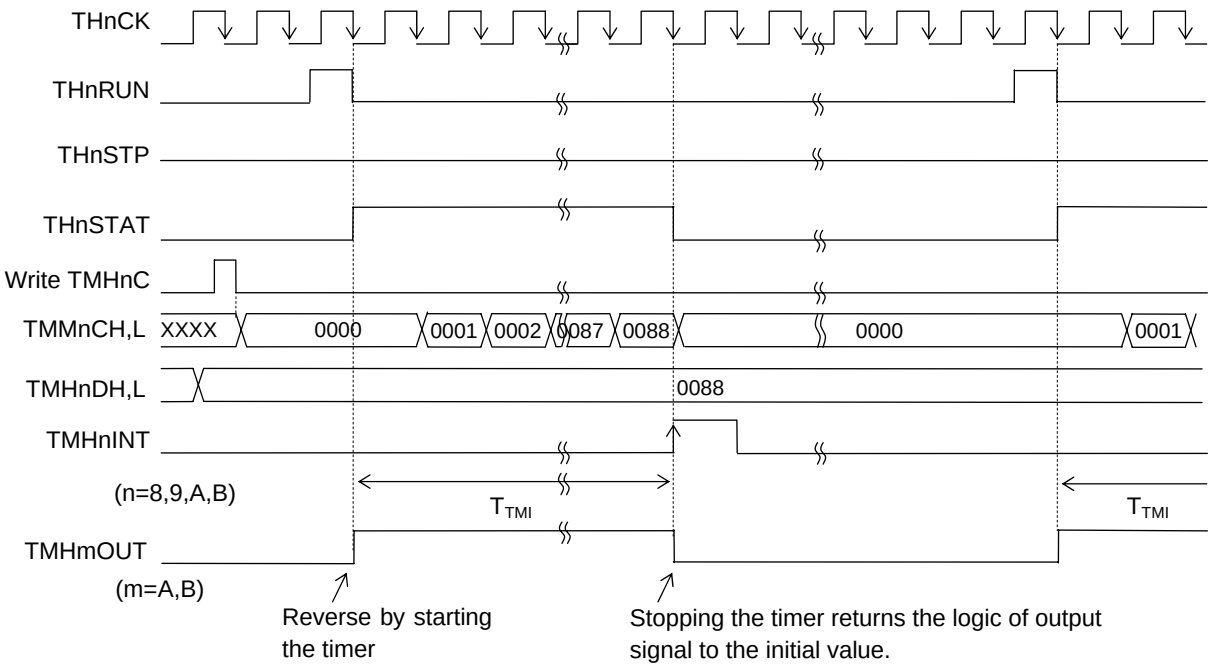


Figure 9-3 One-Shot Timer Mode Operation Timing Diagram

[Note]
TnSTAT bit is automatically cleared when the data of TMHnCH, L and TMHnDH, L matches.

Chapter 10 Watchdog Timer

10 Watchdog Timer

10.1 General Description

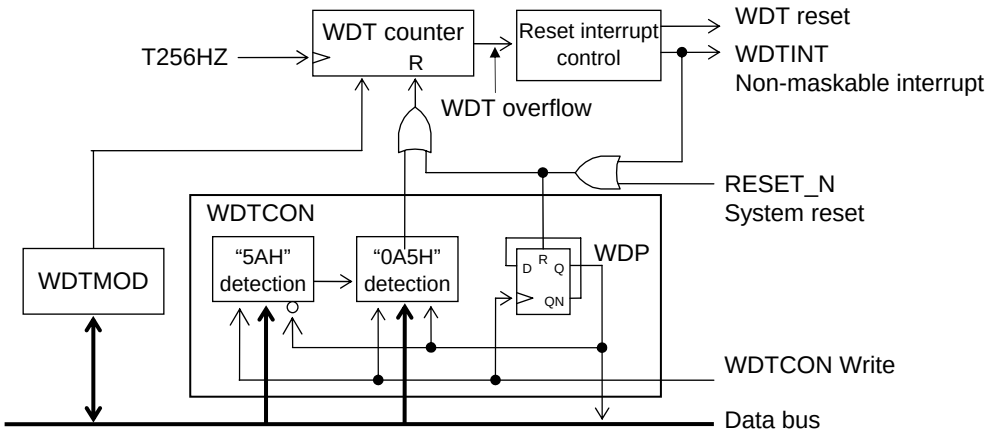
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, “Interrupts,” and for WDT interrupt see Chapter 3, “Reset Function”.

10.1.1 Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Requests a WDT interrupt (non-maskable interrupt) by the first overflow
- WDT reset generated by the second overflow

10.1.2 Configuration

Figure 10-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 10-1 Configuration of Watchdog Timer

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H

10.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to control the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. The WDP is reset to “0” at the system reset or Watch Dog Timer overflow and is inverted every writing to WDTCON.

- **d7-d0** (bits 7-0)
  This bit is used to write data to clear the WDT counter. If writing to the WDTCON, the WDP value is inverted.
  Write “5AH” on the condition of WDP is “0” and then write “0A5H” on the condition of WDP is “1”.Then WDT counter will be clear.

[Note]
When the WDT interrupt (WDTINT) occurs by the first WDT counter overflow, the counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.25us). During the time period that they are initialized, writing to WDTCON is disable and the logic of WDP does not change. Therefore, in the case of that you have program codes handle to clear the WDT when the first overflow WDT interrupt occurs and also the codes run at high-speed system clock, please check the WDP gets reversed after writing to WDTCON to see if the writing was surely successful. For example of the program code, see Section 10.3.1, "Handling example when not using the watch dog timer".

10.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: R/W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	—	—	—	—	—	—	WDT1	WDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT1-0** (bits 1-0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set a overflow period (T_{WOV}) of the WDT counter.

WDT1	WDT0	Description
0	0	125 ms
0	1	500 ms
1	0	2 s (initial value)
1	1	8 s

10.3 Description of operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to “0” at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (TWOV) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter (T_{WCL}) shown in Table 10-1.

Table 10-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125 ms	Approx. 121 ms
0	1	500 ms	Approx. 496 ms
1	0	2000 ms	Approx. 1996 ms
1	1	8000 ms	Approx. 7996 ms

Figure 10-2 shows an example of watchdog timer operation.

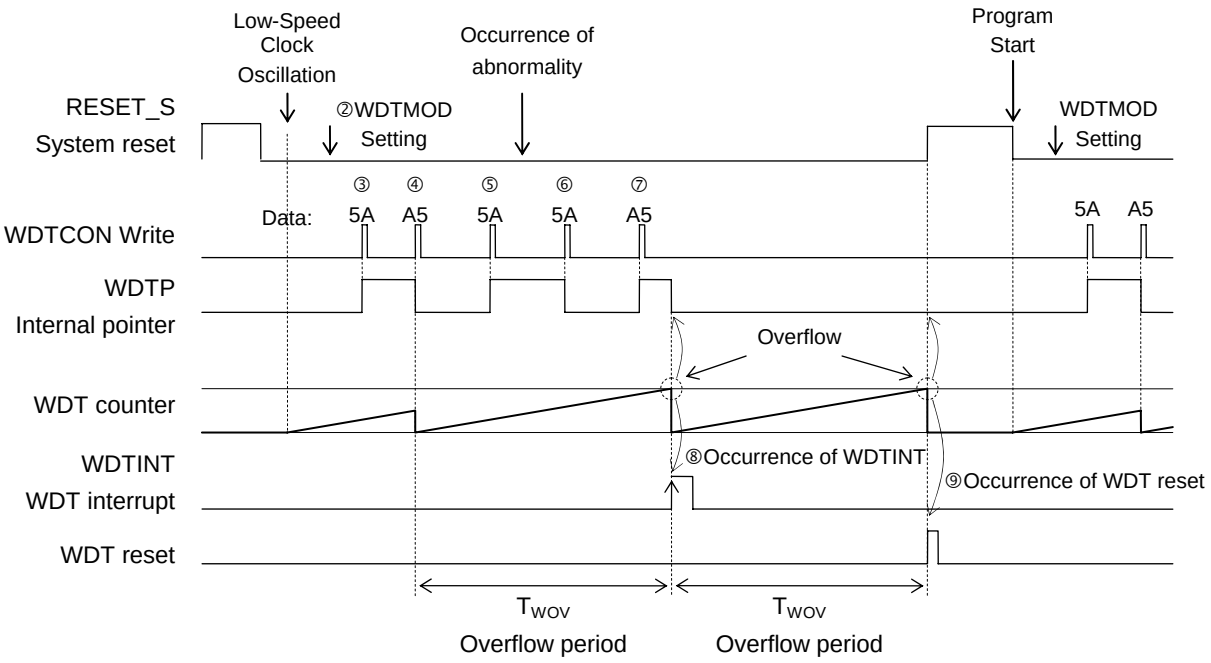


Figure 10-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
③ "5AH" is written to WDTCON. (Internal pointer 0 to 1)
④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1 to 0)
⑤ "5AH" is written to WDTCON. (Internal pointer 0 to 1)
⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1 to 0)
⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in . (Internal pointer 0 to 1)
⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case, the WDT counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.26us).
⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

[Note]
・In STOP mode, the watchdog timer operation also stops.
・In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
・The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

10.3.1 Handling example when not using the watch dog timer

WDT counter is a free-run counter that starts count-up automatically after the system reset released and the low-speed clock (LSCLK) starts oscillating. If the WDT counter gets overflow, the WDT non-maskable interrupt occurs and then a system reset occurs. Therefore, it is needed to clear the WDT counter even if you do not want to use the WDT as a fale-safe function.
See following example programming codes to clear the WDT counter in the interrupt routine.

Program example:

```
__DI();              // Disable interrupts

do {
WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;

__EI();
```

Chapter 11 PWM

11 PWM

11.1 General Description

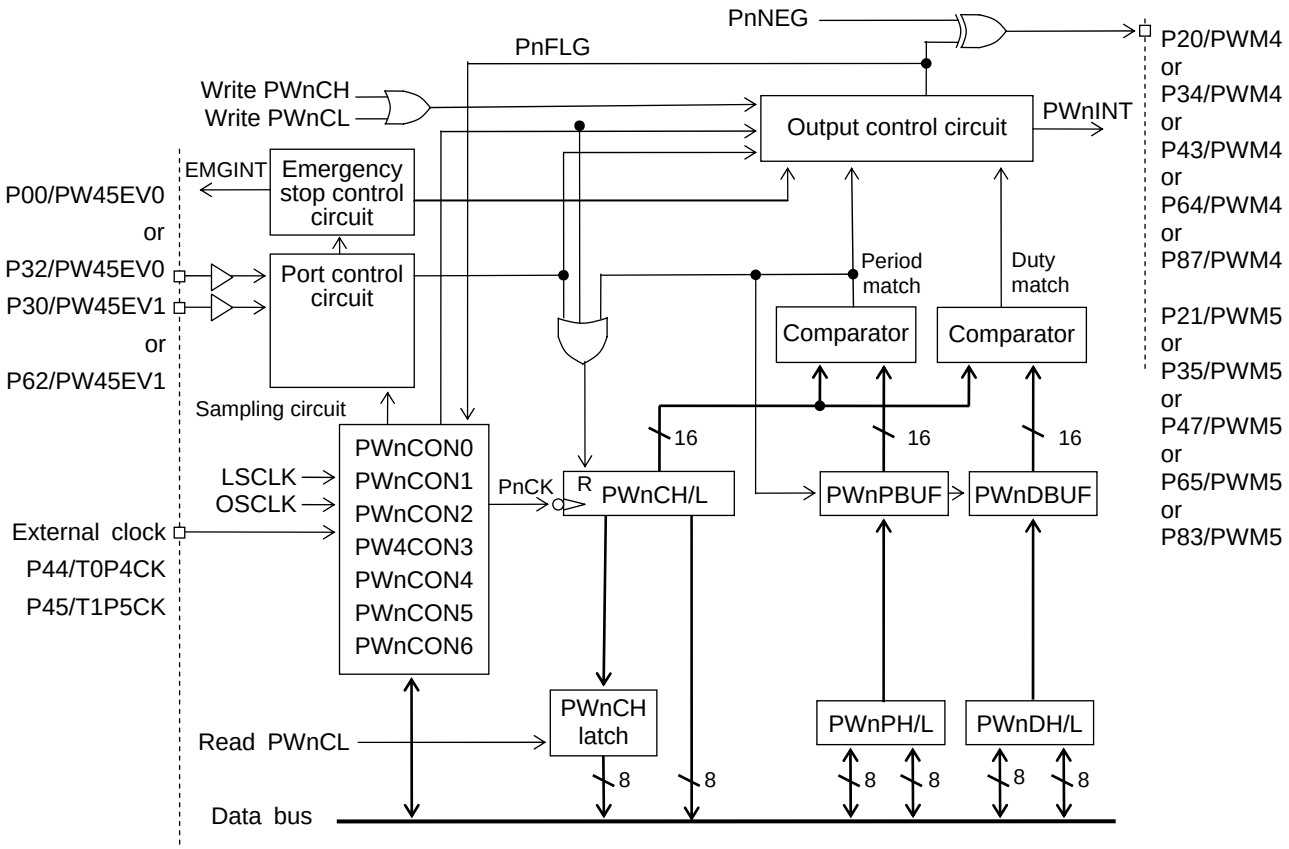
This LSI includes four channels of 16-bit PWM (Pulse Width Modulation).
The PWM4 output (PWM4) is assigned to P20(Port 2), P34(Port 3), P43(Port 4), P64(Port 6) and P87(Port 8) as the tertiary function.
The PWM5 output (PWM5) is assigned to P21(Port 2), P35(Port 3), P47(Port 4), P65(Port 6) and P83(Port 8) as the tertiary function.
The PWM6 output (PWM6) is assigned to P22(Port 2), P53(Port 5), P60(Port 6), P66(Port 6) and P70(Port 7) as the tertiary function.
The PWM7 output (PWM7) is assigned to P23(Port 2), P57(Port 5), P61(Port 6), and P71(Port 7) as the quaternary function.
For the functions of port 2, port 3, port 4, port 5, port 6, port 7 and port 8, see Chapter 17, “Port 2”, Chapter 18, “Port 3”, Chapter 19, “Port 4”, Chapter 20, “Port 5”, Chapter 22, “Port 7” and Chapter 23, “Port 8”.

11.1.1 Features

- The PWM signals with the periods of approximately 244 ns (@OSCLK=8.192MHz) to 2s (@LSCLK=32.768kHz) can be generated and output outside of the LSI.
- The output logic of the PWM signal can be switched to the positive or negative logic.
- At the coincidence of PWM signal period, duties, and period & duty, a PWM interrupt (PWnINT) occurs.
- Repeate mode / One shot mode (Auto-reload PWM mode /One shot PWM mode) is selectable.
- Low-speed clock (LSCLK), high-speed clock (OSCLK) or an external clock is selectable for the PWM clock.
- Dividing of the PWM clock is selectable(1/2, 1/4, 1/8, 1/16 1/32 and 1/64).
- PWM4 and PWM5 coupled mode with a specified dead-time is selectable.
- PWM6 and PWM7 coupled mode with a specified dead-time is selectable.
- Start/Stop/Clear control from the external input is available.
- Emergency stop from the external input and the interrupt occurrence in the coupled mode is available.
- Sampling time of the external input is selectable (when the PWM clock is OSCLK).

11.1.2 Configuration

Figure 11-1 shows the configuration of PWM 4 and PWM5.



PWnPL	: PWMn period register L	PWnPH	: PWMn period register H
PWnPBUF	: PWMn period buffer		
PWnDL	: PWMn duty register L	PWnDH	: PWMn duty register H
PWnDBUF	: PWMn duty buffer		
PWnCL	: PWMn counter register L	PWnCH	: PWMn counter register H
PWnCON0	: PWMn control register 0	PWnCON1	: PWMn control register 1
PWnCON2	: PWMn control register 2	PW4CON3	: PWM4 control register 3
PWnCON4	: PWMn control register 4	PWnCON5	: PWMn control register 5
PWnCON6	: PWMn control register 6		

n=4 to 5

Figure 11-1 (a) Configuration of PWM4 and PWM5 / Single mode

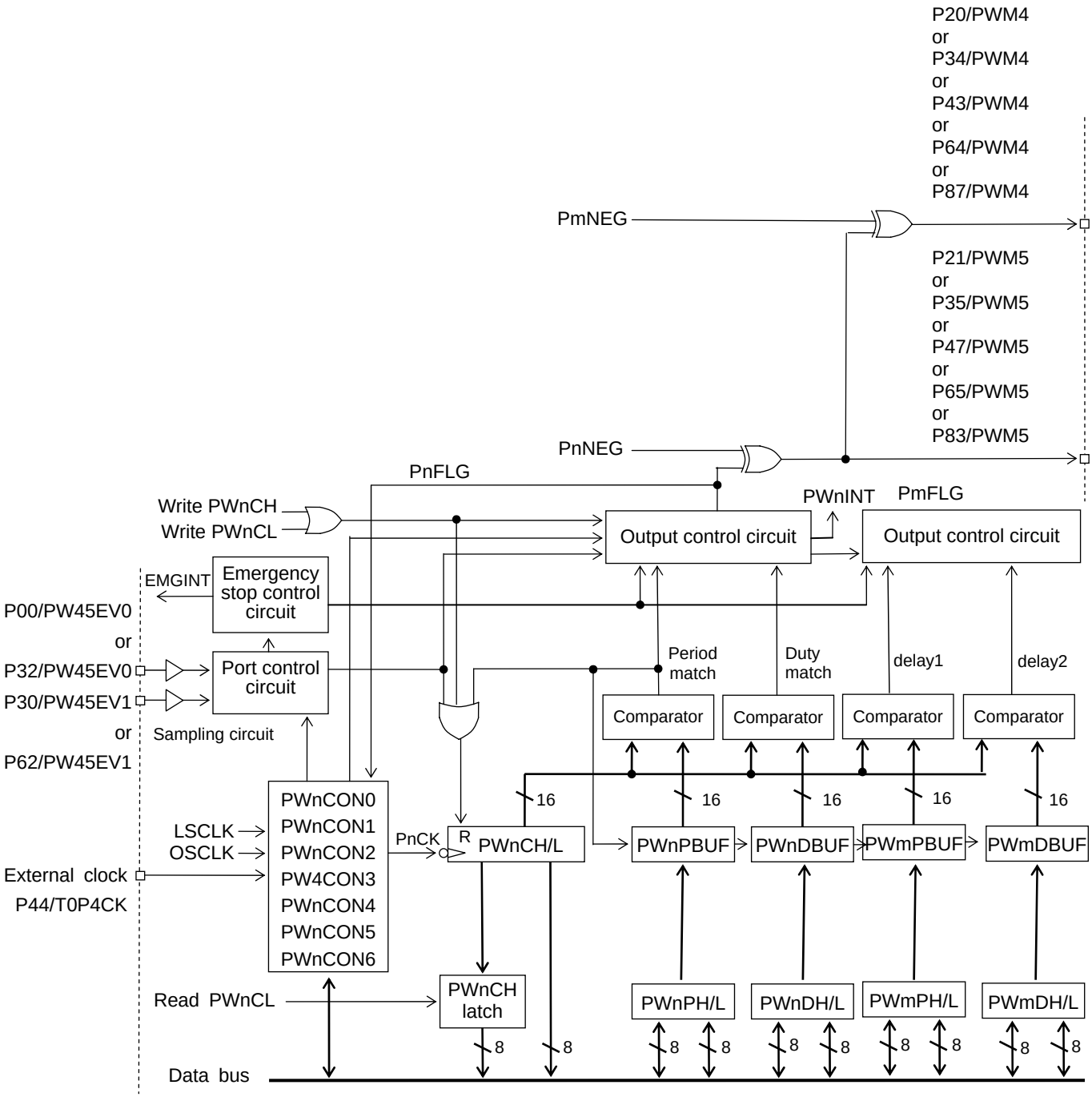
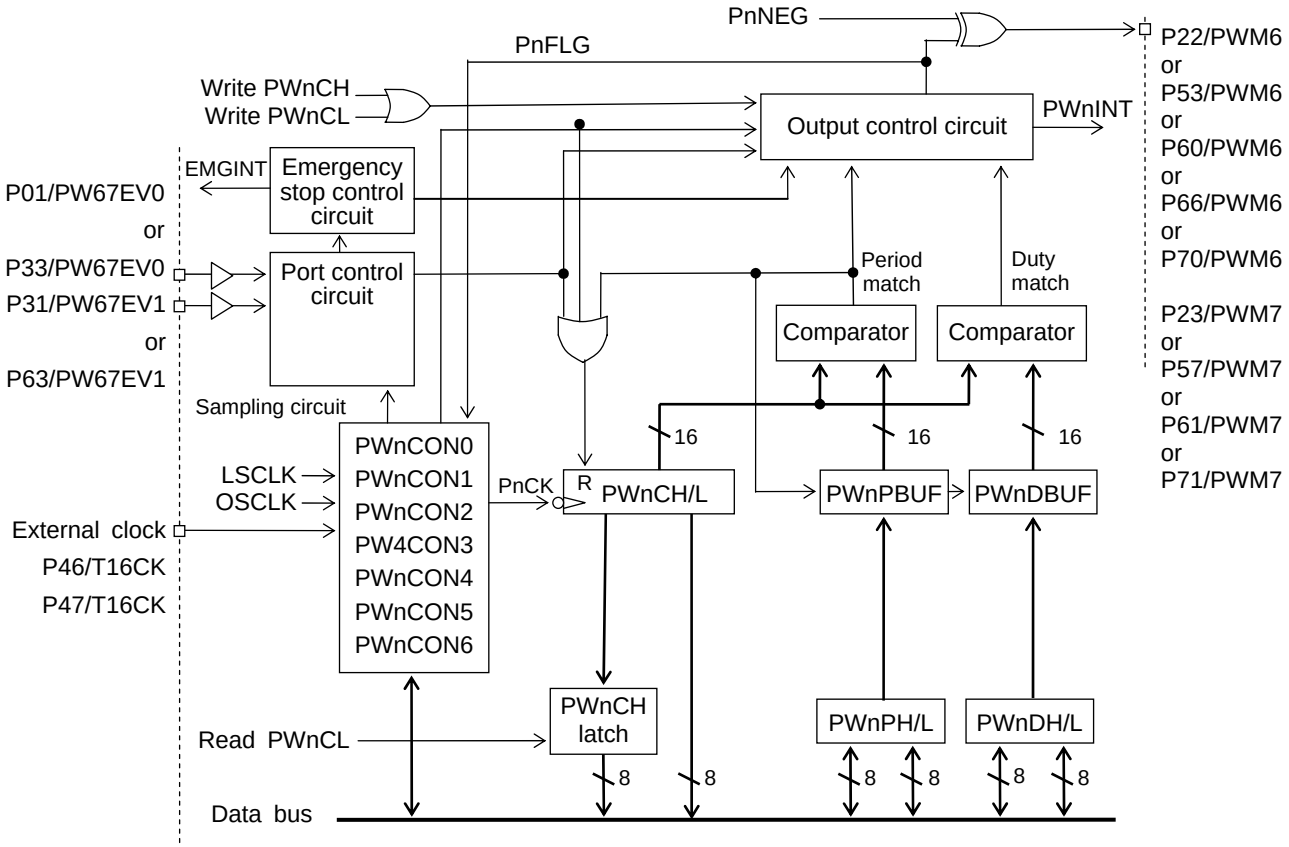


Figure 11-1 (b) Configuration of PWM4 and PWM5 / Coupled mode

Figure 11-2 shows the configuration of PWM 6 and PWM7.



PWnPL	: PWMn period register L	PWnPH	: PWMn period register H
PWnPBUF	: PWMn period buffer		
PWnDL	: PWMn duty register L	PWnDH	: PWMn duty register H
PWnDBUF	: PWMn duty buffer		
PWnCL	: PWMn counter register L	PWnCH	: PWMn counter register H
PWnCON0	: PWMn control register 0	PWnCON1	: PWMn control register 1
PWnCON2	: PWMn control register 2	PW4CON3	: PWM4 control register 3
PWnCON4	: PWMn control register 4	PWnCON5	: PWMn control register 5
PWnCON6	: PWMn control register 6		

n=6 to 7

Figure 11-2 (a) Configuration of PWM6 and PWM7 / Single mode

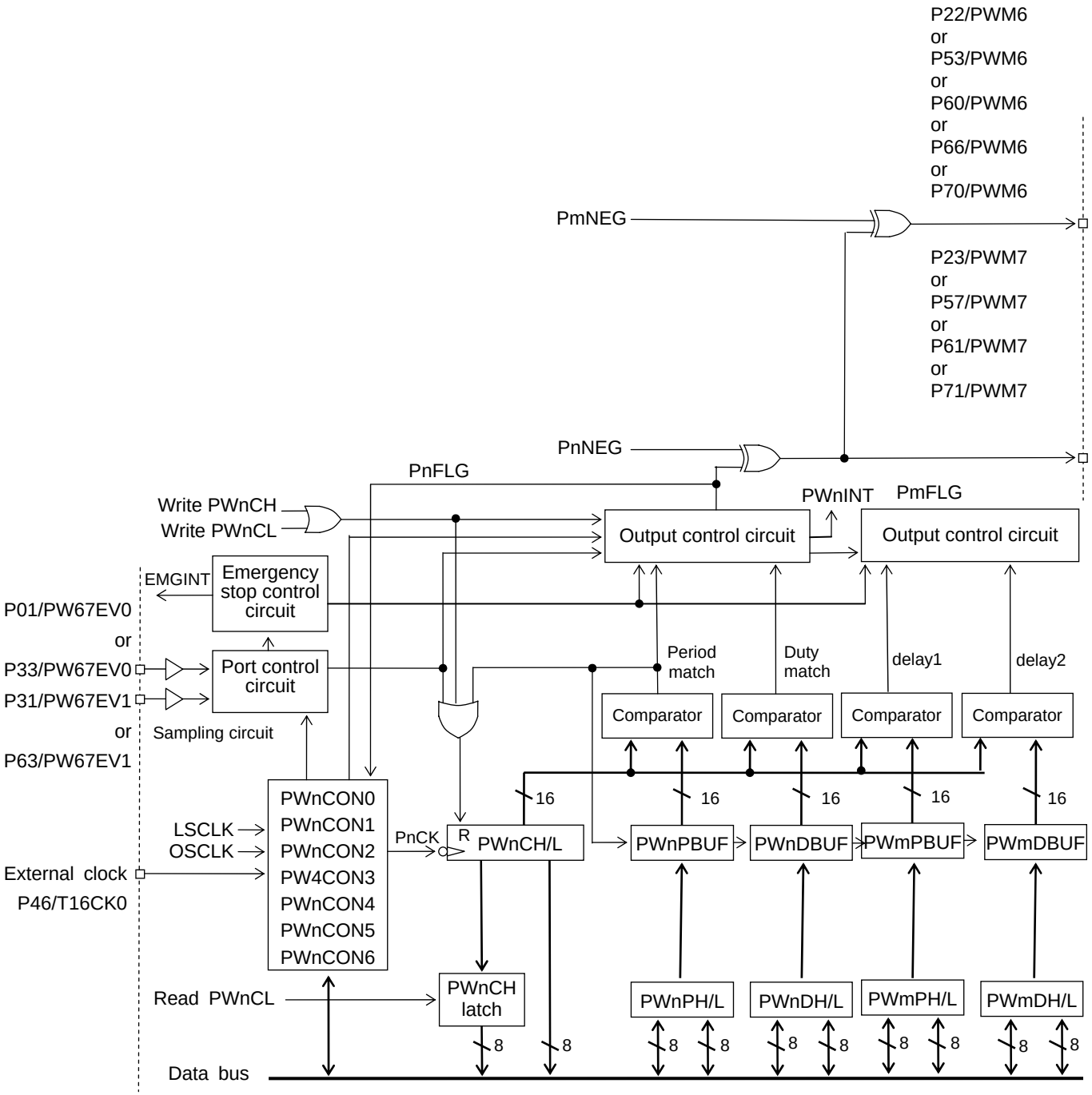


Figure 11-2 (b) Configuration of PWM6 and PWM7 / Coupled mode

11.1.3 List of Pins

Pin name	I/O	Function
P44/T0P4CK	I	Used for an external clock input for PWM4.
P45/T1P5CK	I	Used for an external clock input for PWM5.
P46/ T16CK0	I	Used for an external clock input for PWM6.
P47/ T16CK1	I	Used for an external clock input for PWM7.
P00/PW45EV0	I	Used for an external clock input for PWM4 and PWM5.
P32/PW45EV0	I	Used for an external clock input for PWM4 and PWM5.
P30/PW45EV1	I	Used for an external clock input for PWM4 and PWM5.
P62/PW45EV1	I	Used for an external clock input for PWM4 and PWM5.
P01/PW67EV0	I	Used for an external clock input for PWM6 and PWM7.
P33/PW67EV0	I	Used for an external clock input for PWM6 and PWM7.
P31/PW67EV1	I	Used for an external clock input for PWM6 and PWM7.
P63/PW67EV1	I	Used for an external clock input for PWM6 and PWM7.
P20/PWM4	O	PWM4 output pin, used as the tertiary function of P20.
P34/PWM4	O	PWM4 output pin, used as the tertiary function of P34.
P43/PWM4	O	PWM4 output pin, used as the tertiary function of P43.
P64/PWM4	O	PWM4 output pin, used as the tertiary function of P64.
P87/PWM4	O	PWM4 output pin, used as the tertiary function of P87.
P21/PWM5	O	PWM5 output pin, used as the tertiary function of P21.
P35/PWM5	O	PWM5 output pin, used as the tertiary function of P35.
P47/PWM5	O	PWM5 output pin, used as the tertiary function of P47.
P65/PWM5	O	PWM5 output pin, used as the tertiary function of P65.
P83/PWM5	O	PWM5 output pin, used as the tertiary function of P83.
P22/PWM6	O	PWM6 output pin, used as the quartic function of P22.
P53/PWM6	O	PWM6 output pin, used as the tertiary function of P53.
P60/PWM6	O	PWM6 output pin, used as the quartic function of P60.
P66/PWM6	O	PWM6 output pin, used as the tertiary function of P66.
P67/PWM6	O	PWM6 output pin, used as the tertiary function of P67.
P23/PWM7	O	PWM7 output pin, used as the quartic function of P23.
P57/PWM7	O	PWM7 output pin, used as the quartic function of P57.
P61/PWM7	O	PWM7 output pin, used as the quartic function of P61.
P71/PWM7	O	PWM7 output pin, used as the tertiary function of P71.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F4A0H	PWM4 period register L	PW4PL	PW4P	R/W	8/16	0FFH
0F4A1H	PWM4 period register H	PW4PH		R/W	8	0FFH
0F4A2H	PWM4 duty register L	PW4DL	PW4D	R/W	8/16	00H
0F4A3H	PWM4 duty register H	PW4DH		R/W	8	00H
0F4A4H	PWM4 counter register L	PW4CL	PW4C	R/W	8/16	00H
0F4A5H	PWM4 counter register H	PW4CH		R/W	8	00H
0F4A6H	PWM4 control register 0	PW4CON0	PW4CON0W	R/W	8/16	00H
0F4A7H	PWM4 control register 1	PW4CON1		R/W	8	40H
0F4A8H	PWM4 control register 2	PW4CON2	PW4CON2W	R/W	8/16	00H
0F4A9H	PWM4 control register 3	PW4CON3		R/W	8	10H
0F4AAH	PWM4 control register 4	PW4CON4	PW4CON4W	R/W	8/16	00H
0F4ABH	PWM4 control register 5	PW4CON5		R/W	8	00H
0F4ACH	PWM4 control register 6	PW4CON6	—	R/W	8	00H
0F4B0H	PWM5 period register L	PW5PL	PW5P	R/W	8/16	0FFH
0F4B1H	PWM5 period register H	PW5PH		R/W	8	0FFH
0F4B2H	PWM5 duty register L	PW5DL	PW5D	R/W	8/16	00H
0F4B3H	PWM5 duty register H	PW5DH		R/W	8	00H
0F4B4H	PWM5 counter register L	PW5CL	PW5C	R/W	8/16	00H
0F4B5H	PWM5 counter register H	PW5CH		R/W	8	00H
0F4B6H	PWM5 control register 0	PW5CON0	PW5CON0W	R/W	8/16	00H
0F4B7H	PWM5 control register 1	PW5CON1		R/W	8	40H
0F4B8H	PWM5 control register 2	PW5CON2	—	R/W	8	00H
0F4BAH	PWM5 control register 3	PW5CON4	PW5CON4W	R/W	8/16	00H
0F4BBH	PWM5 control register 4	PW5CON5		R/W	8	00H
0F4BCH	PWM5 control register 5	PW5CON6	—	R/W	8	00H
0F4C0H	PWM6 period register L	PW6PL	PW6P	R/W	8/16	0FFH
0F4C1H	PWM6 period register H	PW6PH		R/W	8	0FFH
0F4C2H	PWM6 duty register L	PW6DL	PW6D	R/W	8/16	00H
0F4C3H	PWM6 duty register H	PW6DH		R/W	8	00H
0F4C4H	PWM6 counter register L	PW6CL	PW6C	R/W	8/16	00H
0F4C5H	PWM6 counter register H	PW6CH		R/W	8	00H
0F4C6H	PWM6 control register 0	PW6CON0	PW6CON0W	R/W	8/16	00H
0F4C7H	PWM6 control register 1	PW6CON1		R/W	8	40H
0F4C8H	PWM6 control register 2	PW6CON2	PW6CON2W	R/W	8/16	00H
0F4C9H	PWM6 control register 3	PW6CON3		R/W	8	10H
0F4CAH	PWM6 control register 4	PW6CON4	PW6CON4W	R/W	8/16	00H
0F4CBH	PWM6 control register 5	PW6CON5		R/W	8	00H
0F4CCH	PWM6 control register 6	PW6CON6	—	R/W	8	00H
0F4D0H	PWM7 period register L	PW7PL	PW7P	R/W	8/16	0FFH
0F4D1H	PWM7 period register H	PW7PH		R/W	8	0FFH
0F4D2H	PWM7 duty register L	PW7DL	PW7D	R/W	8/16	00H
0F4D3H	PWM7 duty register H	PW7DH		R/W	8	00H
0F4D4H	PWM7 counter register L	PW7CL	PW7C	R/W	8/16	00H

0F4D5H	PWM7 counter register H	PW7CH		R/W	8	00H
0F4D6H	PWM7 control register 0	PW7CON0	PW7CON0W	R/W	8/16	00H
0F4D7H	PWM7 control register 1	PW7CON1		R/W	8	40H
0F4D8H	PWM7 control register 2	PW7CON2	—	R/W	8	00H
0F4DAH	PWM7 control register 3	PW7CON4	PW7CON4W	R/W	8/16	00H
0F4DBH	PWM7 control register 4	PW7CON5		R/W	8	00H
0F4DCH	PWM7 control register 6	PW7CON6	—	R/W	8	00H

11.2.2 PWM4 period register (PW4PL, PW4PH)

Address: 0F4A0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW4PL	P4P7	P4P6	P4P5	P4P4	P4P3	P4P2	P4P1	P4P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F4A1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW4PH	P4P15	P4P14	P4P13	P4P12	P4P11	P4P10	P4P9	P4P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PW4PH and PW4PL are special function registers (SFRs) to set the PWM4 periods.

Note:
When PW4PH or PW4PL is set to “0000H”, the PWM4 period buffer (PW4PBUF) is set to “0001H”.
Execute a word type transfer instruction to set the register.

11.2.3 PWM4 duty register (PW4DL, PW4DH)

Address: 0F4A2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4DL	P4D7	P4D6	P4D5	P4D4	P4D3	P4D2	P4D1	P4D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4DH	P4D15	P4D14	P4D13	P4D12	P4D11	P4D10	P4D9	P4D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4DH and PW4DL are special function registers (SFRs) to set the PWM4 duties.
In the coupled mode (P45MD=1) and when the dead-time is set (P4DTMD=1), the duty of PWM4 is determined by setting data of PW4D plus PW5D, and the period of PWM5 is determined by the setting data of PW4D.

Note:
Set PW4DH and PW4DL to values smaller than those to which PW4PH and PW4PL are set.
Execute a word type transfer instruction to set the register.

11.2.4 PWM4 counter register (PW4CL, PW4CH)

Address: 0F4A4H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CL	P4C7	P4C6	P4C5	P4C4	P4C3	P4C2	P4C1	P4C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4A5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CH	P4C15	P4C14	P4C13	P4C12	P4C11	P4C10	P4C9	P4C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CL and PW4CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW4CL or PW4CH, PW4CL and PW4CH is set to “0000H”. The data that is written is meaningless.
When data is read from PW4CL, the value of PW4CH is latched. When reading PW4CH and PW4CL, use a word type instruction or pre-read PW4CL.

The contents of PW4CH and PW4CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 11-1 shows PW4CH and PW4CL read enable/disable for each combination of the PWM clock and system clock.

Table 11-1 PW4CH and PW4CL Read Enable/Disable during PWM4 Operation

PWM clock P4CK	System clock SYSCLK	PW4CH and PW4CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW4CH or PW4CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

11.2.5 PWM4 control register 0 (PW4CON0)

Address: 0F4A6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CON0	P4CLIG	P4STPSEL	P4INI	P4NEG	P4IS1	P4IS0	P4CS1	P4CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CON0 is a special function register (SFR) to control the PWM4.

[Description of Bits]

- **P4CLIG** (bit 7)
  The P4CLIG bit is used to enable or disable the external clear input when the mode is software start mode or external input clear mode and the PWM4 output flag (P4FLG) is "H" level. In the coupled mode (P45MD="H"), this setting is also applied to the PWM5.

P4CLIG	Description
0	The external clear input is enable (Initial)
1	The external clear input is disable

- **P4STPSEL** (bit 6)
  The P4STPSEL bit is used to select the PWM4 output level while the PWM4 output is being temporarilly suspended, which holds the level or gets it back to an initial level. The initial level is determined by P4INI bit and the level is reversed when P4NEG bit is "1".

P4STPSEL	Description
0	Holds the PWM4 output level during the temporary suspension (Initial)
1	Gets the PWM4 output back to the initial level during the temporary suspension

- **P4INI** (bit 5)
  The P4INI bit is used to select the initial level of PWM4. When P4NEG bit is "1" the initial level is also reversed.

P4INI	Description
0	The initial level of PWM4 output is "H" (Initial)
1	The initial level of PWM4 output is "L"

- **P4NEG** (bit 4)
  The P4NEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWM4 output is "H", and when the negative logic is selected, the initial value of PWM4 output is "L".

P0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P4IS1, P4IS0** (bits 3, 2)
  The P4IS1 and P4IS0 bits are used to select the point at which the PWM4 interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

P4IS1	P4IS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **P4CS1, P4CS0** (bits 1, 0)
  The P4CS1 and P4CS0 bits are used to select the PWM4 operation clocks. LSCLK, OSCLK, or the external clock (P44/T0P4CK) can be selected. When the OSCLK is selected for the PWM4 clock, external triggers (external input start or clear) are sampled by the OSCLK. When other clocks are selected for the PWM4 clock, they are sampled by the LSCLK.
  In the coupled mode (P45MD="H"), this setting is also applied to the PWM5.

P4CS1	P4CS0	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use
1	1	External clock (P44/T0P4CK)

11.2.6 PWM4 control register 1 (PW4CON1)

Address: 0F4A7H
Access: R/W
Access size: 8 bits
Initial value: 40H

	7	6	5	4	3	2	1	0
PW4CON1	P4STAT	P4FLG	—	—	—	—	—	P4RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	1	0	0	0	0	0	0

PW4CON1 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P4STAT** (bit 7)
  The P4STAT bit indicates “counting stopped or “counting in progress” of PWM4.

P4STAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

- **P4FLG** (bit 6)
  The P4FLG bit is used to read the output flag(internal level) of PWM4.
  This bit is set to “1” when write operation to PW4CH or PW4CL is performed,

P4FLG	Description
0	PWM4 output flag = “0”
1	PWM4 output flag = “1” (initial value)

- **P4RUN** (bit 0)
  The P4RUN bit is used to control count stop/start of PWM4.

P4RUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

11.2.7 PWM4 control register 2 (PW4CON2)

Address: 0F4A8H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CON2	P45MD	P4MD	—	P4TGSEL	P4STM1	P4STM0	P4TGE1	P4TGE0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CON2 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P45 MD** (bit 7)
  The P45MD bit is used to select single mode or coupled mode of PWM4 and PWM5. Setting "1" to the P45MD bit enables PWM4 work in conjunction with PWM5.

P45MD	Description
0	Single mode of PWM4 or PWM5 (Initial value)
1	Coupled mode of PWM4 and PWM5

- **P4 MD** (bit 6)
  The P4MD bit is used to select one shot mode or repeate mode of PWM4. Setting "1" to the P4MD bit selects the one shot mode. In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4MD	Description
0	Reapet mode of PWM4 (Initial value)
1	One shot mode of PWM4

- **P4TGSEL** (bit 4)
  P4TGSEL is used to select the hardware control pin. In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4TGSEL	Description	
	External input start / External input clear control	Emergency stop control
0	Use PW45EV0 pin (Initial value)	Use PW45EV1 pin (Initial value)
1	Use PW45EV1 pin	Use PW45EV0 pin

- **P4STM1、P4STM0** (bit 3, bit 2)
  P4STM1 and P4STM0 are used to select the count start mode of PWM4. In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4STM1	P4STM0	Description
0	0	Software start mode (Initial value)
0	1	Software start mode or External input start mode
1	0	External input start mode
1	1	Software start mode or External input clear mode

- **P4TGE1**、**P4TGE0** (bit 1, bit 0)
  P4TGE1 and P4TGE0 are used to select the trigger edge of PWM4 external input control. In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4TGE1	P4TGE0	Description	
		During the external input start mode (P4STM1,P4STM0 = ”01” or ”10”)	During the external input clear mode (P4STM1,P4STM0 = ”11”)
0	0	External input start is disable(Initial)	External input clear is disable(Initial)
0	1	Rising edge start Falling edge stop & clear	Falling edge clear
1	0	Falling edge start Rising edge stop & clear	Rising edge clear
1	1	External input start is disable	Both edge clear

11.2.8 PWM4 control register 3 (PW4CON3)

Address: 0F4A9H
Access: R/W
Access size: 8 bits
Initial value: 10H

	7	6	5	4	3	2	1	0
PW4CON3	P4SDST	—	—	P4DTMD	—	—	P4SDE1	P4SDE0
R/W	R/W	R	R	R/W	R	R	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

PW4CON3 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P4SDST** (bit 7)

P4SDST bit indicates that emergency stop interrupt occurred. Writing "1" to this bit clears the bit.
The emergency stop function is enable in the coupled mode (P45MD=1).

P4SDST	Description
0	No emergency stop interrupt occurred (Initial)
1	Emergency stop interrupt occurred

- **P4DTMD** (bit 4)

P4DTMD bit is used to determine if the PWM has the dead-time or not in the coupled mode(P45MD=1).
When the PWM has the dead-time, the setting data of PWM5 duty register(PW5D) is applied for the dead-time.
This function is available in the coupled mode (P45MD=1).

- **P4SDE1, P4SDE0** (bit 1, bit 0)

P4SDE1 bit and P4SDE0 bit are used to enable / disable the emrgency stop function and select the operating edge of the emergency stop. The emergency stop function is enable in the coupled mode (P45MD=1).

P4SDE1	P4SDE0	Description
0	0	Emrgency stop function is disabled (Initial)
0	1	Rising edge
1	0	Falling edge
1	1	Both edge

11.2.9 PWM4 control register 4 (PW4CON4)

Address: 0F4AAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CON4	—	—	—	—	—	P4T1SEL0	—	P4T0SEL0
R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CON4 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P4T1SEL0** (bit 2)
  P4T1SEL0 bit is used to select the external input PW45EV1 pin.
  In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4T1SEL0	Description
0	Specify PW45EV1 pin to P30 pin (Initial)
1	Specify PW45EV1 pin to P62 pin

- **P4T0SEL0** (bit 0)
  P4T0SEL0 bit is used to select the external input PW45EV0 pin.
  In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4T0SEL0	Description
0	Specify PW45EV0 pin to P00 pin (Initial)
1	Specify PW45EV0 pin to P32 pin

11.2.10 PWM4 control register 5 (PW4CON5)

Address: 0F4ABH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CON5	—	—	P4T1S1	P4T1S0	—	—	P4T0S1	P4T0S0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CON5 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P4T1S1, P4T1S0** (bit 5, bit 4)
  P4T1S1 and P4T1S0 determines sampling time for the external input PW45EV1 pin. This function is available when the PWM4 operating clock is OSCLK (P4CS1=0, P4CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4T1S1	P4T1S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

- **P4T0S1, P4T0S0** (bit 1, bit 0)
  P4T0S1 and P4T0S0 determines sampling time for the external input PW45EV0 pin. This function is available when the PWM4 operating clock is OSCLK (P4CS1=0, P4CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4T0S1	P4T0S0	説明
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

Note:
This function is available when the PWM4 operating clock is OSCLK (P4CS1=0, P4CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.

11.2.11 PWM4 control register 6 (PW4CON6)

Address: 0F4ACH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW4CON6	—	—	—	—	—	P4DIV2	P4DIV1	P4DIV0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW4CON6 is a special function register (SFR) to control PWM4.

[Description of Bits]

- **P4DIV2 ~P4DIV0** (bit 2 to bit 0)
  P4DIV2~P4DIV0 are used to select division ratio of PWM4 operating clock.
  PWM4 works with the divided clock of that selected by P4CS1 and P4CS0 bit.
  In the coupled mode (P45MD=1), this setting is also applied to the PWM5.

P4DIV2	P4DIV1	P4DIV0	Description
0	0	0	1/1 Clock selected by P4CS1 and P4CS0 bit (Initial)
0	0	1	1/2 Clock selected by P4CS1 and P4CS0 bit
0	1	0	1/4 Clock selected by P4CS1 and P4CS0 bit
0	1	1	1/8 Clock selected by P4CS1 and P4CS0 bit
1	0	0	1/16 Clock selected by P4CS1 and P4CS0 bit
1	0	1	1/32 Clock selected by P4CS1 and P4CS0 bit
1	1	0	1/64 Clock selected by P4CS1 and P4CS0 bit
1	1	1	Do not use (1/1 Clock selected by P4CS1 and P4CS0 bit)

11.2.12 PWM5 period register (PW5PL, PW5PH)

Address: 0F4B0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW5PL	P5P7	P5P6	P5P5	P5P4	P5P3	P5P2	P5P1	P5P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F4B1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW5PH	P5P15	P5P14	P5P13	P5P12	P5P11	P5P10	P5P9	P5P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PW5PH and PW5PL are special function registers (SFRs) to set the PWM5 periods.

Note:
When PW5PH or PW5PL is set to “0000H”, the PWM5 period buffer (PW5PBUF) is set to “0001H”.
Execute a word type transfer instruction to set the register.

11.2.13 PWM5 duty register (PW5DL, PW5DH)

Address: 0F4B2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5DL	P5D7	P5D6	P5D5	P5D4	P5D3	P5D2	P5D1	P5D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4B3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5DH	P5D15	P5D14	P5D13	P5D12	P5D11	P5D10	P5D9	P5D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5DH and PW5DL are special function registers (SFRs) to set the PWM4 duties.
In the coupled mode (P45MD=1) and when the dead-time is set (P4DTMD=1), PW5D is used as the setting data of dead-time.

Note:
Set PW5DH and PW5DL to values smaller than those to which PW5PH and PW5PL are set.
Execute a word type transfer instruction to set the register.

11.2.14 PWM5 counter register (PW4CL, PW4CH)

Address: 0F4B4H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CL	P5C7	P5C6	P5C5	P5C4	P5C3	P5C2	P5C1	P5C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4B5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CH	P5C15	P5C14	P5C13	P5C12	P5C11	P5C10	P5C9	P5C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CL and PW5CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW5CL or PW5CH, PW5CL and PW5CH is set to “0000H”. The data that is written is meaningless.
When data is read from PW5CL, the value of PW5CH is latched. When reading PW5CH and PW5CL, use a word type instruction or pre-read PW5CL.

The contents of PW5CH and PW5CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 11-2 shows PW5CH and PW5CL read enable/disable for each combination of the PWM clock and system clock.

Table 11-2 PW5CH and PW5CL Read Enable/Disable during PWM5 Operation

PWM clock P5CK	System clock SYSCLK	PW5CH and PW5CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW5CH or PW5CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

11.2.15 PWM5 control register 0 (PW5CON0)

Address: 0F4B6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CON0	P5CLIG	P5STPSEL	P5INI	P5NEG	P5IS1	P5IS0	P5CS1	P5CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CON0 is a special function register (SFR) to control the PWM5.

[Description of Bits]

- **P5CLIG** (bit 7)
  The P5CLIG bit is used to enable or disable the external clear input when the mode is software start mode or external input clear mode and the PWM5 output flag (P5FLG) is "H" level. In the coupled mode (P45MD="H"), this bit is ignored and the setting of P4CLIG bit is applied.

P5CLIG	Description
0	The external clear input is enable (Initial)
1	The external clear input is disable

- **P5STPSEL** (bit 6)
  The P5STPSEL bit is used to select the PWM5 output level while the PWM5 output is being temporarilly suspended, which holds the level or gets it back to an initial level. The initial level is determined by P5INI bit and the level is reversed when P5NEG bit is "1". In the coupled mode (P45MD="H"), the setting of this bit is applied when P4RUN bit is "0".

P5STPSEL	Description
0	Holds the PWM5 output level during the temporary suspension (Initial)
1	Gets the PWM5 output back to the initial level during the temporary suspension

- **P5INI** (bit 5)
  The P5INI bit is used to select the initial level of PWM5. When P5NEG bit is "1" the initial level is also reversed.

P5INI	Description
0	The initial level of PWM5 output is "H" (Initial)
1	The initial level of PWM5 output is "L"

- **P5NEG** (bit 4)
  The P5NEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWM5 output is "H", and when the negative logic is selected, the initial value of PWM5 output is "L".

P5NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P5IS1, P5IS0** (bits 3, 2)
  The P5IS1 and P5IS0 bits are used to select the point at which the PWM5 interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

P5IS1	P5IS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **P5CS1, P5CS0** (bits 1, 0)
  The P5CS1 and P5CS0 bits are used to select the PWM5 operation clocks. LSCLK, OSCLK, or the external clock (P45/T1P5CK) can be selected. When the OSCLK is selected for the PWM5 clock, external triggers (external input start or clear) are sampled by the OSCLK. When other clocks are selected for the PWM5 clock, they are sampled by the LSCLK.

P4CS1	P4CS0	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use
1	1	External clock (P45/T1P5CK)

11.2.16 PWM5 control register 1 (PW5CON1)

Address: 0F4B7H
Access: R/W
Access size: 8 bits
Initial value: 40H

	7	6	5	4	3	2	1	0
PW5CON1	P5STAT	P5FLG	—	—	—	—	—	P5RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	1	0	0	0	0	0	0

PW5CON1 is a special function register (SFR) to control PWM5.

[Description of Bits]

- **P5STAT** (bit 7)
  The P5STAT bit indicates “counting stopped or “counting in progress” of PWM5.

P5STAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

- **P5FLG** (bit 6)
  The P5FLG bit is used to read the output flag (internal level) of PWM5.
  This bit is set to “1” when write operation to PW5CH or PW5CL is performed,

P5FLG	Description
0	PWM5 output flag = “0”
1	PWM5 output flag = “1” (initial value)

- **P5RUN** (bit 0)
  The P5RUN bit is used to control count stop/start of PWM5.

P5RUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

11.2.17 PWM5 control register 2 (PW5CON2)

Address: 0F4B8H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CON2	—	P5MD	—	P5TGSEL	P5STM1	P5STM0	P5TGE1	P5TGE0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CON2 is a special function register (SFR) to control PWM5.

[Description of Bits]

- **P5 MD** (bit 6)
  The P5MD bit is used to select one shot mode or repeate mode of PWM5. Setting “1” to the P5MD bit selects the one shot mode. In the coupled mode (P45MD=”H”), this bit is ignored and the setting of P4MD bit is applied.

P5MD	Description
0	Reapet mode of PWM5 (Initial value)
1	One shot mode of PWM5

- **P5TGSEL** (bit 4)
  P5TGSEL is used to select the hardware control pin. In the coupled mode (P45MD=”H”), this bit is ignored and the setting of P4TGSEL bit is applied.

P5TGSEL	Description
	External input start / External input clear control
0	Use PW45EV0 pin (Initial value)
1	Use PW45EV1 pin

- **P5STM1、P5STM0** (bit 3, bit 2)
  P5STM1 and P5STM0 are used to select the count start mode of PWM5. In the coupled mode (P45MD=1), this bit is ignored.

P5STM1	P5STM0	Description
0	0	Software start mode (Initial value)
0	1	Software start mode or External input start mode
1	0	External input start mode
1	1	Software start mode or External input clear mode

- **P5TGE1**、**P5TGE0** (bit 1, bit 0)
  P5TGE1 and P5TGE0 are used to select the trigger edge of PWM5 external input control. In the coupled mode (P45MD=1), this bit is ignored.

P5TGE1	P5TGE0	Description	
		During the external input start mode (P5STM1,P5STM0 = ”01” or ”10”)	During the external input clear mode (P5STM1,P5STM0 = ”11”)
0	0	External input start is disable(Initial)	External input clear is disable(Initial)
0	1	Rising edge start Falling edge stop & clear	Falling edge clear
1	0	Falling edge start Rising edge stop & clear	Rising edge clear
1	1	External input start is disable	Both edge clear

11.2.18 PWM5 control register 4 (PW5CON4)

Address: 0F4BAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CON4	—	—	—	—	—	P5T1SEL0	—	P5T0SEL0
R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CON4 is a special function register (SFR) to control PWM5.

[Description of Bits]

- **P5T1SEL0** (bit 2)
  P5T1SEL0 bit is used to select the external input PW45EV1 pin.
  In the coupled mode (P45MD=1), this bit is ignored and the setting of P4T1SEL0 bit is applied.

P5T1SEL0	Description
0	Specify PW45EV1 pin to P30 pin (Initial)
1	Specify PW45EV1 pin to P62 pin

- **P5T0SEL0** (bit 0)
  P5T0SEL0 bit is used to select the external input PW45EV0 pin.
  In the coupled mode (P45MD=1), this bit is ignored and the setting of P4T0SEL0 bit is applied.

P5T0SEL0	Description
0	Specify PW45EV0 pin to P00 pin (Initial)
1	Specify PW45EV0 pin to P32 pin

11.2.19 PWM5 control register 5 (PW5CON5)

Address: 0F4BBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CON5	—	—	P5T1S1	P5T1S0	—	—	P5T0S1	P5T0S0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CON5 is a special function register (SFR) to control PWM5.

[Description of Bits]

- **P5T1S1, P5T1S0** (bit 5, bit 4)
  P5T1S1 and P5T1S0 determines sampling time for the external input PW45EV1 pin. This function is available when the PWM5 operating clock is OSCLK (P5CS1=0, P5CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P45MD=1), these bits are ignored and the setting of P4T1S1 and P4T1S0 bit are applied.

P5T1S1	P5T1S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

- **P5T0S1, P5T0S0** (bit 1, bit 0)
  P5T0S1 and P5T0S0 determines sampling time for the external input PW45EV0 pin. This function is available when the PWM5 operating clock is OSCLK (P5CS1=0, P5CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P45MD=1), these bits are ignored and the setting of P4T0S1 and P4T0S0 bit are applied.

P5T0S1	P5T0S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

Note:
This function is available when the PWM5 operating clock is OSCLK (P5CS1=0, P5CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.

11.2.20 PWM5 control register 6 (PW5CON6)

Address: 0F4BCH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW5CON6	—	—	—	—	—	P5DIV2	P5DIV1	P5DIV0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW5CON6 is a special function register (SFR) to control PWM5.

[Description of Bits]

- **P5DIV2 ~P5DIV0** (bit 2 to bit 0)
  P5DIV2~P5DIV0 are used to select division ratio of PWM5 operating clock.
  PWM5 works with the divided clock of that selected by P5CS1 and P5CS0 bit.
  In the coupled mode (P45MD=1), these bits are ignored and the setting of P4DIV2~P4DIV0 bit are applied.

P5DIV2	P5DIV1	P5DIV0	Description
0	0	0	1/1 Clock selected by P5CS1 and P5CS0 bit (Initial)
0	0	1	1/2 Clock selected by P5CS1 and P5CS0 bit
0	1	0	1/4 Clock selected by P5CS1 and P5CS0 bit
0	1	1	1/8 Clock selected by P5CS1 and P5CS0 bit
1	0	0	1/16 Clock selected by P5CS1 and P5CS0 bit
1	0	1	1/32 Clock selected by P5CS1 and P5CS0 bit
1	1	0	1/64 Clock selected by P5CS1 and P5CS0 bit
1	1	1	Do not use (1/1 Clock selected by P5CS1 and P5CS0 bit)

11.2.21 PWM6 period register (PW6PL, PW6PH)

Address: 0F4C0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW6PL	P6P7	P6P6	P6P5	P6P4	P6P3	P6P2	P6P1	P6P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F4C1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW6PH	P6P15	P6P14	P6P13	P6P12	P6P11	P6P10	P6P9	P6P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PW6PH and PW6PL are special function registers (SFRs) to set the PWM6 periods.

Note:
When PW6PH or PW6PL is set to “0000H”, the PWM6 period buffer (PW6PBUF) is set to “0001H”.
Execute a word type transfer instruction to set the register.

11.2.22 PWM6 duty register (PW6DL, PW6DH)

Address: 0F4C2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6DL	P6D7	P6D6	P6D5	P6D4	P6D3	P6D2	P6D1	P6D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4C3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6DH	P6D15	P6D14	P6D13	P6D12	P6D11	P6D10	P6D9	P6D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6DH and PW6DL are special function registers (SFRs) to set the PWM6 duties.
In the coupled mode (P67MD=1) and when the dead-time is set (P6DTMD=1), the duty of PWM6 is determined by setting data of PW6D plus PW7D, and the period of PWM7 is determined by the setting data of PW6D.

Note:
Set PW6DH and PW6DL to values smaller than those to which PW6PH and PW6PL are set.
Execute a word type transfer instruction to set the register.

11.2.23 PWM6 counter register (PW6CL, PW6CH)

Address: 0F4C4H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CL	P6C7	P6C6	P6C5	P6C4	P6C3	P6C2	P6C1	P6C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4C5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CH	P6C15	P6C14	P6C13	P6C12	P6C11	P6C10	P6C9	P6C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CL and PW6CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW6CL or PW6CH, PW6CL and PW6CH is set to “0000H”. The data that is written is meaningless.
When data is read from PW6CL, the value of PW6CH is latched. When reading PW6CH and PW6CL, use a word type instruction or pre-read PW6CL.

The contents of PW6CH and PW6CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 11-3 shows PW6CH and PW6CL read enable/disable for each combination of the PWM clock and system clock.

Table 11-3 PW6CH and PW6CL Read Enable/Disable during PWM6 Operation

PWM clock P6CK	System clock SYSCLK	PW6CH and PW6CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW6CH or PW6CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

11.2.24 PWM6 control register 0 (PW6CON0)

Address: 0F4C6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CON0	P6CLIG	P6STPSEL	P6INI	P6NEG	P6IS1	P6IS0	P6CS1	P6CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CON0 is a special function register (SFR) to control the PWM6.

[Description of Bits]

- **P6CLIG** (bit 7)
  The P6CLIG bit is used to enable or disable the external clear input when the mode is software start mode or external input clear mode and the PWM6 output flag (P6FLG) is "H" level. In the coupled mode (P67MD="H"), this setting is also applied to the PWM7.

P6CLIG	Description
0	The external clear input is enable (Initial)
1	The external clear input is disable

- **P6STPSEL** (bit 6)
  The P6STPSEL bit is used to select the PWM6 output level while the PWM6 output is being temporarilly suspended, which holds the level or gets it back to an initial level. The initial level is determined by P6INI bit and the level is reversed when P6NEG bit is "1".

P6STPSEL	Description
0	Holds the PWM6 output level during the temporary suspension (Initial)
1	Gets the PWM6 output back to the initial level during the temporary suspension

- **P6INI** (bit 5)
  The P6INI bit is used to select the initial level of PWM6. When P6NEG bit is "1" the initial level is also reversed.

P6INI	Description
0	The initial level of PWM6 output is "H" (Initial)
1	The initial level of PWM6 output is "L"

- **P6NEG** (bit 4)
  The P6NEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWM6 output is "H", and when the negative logic is selected, the initial value of PWM6 output is "L".

P0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P6IS1, P6IS0** (bits 3, 2)
  The P6IS1 and P6IS0 bits are used to select the point at which the PWM6 interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

P6IS1	P6IS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **P6CS1, P6CS0** (bits 1, 0)
  The P6CS1 and P6CS0 bits are used to select the PWM6 operation clocks. LSCLK, OSCLK, or the external clock (P46/T16CK0) can be selected. When the OSCLK is selected for the PWM6 clock, external triggers (external input start or clear) are sampled by the OSCLK. When other clocks are selected for the PWM6 clock, they are sampled by the LSCLK.
  In the coupled mode (P67MD="H"), this setting is also applied to the PWM7.

P6CS1	P6CS0	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use
1	1	External clock (P46/T16CK0)

11.2.25 PWM6 control register 1 (PW6CON1)

Address: 0F4C7H
Access: R/W
Access size: 8 bits
Initial value: 40H

	7	6	5	4	3	2	1	0
PW6CON1	P6STAT	P6FLG	—	—	—	—	—	P6RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	1	0	0	0	0	0	0

PW6CON1 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P6STAT** (bit 7)
  The P6STAT bit indicates “counting stopped or “counting in progress” of PWM6.

P6STAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

- **P6FLG** (bit 6)
  The P6FLG bit is used to read the output flag (internal level) of PWM6.
  This bit is set to “1” when write operation to PW6CH or PW6CL is performed,

P6FLG	Description
0	PWM6 output flag = “0”
1	PWM6 output flag = “1” (initial value)

- **P6RUN** (bit 0)
  The P6RUN bit is used to control count stop/start of PWM6.

P6RUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

11.2.26 PWM6 control register 2 (PW6CON2)

Address: 0F4C8H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CON2	P67MD	P6MD	—	P6TGSEL	P6STM1	P6STM0	P6TGE1	P6TGE0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CON2 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P67 MD** (bit 7)
  The P67MD bit is used to select single mode or coupled mode of PWM6 and PWM7. Setting "1" to the P67MD bit enables PWM6 work in conjunction with PWM7.

P67MD	Description
0	Single mode of PWM6 or PWM7 (Initial value)
1	Coupled mode of PWM6 and PWM7

- **P6 MD** (bit 6)
  The P6MD bit is used to select one shot mode or repeate mode of PWM6. Setting "1" to the P6MD bit selects the one shot mode. In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6MD	Description
0	Reapet mode of PWM6 (Initial value)
1	One shot mode of PWM6

- **P6TGSEL** (bit 4)
  P6TGSEL is used to select the hardware control pin. In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6TGSEL	Description	
	External input start / External input clear control	Emergency stop control
0	Use PW67EV0 pin (Initial value)	Use PW67EV1 pin (Initial value)
1	Use PW67EV1 pin	Use PW67EV0 pin

- **P6STM1、P6STM0** (bit 3, bit 2)
  P6STM1 and P6STM0 are used to select the count start mode of PWM6. In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6STM1	P6STM0	Description
0	0	Software start mode (Initial value)
0	1	Software start mode or External input start mode
1	0	External input start mode
1	1	Software start mode or External input clear mode

- **P6TGE1**、**P6TGE0** (bit 1, bit 0)
  P6TGE1 and P6TGE0 are used to select the trigger edge of PWM6 external input control. In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6TGE1	P6TGE0	Description	
		During the external input start mode (P6STM1,P6STM0 = ”01” or ”10”)	During the external input clear mode (P6STM1,P6STM0 = ”11”)
0	0	External input start is disable(Initial)	External input clear is disable(Initial)
0	1	Rising edge start Falling edge stop & clear	Falling edge clear
1	0	Falling edge start Rising edge stop & clear	Rising edge clear
1	1	External input start is disable	Both edge clear

11.2.27 PWM6 control register 3 (PW6CON3)

Address: 0F4C9H
Access: R/W
Access size: 8 bits
Initial value: 10H

	7	6	5	4	3	2	1	0
PW6CON3	P6SDST	—	—	P6DTMD	—	—	P6SDE1	P6SDE0
R/W	R/W	R	R	R/W	R	R	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

PW6CON3 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P6SDST** (bit 7)

P6SDST bit indicates that emergency stop interrupt occurred. Writing "1" to this bit clears the bit.
The emergency stop function is enable in the coupled mode (P67MD=1).

P6SDST	Description
0	No emergency stop interrupt occurred (Initial)
1	Emergency stop interrupt occurred

- **P6DTMD** (bit 4)

P6DTMD bit is used to determine if the PWM has the dead-time or not in the coupled mode(P67MD=1).
When the PWM has the dead-time, the setting data of PWM7 duty register(PW7D) is applied for the dead-time.
This function is available in the coupled mode (P67MD=1).

- **P6SDE1, P6SDE0** (bit 1, bit 0)

P6SDE1 bit and P6SDE0 bit are used to enable / disable the emrgency stop function and select the operating edge of the emergency stop. The emergency stop function is enable in the coupled mode (P67MD=1).

P6SDE1	**P6SDE0**	Description
0	0	Emrgency stop function is disabled (Initial)
0	1	Rising edge
1	0	Falling edge
1	1	Both edge

11.2.28 PWM6 control register 4 (PW6CON4)

Address: 0F4CAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CON4	—	—	—	—	—	P6T1SEL0	—	P6T0SEL0
R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CON4 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P6T1SEL0** (bit 2)
  P6T1SEL0 bit is used to select the external input PW67EV1 pin.
  In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6T1SEL0	Description
0	Specify PW67EV1 pin to P30 pin (Initial)
1	Specify PW67EV1 pin to P62 pin

- **P6T0SEL0** (bit 0)
  P6T0SEL0 bit is used to select the external input PW67EV0 pin.
  In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6T0SEL0	Description
0	Specify PW67EV0 pin to P00 pin (Initial)
1	Specify PW67EV0 pin to P32 pin

11.2.29 PWM6 control register 5 (PW6CON5)

Address: 0F4CBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CON5	—	—	P6T1S1	P6T1S0	—	—	P6T0S1	P6T0S0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CON5 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P6T1S1, P6T1S0** (bit 5, bit 4)
  P6T1S1 and P6T1S0 determines sampling time for the external input PW67EV1 pin. This function is available when the PWM6 operating clock is OSCLK (P6CS1=0, P6CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6T1S1	P6T1S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

- **P6T0S1, P6T0S0** (bit 1, bit 0)
  P6T0S1 and P6T0S0 determines sampling time for the external input PW67EV0 pin. This function is available when the PWM6 operating clock is OSCLK (P6CS1=0, P6CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6T0S1	P6T0S0	説明
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

Note:
This function is available when the PWM6 operating clock is OSCLK (P6CS1=0, P6CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.

11.2.30 PWM6 control register 6 (PW6CON6)

Address: 0F4CCH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW6CON6	—	—	—	—	—	P6DIV2	P6DIV1	P6DIV0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW6CON6 is a special function register (SFR) to control PWM6.

[Description of Bits]

- **P6DIV2 ~P6DIV0** (bit 2 to bit 0)
  P6DIV2~P6DIV0 are used to select division ratio of PWM6 operating clock.
  PWM6 works with the divided clock of that selected by P6CS1 and P6CS0 bit.
  In the coupled mode (P67MD=1), this setting is also applied to the PWM7.

P6DIV2	P6DIV1	P6DIV0	Description
0	0	0	1/1 Clock selected by P6CS1 and P6CS0 bit (Initial)
0	0	1	1/2 Clock selected by P6CS1 and P6CS0 bit
0	1	0	1/4 Clock selected by P6CS1 and P6CS0 bit
0	1	1	1/8 Clock selected by P6CS1 and P6CS0 bit
1	0	0	1/16 Clock selected by P6CS1 and P6CS0 bit
1	0	1	1/32 Clock selected by P6CS1 and P6CS0 bit
1	1	0	1/64 Clock selected by P6CS1 and P6CS0 bit
1	1	1	Do not use (1/1 Clock selected by P6CS1 and P6CS0 bit)

11.2.31 PWM7 period register (PW7PL, PW7PH)

Address: 0F4D0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW7PL	P7P7	P7P6	P7P5	P7P4	P7P3	P7P2	P7P1	P7P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F4B1H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PW7PH	P7P15	P7P14	P7P13	P7P12	P7P11	P7P10	P7P9	P7P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PW7PH and PW7PL are special function registers (SFRs) to set the PWM7 periods.

Note:
When PW7PH or PW7PL is set to “0000H”, the PWM7 period buffer (PW7PBUF) is set to “0001H”.
Execute a word type transfer instruction to set the register.

11.2.32 PWM7 duty register (PW7DL, PW7DH)

Address: 0F4D2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7DL	P7D7	P7D6	P7D5	P7D4	P7D3	P7D2	P7D1	P7D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4D3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7DH	P7D15	P7D14	P7D13	P7D12	P7D11	P7D10	P7D9	P7D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7DH and PW7DL are special function registers (SFRs) to set the PWM6 duties.
In the coupled mode (P67MD=1) and when the dead-time is set (P6DTMD=1), PW7D is used as the setting data of dead-time.

Note:
Set PW7DH and PW7DL to values smaller than those to which PW7PH and PW7PL are set.
Execute a word type transfer instruction to set the register.

11.2.33 PWM7 counter register (PW4CL, PW4CH)

Address: 0F4D4H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CL	P7C7	P7C6	P7C5	P7C4	P7C3	P7C2	P7C1	P7C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F4D5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CH	P7C15	P7C14	P7C13	P7C12	P7C11	P7C10	P7C9	P7C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CL and PW7CH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PW7CL or PW7CH, PW7CL and PW7CH is set to “0000H”. The data that is written is meaningless.
When data is read from PW7CL, the value of PW7CH is latched. When reading PW7CH and PW7CL, use a word type instruction or pre-read PW7CL.

The contents of PW7CH and PW7CL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 11-4 shows PW7CH and PW7CL read enable/disable for each combination of the PWM clock and system clock.

Table 11-4 PW7CH and PW7CL Read Enable/Disable during PWM7 Operation

PWM clock P7CK	System clock SYSCLK	PW7CH and PW7CL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PW7CH or PW7CL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
External clock	LSCLK	Read disabled
	HSCLK	

11.2.34 PWM7 control register 0 (PW7CON0)

Address: 0F4D6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CON0	P7CLIG	P7STPSEL	P7INI	P7NEG	P7IS1	P7IS0	P7CS1	P7CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CON0 is a special function register (SFR) to control the PWM7.

[Description of Bits]

- **P7CLIG** (bit 7)
  The P7CLIG bit is used to enable or disable the external clear input when the mode is software start mode or external input clear mode and the PWM7 output flag (P7FLG) is "H" level. In the coupled mode (P67MD="H"), this bit is ignored and the setting of P6CLIG bit is applied.

P7CLIG	Description
0	The external clear input is enable (Initial)
1	The external clear input is disable

- **P7STPSEL** (bit 6)
  The P7STPSEL bit is used to select the PWM7 output level while the PWM7 output is being temporarilly suspended, which holds the level or gets it back to an initial level. The initial level is determined by P7INI bit and the level is reversed when P7NEG bit is "1". In the coupled mode (P67MD="H"), the setting of this bit is applied when P6RUN bit is "0".

P7STPSEL	Description
0	Holds the PWM7 output level during the temporary suspension (Initial)
1	Gets the PWM7 output back to the initial level during the temporary suspension

- **P7INI** (bit 5)
  The P7INI bit is used to select the initial level of PWM7. When P7NEG bit is "1" the initial level is also reversed.

P7INI	Description
0	The initial level of PWM7 output is "H" (Initial)
1	The initial level of PWM7 output is "L"

- **P7NEG** (bit 4)
  The P7NEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWM7 output is "H", and when the negative logic is selected, the initial value of PWM7 output is "L".

P7NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **P7IS1, P7IS0** (bits 3, 2)
  The P7IS1 and P7IS0 bits are used to select the point at which the PWM7 interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

P7IS1	P7IS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **P7CS1, P7CS0** (bits 1, 0)
  The P7CS1 and P7CS0 bits are used to select the PWM7 operation clocks. LSCLK, OSCLK, or the external clock (P47/T16CK1) can be selected. When the OSCLK is selected for the PWM7 clock, external triggers (external input start or clear) are sampled by the OSCLK. When other clocks are selected for the PWM7 clock, they are sampled by the LSCLK.

P4CS1	P4CS0	Description
0	0	LSCLK (initial value)
0	1	OSCLK
1	0	Do not use
1	1	External clock (P47/T16CK1)

11.2.35 PWM7 control register 1 (PW7CON1)

Address: 0F4D7H
Access: R/W
Access size: 8 bits
Initial value: 40H

	7	6	5	4	3	2	1	0
PW7CON1	P7STAT	P7FLG	—	—	—	—	—	P7RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	1	0	0	0	0	0	0

PW7CON1 is a special function register (SFR) to control PWM7.

[Description of Bits]

- **P7STAT** (bit 7)
  The P7STAT bit indicates “counting stopped or “counting in progress” of PWM7.

P7STAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

- **P7FLG** (bit 6)
  The P7FLG bit is used to read the output flag (internal level) of PWM7.
  This bit is set to “1” when write operation to PW7CH or PW7CL is performed,

P7FLG	Description
0	PWM7 output flag = “0”
1	PWM7 output flag = “1” (initial value)

- **P7RUN** (bit 0)
  The P7RUN bit is used to control count stop/start of PWM7.

P7RUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

11.2.36 PWM7 control register 2 (PW7CON2)

Address: 0F4D8H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CON2	−	P7MD	−	P7TGSEL	P7STM1	P7STM0	P7TGE1	P7TGE0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CON2 is a special function register (SFR) to control PWM7.

[Description of Bits]

- **P7 MD** (bit 6)
  The P7MD bit is used to select one shot mode or repeate mode of PWM7. Setting “1” to the P7MD bit selects the one shot mode. In the coupled mode (P67MD=”H”), this bit is ignored and the setting of P6MD bit is applied.

P7MD	Description
0	Reapet mode of PWM7 (Initial value)
1	One shot mode of PWM7

- **P7TGSEL** (bit 4)
  P7TGSEL is used to select the hardware control pin. In the coupled mode (P67MD=”H”), this bit is ignored and the setting of P6TGSEL bit is applied.

P7TGSEL	Description
	External input start / External input clear control
0	Use PW67EV0 pin (Initial value)
1	Use PW67EV1 pin

- **P7STM1、P7STM0** (bit 3, bit 2)
  P7STM1 and P7STM0 are used to select the count start mode of PWM7. In the coupled mode (P67MD=1), this bit is ignored.

P7STM1	P7STM0	Description
0	0	Software start mode (Initial value)
0	1	Software start mode or External input start mode
1	0	External input start mode
1	1	Software start mode or External input clear mode

- **P7TGE1**、**P7TGE0** (bit 1, bit 0)
  P7TGE1 and P7TGE0 are used to select the trigger edge of PWM7 external input control. In the coupled mode (P67MD=1), this bit is ignored.

P7TGE1	P7TGE0	Description	
		During the external input start mode (P7STM1,P7STM0 = ”01” or ”10”)	During the external input clear mode (P7STM1,P7STM0 = ”11”)
0	0	External input start is disable(Initial)	External input clear is disable(Initial)
0	1	Rising edge start Falling edge stop & clear	Falling edge clear
1	0	Falling edge start Rising edge stop & clear	Rising edge clear
1	1	External input start is disable	Both edge clear

11.2.37 PWM7 control register 4 (PW7CON4)

Address: 0F4DAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CON4	—	—	—	—	—	P7T1SEL0	—	P7T0SEL0
R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CON4 is a special function register (SFR) to control PWM7.

[Description of Bits]

- **P7T1SEL0** (bit 2)
  P7T1SEL0 bit is used to select the external input PW67EV1 pin.
  In the coupled mode (P67MD=1), this bit is ignored and the setting of P6T1SEL0 bit is applied.

P7T1SEL0	Description
0	Specify PW67EV1 pin to P31 pin (Initial)
1	Specify PW67EV1 pin to P63 pin

- **P7T0SEL0** (bit 0)
  P7T0SEL0 bit is used to select the external input PW67EV0 pin.
  In the coupled mode (P67MD=1), this bit is ignored and the setting of P6T0SEL0 bit is applied.

P7T0SEL0	Description
0	Specify PW67EV0 pin to P01 pin (Initial)
1	Specify PW67EV0 pin to P33 pin

11.2.38 PWM7 control register 5 (PW7CON5)

Address: 0F4DBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CON5	—	—	P7T1S1	P7T1S0	—	—	P7T0S1	P7T0S0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CON5 is a special function register (SFR) to control PWM7.

[Description of Bits]

- **P7T1S1, P7T1S0** (bit 5, bit 4)
  P7T1S1 and P7T1S0 determines sampling time for the external input PW67EV1 pin. This function is available when the PWM7 operating clock is OSCLK (P7CS1=0, P7CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P67MD=1), these bits are ignored and the setting of P6T1S1 and P6T1S0 bit are applied.

P7T1S1	P7T1S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

- **P7T0S1, P7T0S0** (bit 1, bit 0)
  P7T0S1 and P7T0S0 determines sampling time for the external input PW67EV0 pin. This function is available when the PWM7 operating clock is OSCLK (P7CS1=0, P7CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.
  In the coupled mode (P67MD=1), these bits are ignored and the setting of P6T0S1 and P6T0S0 bit are applied.

P7T0S1	P7T0S0	Description
0	0	OSCLK x max. 2 clock (Initial)
0	1	OSCLK x max. 4 clock
1	0	OSCLK x max. 8 clock
1	1	OSCLK x max. 16 clock

Note:
This function is available when the PWM7 operating clock is OSCLK (P7CS1=0, P7CS0=1) and the sampling time in other case is fixed to the max. LSCLK x 2.

11.2.39 PWM7 control register 6 (PW7CON6)

Address: 0F4DCH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PW7CON6	–	–	–	–	–	P7DIV2	P7DIV1	P7DIV0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PW7CON6 is a special function register (SFR) to control PWM7.

[Description of Bits]

- **P7DIV2 ~P7DIV0** (bit 2 to bit 0)
  P7DIV2~P7DIV0 are used to select division ratio of PWM7 operating clock.
  PWM7 works with the divided clock of that selected by P7CS1 and P7CS0 bit.
  In the coupled mode (P67MD=1), these bits are ignored and the setting of P6DIV2~P6DIV0 bit are applied.

P7DIV2	P7DIV1	P7DIV0	Description
0	0	0	1/1 Clock selected by P7CS1 and P7CS0 bit (Initial)
0	0	1	1/2 Clock selected by P7CS1 and P7CS0 bit
0	1	0	1/4 Clock selected by P7CS1 and P7CS0 bit
0	1	1	1/8 Clock selected by P7CS1 and P7CS0 bit
1	0	0	1/16 Clock selected by P7CS1 and P7CS0 bit
1	0	1	1/32 Clock selected by P7CS1 and P7CS0 bit
1	1	0	1/64 Clock selected by P7CS1 and P7CS0 bit
1	1	1	Do not use (1/1 Clock selected by P7CS1 and P7CS0 bit)

11.3 Description of Operation

The operation of PWM4 and PWM5 are categorized into six modes. For more details about each operation mode, see the section 11.3.1 to 11.3.6.

P45MD	P4DTMD	PnMD	Operation mode	Description
0	-	0	Repeat mode in Single mode	PWM4 and PWM5 repeats working independently.
	-	1	One shot mode in Single mode	PWM4 and PWM5 works in one shot (one period cycle) and automatically stops, independently.
1	0	0	Repeat mode in Coupled mode No dead-time* specified	PWM4 repeats working in conjunction with PWM5. Each duty of PWM4 and PWM5 is configurable independently.
		1	One shot mode in Coupled mode No dead-time* specified	PWM4 works in one shot (one period cycle) and automatically stops, in conjunction with PWM5. Each duty of PWM4 and PWM5 is configurable independently.
	1	0	Repeat mode in Coupled mode Dead-time* specified	PWM4 repeats working in conjunction with PWM5. Dead-time can be specified to generate the timing that de-activates both PWM4 and PWM5 at the same time.
		1	One shot mode in Coupled mode Dead-time* specified	PWM4 works in one shot (one period cycle) and automatically stops, in conjunction with PWM5. Dead-time can be specified to generate the timing that de-activates both PWM4 and PWM5 at the same time.

n=4, 5

* Some motor control application uses the dead-time.

The Start/Stop/Clear controls of PWM4 and PWM5 are categorized into eleven modes.
"P00 or P32/PW45EV0" and "P30 or P62/PW45EV1" are selectable for the external hardware control.
For more details about each mode, see the section 11.3.7.

PnSTM1	PnSTM0	PnTGE1	PnTGE0	Operation mode	Description
0	0	–	–	Software start mode	Control the start/stop by writing PnRUN bit.
0	1	0	1	Software start mode or External input start mode	Control the start/stop by writing PnRUN bit. Also, can start the PWM by the external input "H" level and can stop / clear by the "L" level.
		1	0		Control the start/stop by writing PnRUN bit. Also, can start the PWM by the external input "L" level and can stop / clear by the "H" level.
		0	0		Control the start/stop by writing PnRUN bit. The external input control is disabled.
		1	1		
1	0	0	1	External input start mode	It can start the PWM by the riging edge of external input and can stop / clear by the falling edge.
		1	0		It can start the PWM by the falling edge of external input and can stop / clear by the riging edge.
		0	0		The external input control is disabled and the PWM does not work.
		1	1		
1	1	0	0	Software start mode or External input clear mode	Control the start/stop by writing PnRUN bit. The external input control is disabled.
		0	1		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the falling edge of external input.
		1	0		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the riging edge of external input.
		1	1		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the riging edge or falling edeg of external input.

n=4, 5

The operation of PWM6 and PWM7 are categorized into six modes. For more details about each operation mode, see the section 11.3.9 to 11.3.14.

P67MD	P7DTMD	PnMD	Operation mode	Description
0	-	0	Repeat mode in Single mode	PWM6 and PWM7 repeats working independently.
	-	1	One shot mode in Single mode	PWM6 and PWM7 works in one shot (one period cycle) and automatically stops, independently.
1	0	0	Repeat mode in Coupled mode No dead-time specified	PWM6 repeats working in conjunction with PWM7. Each duty of PWM6 and PWM7 is configurable independently.
		1	One shot mode in Coupled mode No dead-time specified	PWM6 works in one shot (one period cycle) and automatically stops, in conjunction with PWM7. Each duty of PWM6 and PWM7 is configurable independently.
	1	0	Repeat mode in Coupled mode Dead-time specified	PWM6 repeats working in conjunction with PWM7. Dead-time can be specified to generate the timing that de-activates both PWM6 and PWM7 at the same time.
		1	One shot mode in Coupled mode Dead-time specified	PWM6 works in one shot (one period cycle) and automatically stops, in conjunction with PWM7. Dead-time can be specified to generate the timing that de-activates both PWM6 and PWM7 at the same time.

n=6, 7

The Start/Stop/Clear controls of PWM6 and PWM7 are categorized into eleven modes.
"P01 or P33/PW67EV0" and "P31 or P63/PW67EV1" are selectable for the external hardware control.
For more details about each mode, see the section 11.3.15.

PnSTM1	PnSTM0	PnTGE1	PnTGE0	Operation mode	Description
0	0	–	–	Software start mode	Control the start/stop by writing PnRUN bit.
0	1	0	1	Software start mode or External input start mode	Control the start/stop by writing PnRUN bit. Also, can start the PWM by the external input "H" level and can stop / clear by the "L" level.
		1	0		Control the start/stop by writing PnRUN bit. Also, can start the PWM by the external input "L" level and can stop / clear by the "H" level.
		0	0		Control the start/stop by writing PnRUN bit. The external input control is disabled.
		1	1		
1	0	0	1	External input start mode	It can start the PWM by the riging edge of external input and can stop / clear by the falling edge.
		1	0		It can start the PWM by the falling edge of external input and can stop / clear by the riging edge.
		0	0		The external input control is disabled and the PWM does not work.
		1	1		
1	1	0	0	Software start mode or External input clear mode	Control the start/stop by writing PnRUN bit. The external input control is disabled.
		0	1		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the falling edge of external input.
		1	0		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the riging edge of external input.
		1	1		Control the start/stop by writing PnRUN bit. Also, can clear the PWM by the riging edge or falling edeg of external input.

n=6, 7

11.3.1 PWM4 and PWM5, Single mode / Repeat mode (P45MD="0", PnMD="0")

The PWM counter registers (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that are selected by the PWMn control register 0 (PWnCON0) when the PnRUN bit of PWMn control register 1 (PWnCON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn duty buffer (PWnDBUF) coincide, the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn period buffer (PWnPBUF) coincide, the PWM flag (PnFLG) is set to "1" on the next falling edge of PnCK and PWMn counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the PnRUN bit is set to "0", the PWM counter registers (PWnCH, PWnCL) stop counting after counting once the falling of the PWM clock (PnCK). Confirm that PWnCH and PWnCL are stopped by checking that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, PWnCH and PWnCL restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWM counter registers (PWnCH, PWnCL) to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWMn control register 0 (PWnCON0) and PWMn control register 6 (PW0CON6).
PWMn interrupt occurrence point and logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

External input can start / stop / clear the PWMn by setting the PnSTM1 bit and PnSTM0 bit of PWMn control register 2 (PWnCON2). The control edge or level is selected by the PnTGE0 bit and PnTGE1 bit and the external input pin is selected by PnTGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency

n=4, 5

After the PnRUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-3 shows the operation timing of PWMn on the condition of single mode and repeat mode (P45MD="0", PnMD="0").

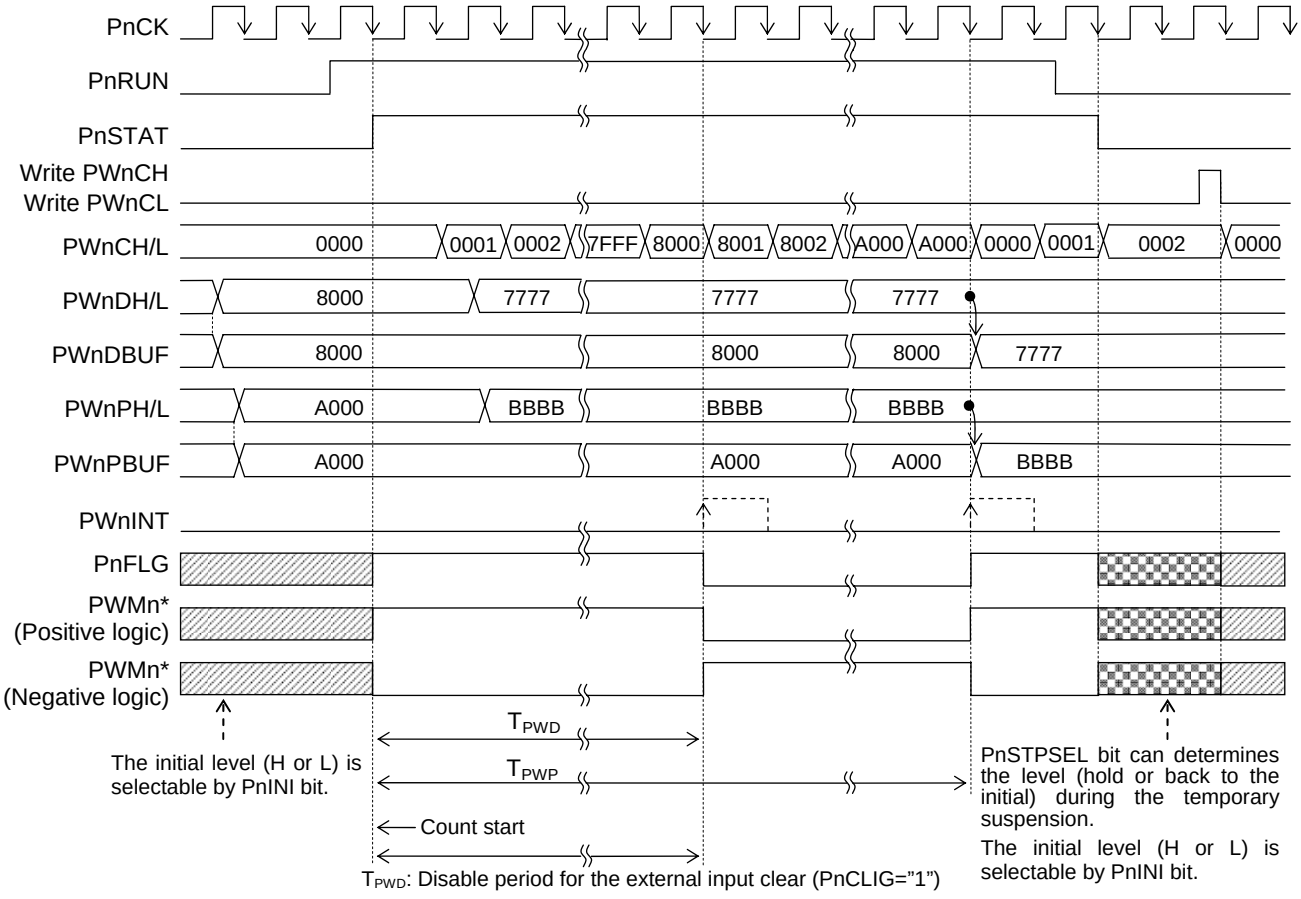


Figure 11-3 (1/2) PWMn Operating timing chart (PnMD="0", P45MD="0")

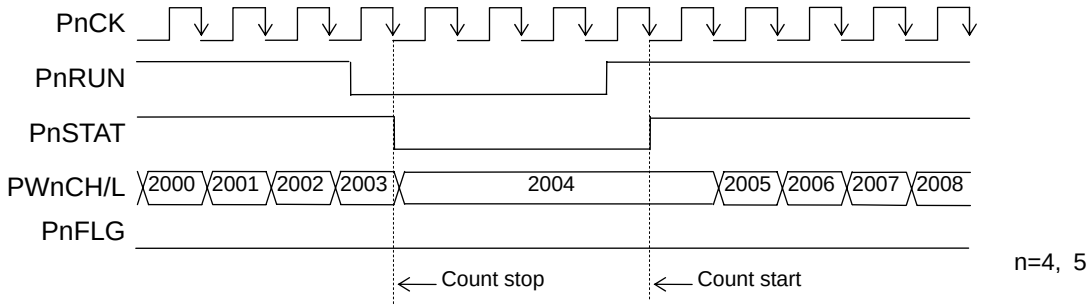


Figure 11-3 (2/2) PWMn Operating timing chart

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

11.3.2 PWM4 and PWM5, Single mode / One shot mode (P45MD="0", PnMD="1")

The PWM counter registers (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that are selected by the PWMn control register 0 (PWnCON0) when the PnRUN bit of PWMn control register 1 (PWnCON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn duty buffer (PWnDBUF) coincide, the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn period buffer (PWnPBUF) coincide, the PWM flag (PnFLG) is set to "1" on the next falling edge of PnCK and PWMn counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the PnRUN bit to "1" restarts incremental counting the PWM counter registers.

When the PnRUN bit is set to "0", the PWM counter registers (PWnCH, PWnCL) stop counting after counting once the falling of the PWM clock (PnCK). Confirm that PWnCH and PWnCL are stopped by checking that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, PWnCH and PWnCL restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWM counter registers (PWnCH, PWnCL) to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWMn control register 0 (PWnCON0) and PWMn control register 6 (PW0CON6).
PWMn interrupt occurrence point and logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

External input can start / stop / clear the PWMn by setting the PnSTM1 bit and PnSTM0 bit of PWMn control register 2 (PWnCON2). The control edge or level is selected by the PnTGE0 bit and PnTGE1 bit and the external input pin is selected by PnTGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency

n=4, 5

After the PnRUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued.
Figure 11-4 shows the operation timing of PWMn on the condition of single mode and repeat mode (P45MD="0", PnMD="1").

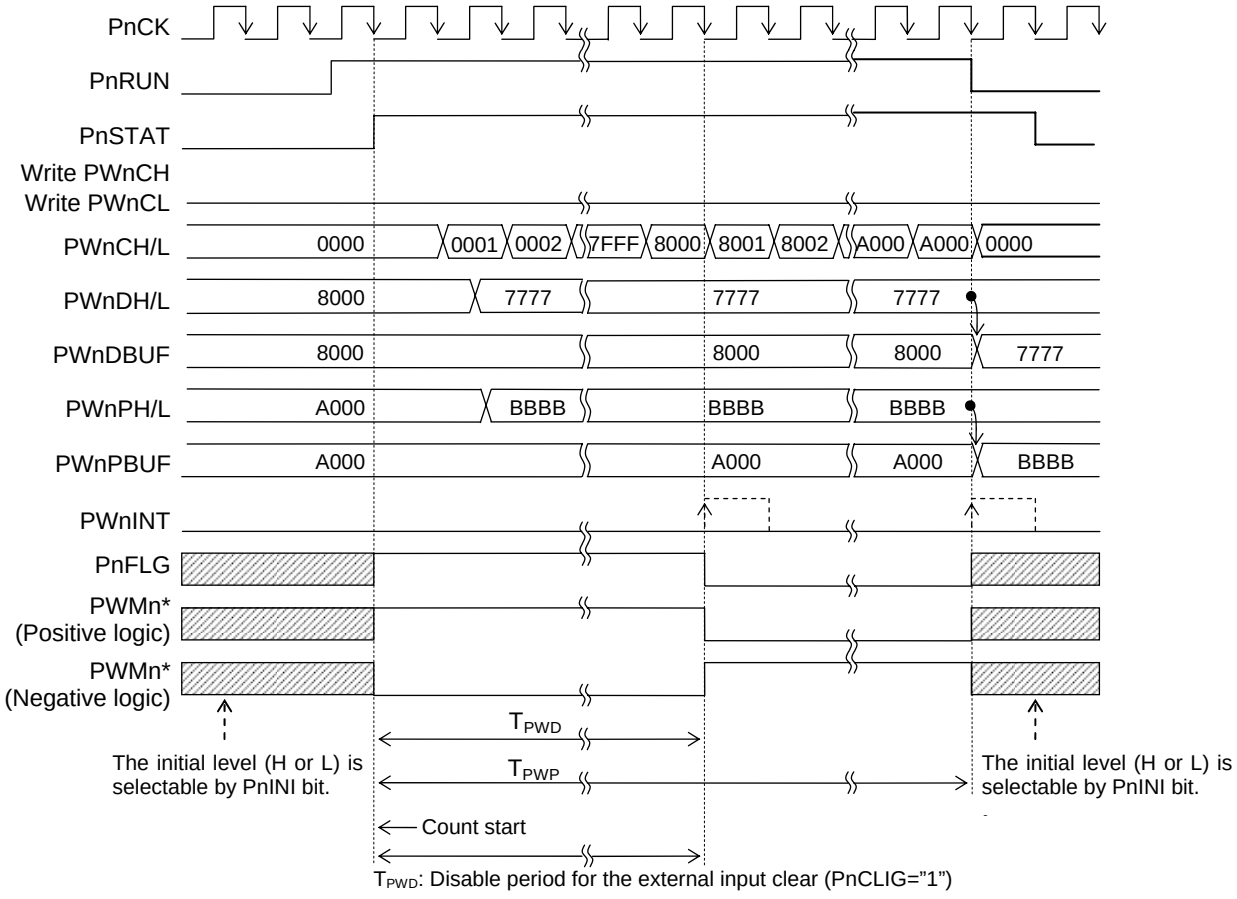


Figure 11-4 (1/2) PWMn Operating timing chart (PnMD="1", P45MD="0")

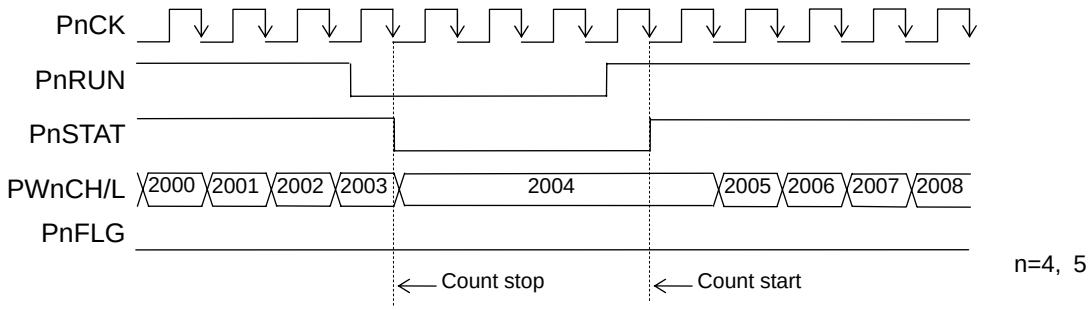


Figure 11-4 (2/2) PWMn Operating timing chart

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

11.3.3 PWM4 and PWM5, Coupled mode (with no dead-time specified) / Repeat mode (P45MD="1", P4DTMD="0", P4MD="0")

The PWM4 counter registers (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that are selected by the PWM4 control register 0 (PW4CON0) and the PWM4 control register 6 (PW4CON6) when the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 period buffer (PW5PBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 period buffer (PW5PBUF) coincide, the PWM4 flag (P4FLG) is set to "1" on the next falling edge of P4CK and the PWM4 counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P4RUN bit is set to "0", the PWM4 counter registers (PW4CH, PW4CL) stop counting after counting once the falling of the PWM clock (P4CK). Confirm that PW4CH and PW4CL are stopped by checking that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, PW4CH and PW4CL restarts incremental counting from the previous value on the falling edge of P4CK.

To initialize the PWM4 counter registers (PW4CH, PW4CL) to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM4 control register 0 (PW4CON0) and PWM4 control register 6 (PW0CON6).
PWM4 interrupt occurrence point and logic of the PWM4 output are selected by PWM4 control register 0 (PW4CON0). The logic of the PWM5 output are selected by PWM5 control register 0 (PW5CON0).

External input can start / stop / clear the PWMn by setting the P4STM1 bit and P4STM0 bit of PWM4 control register 2 (PW4CON2). The control edge or level is selected by the P4TGE0 bit and P4TGE1 bit and the external input pin is selected by P4TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM4 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM5 signal delay1 (T_{PWD1}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW5P + 1}{P4CK\ (Hz)}$$

PW4P:	PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D:	PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK:	Clock frequency specified by PWM4 control registers
PW5P:	PWM5 period registers (PW5PH, PW5PL) setting value (0001H to 0FFFFH)
PW5D:	PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-5 shows the operation timing of PWM4 and PWM5 on the condition of coupled mode with no dead-time specified (P45MD="1", P4DTMD="0") and repeat mode (P4MD="0").

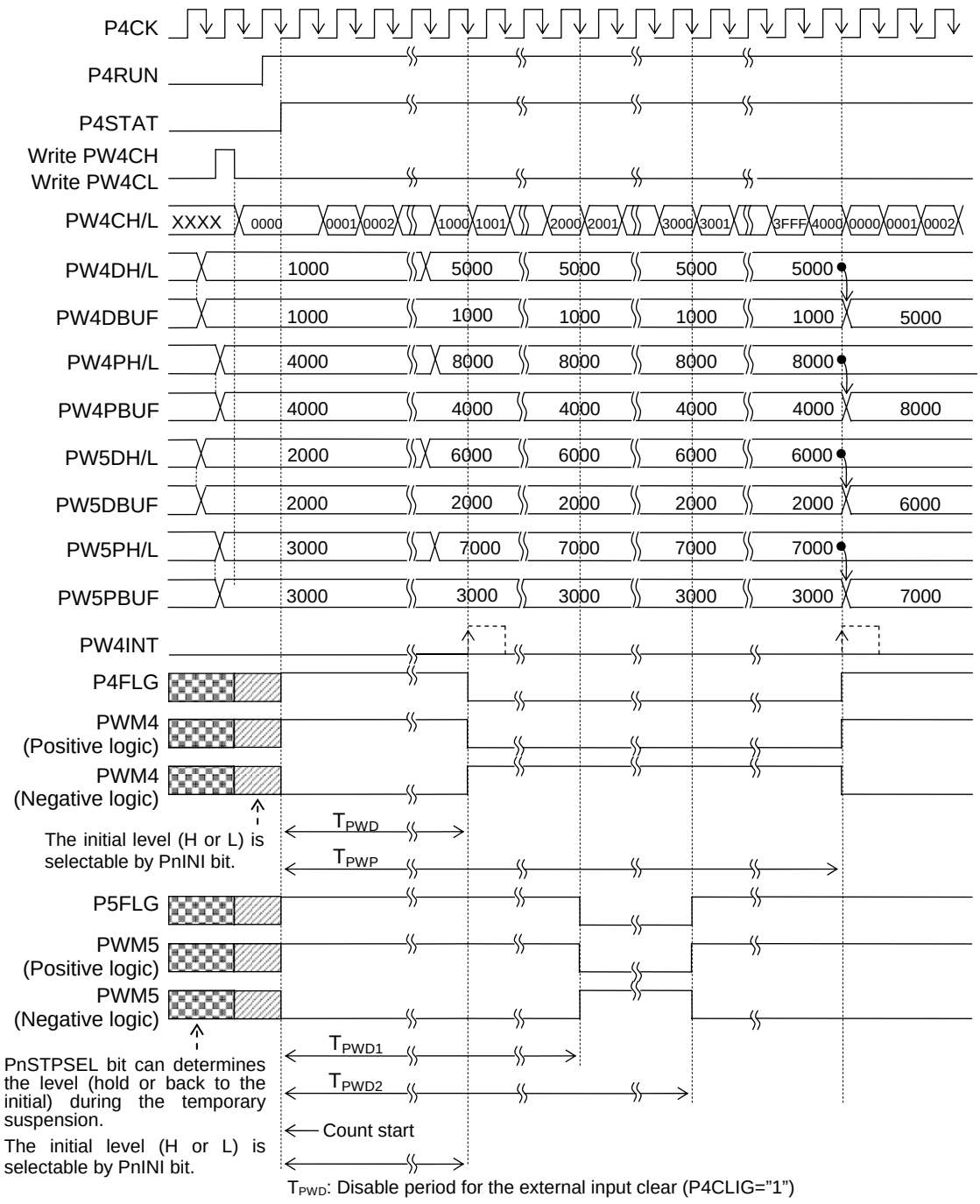


Figure 11-5 PWM4 and PWM5 Operating timing chart (P4MD="0", P45MD="1", P4DTMD="0")

11.3.4 PWM4 and PWM5, Coupled mode (with no dead-time specified) / One shot mode (P45MD="1", P4DTMD="0", P4MD="1")

The PWM4 counter registers (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that are selected by the PWM4 control register 0 (PW4CON0) and the PWM4 control register 6 (PW4CON6) when the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 period buffer (PW5PBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 period buffer (PW5PBUF) coincide, the PWM4 flag (P4FLG) is set to "1" on the next falling edge of P4CK and the PWM4 counter registers is set to "0000H", stops incremental counting and the P4RUN bit gets cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the P4RUN bit to "1" restarts incremental counting the PWM counter registers.

When the P4RUN bit is set to "0", the PWM4 counter registers (PW4CH, PW4CL) stop counting after counting once the falling of the PWM clock (P4CK). Confirm that PW4CH and PW4CL are stopped by checking that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, PW4CH and PW4CL restarts incremental counting from the previous value on the falling edge of P4CK.

To initialize the PWM4 counter registers (PW4CH, PW4CL) to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM4 control register 0 (PW4CON0) and PWM4 control register 6 (PW0CON6).
PWM4 interrupt occurrence point and logic of the PWM4 output are selected by PWM4 control register 0 (PW4CON0).

External input can start / stop / clear the PWMn by setting the P4STM1 bit and P4STM0 bit of PWM4 control register 2 (PW4CON2). The control edge or level is selected by the P4TGE0 bit and P4TGE1 bit and the external input pin is selected by P4TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM4 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM5 signal delay1 (T_{PWD1}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW5P + 1}{P4CK\ (Hz)}$$

PW4P:	PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D:	PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK:	Clock frequency specified by PWM4 control registers
PW5P:	PWM5 period registers (PW5PH, PW5PL) setting value (0001H to 0FFFFH)
PW5D:	PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-6 shows the operation timing of PWM4 and PWM5 on the condition of coupled mode with no dead-time specified (P45MD="1", P4DTMD="0") and one shot mode (P4MD="1").

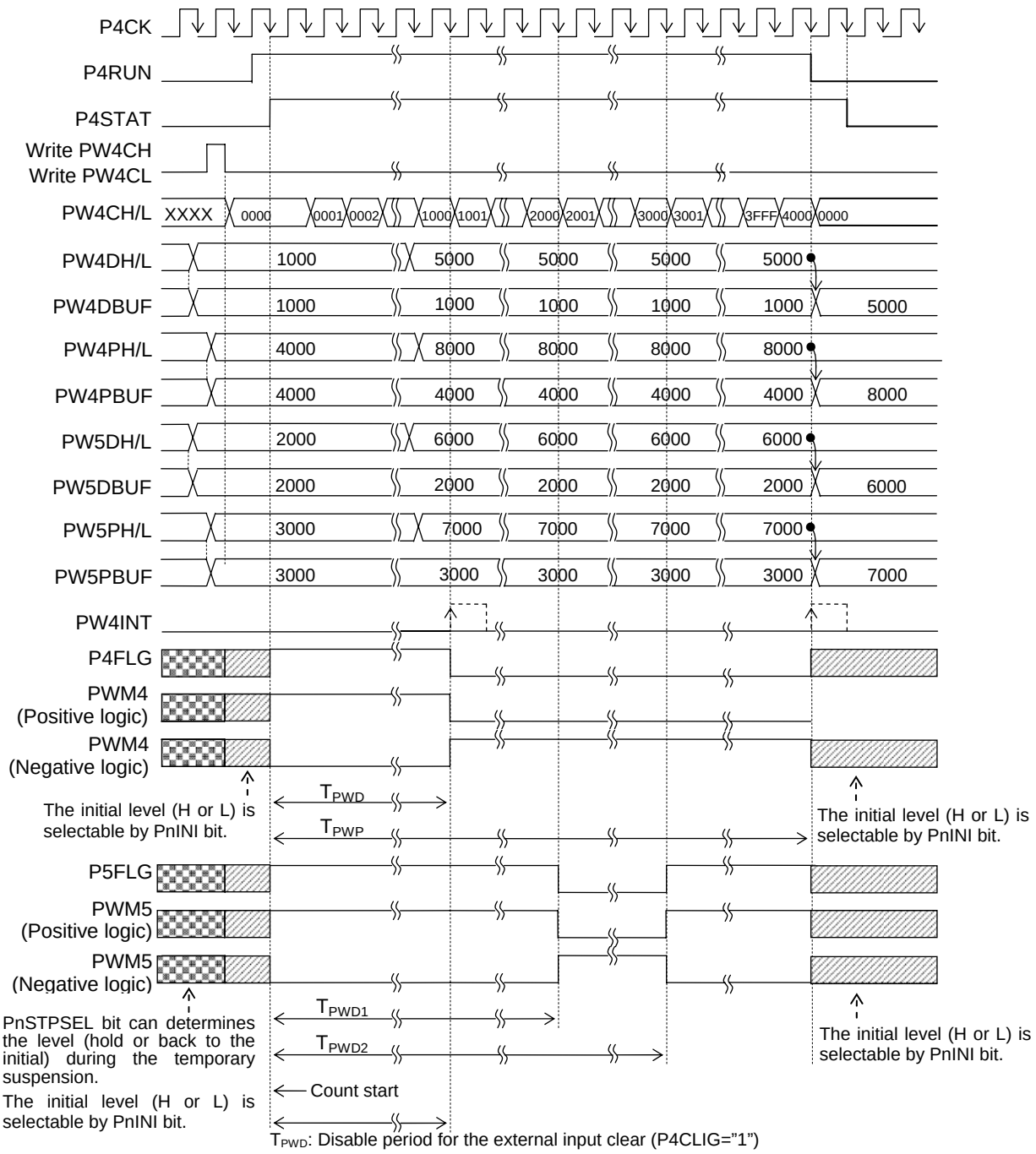


Figure 11-6 PWM4 and PWM5 Operating timing chart (P4MD="1", P45MD="1", P4DTMD="0")

11.3.5 PWM4 and PWM5, Coupled mode (with dead-time specified) / Repeat mode (P45MD="1", P4DTMD="1", P4MD="0")

The PWM4 counter registers (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that are selected by the PWM4 control register 0 (PW4CON0) and the PWM4 control register 6 (PW4CON6) when the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

Setting P4DTMD bit to "1" enables the dead-time to generate the timing that de-activates both PWM4 and PWM5 at the same time. Specifiy the value of dead-time into PW5DH and PW5DL registers.

When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the [PWM4 duty buffer] + [dead-time] (PW4DBUF + PW5DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 period buffer (PW5PBUF) coincide, the PWM4 flag (P4FLG) is set to "1" on the next falling edge of P4CK and the PWM4 counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P4RUN bit is set to "0", the PWM4 counter registers (PW4CH, PW4CL) stop counting after counting once the falling of the PWM clock (P4CK). Confirm that PW4CH and PW4CL are stopped by checking that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, PW4CH and PW4CL restarts incremental counting from the previous value on the falling edge of P4CK.

To initialize the PWM4 counter registers (PW4CH, PW4CL) to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM4 control register 0 (PW4CON0) and PWM4 control register 6 (PW0CON6).
PWM4 interrupt occurrence point and logic of the PWM4 output are selected by PWM4 control register 0 (PW4CON0).
The logic of the PWM5 output are selected by PWM5 control register 0 (PW5CON0).

External input can start / stop / clear the PWMn by setting the P4STM1 bit and P4STM0 bit of PWM4 control register 2 (PW4CON2). The control edge or level is selected by the P4TGE0 bit and P4TGE1 bit and the external input pin is selected by P4TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM4 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM5 dead-time (T_{DTM}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + PW5D + 2}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{DTM} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency specified by PWM4 control registers
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-7 shows the operation timing of PWM4 and PWM5 on the condition of coupled mode with dead-time specified (P45MD="1", P4DTMD="1") and repeat mode (P4MD="0").

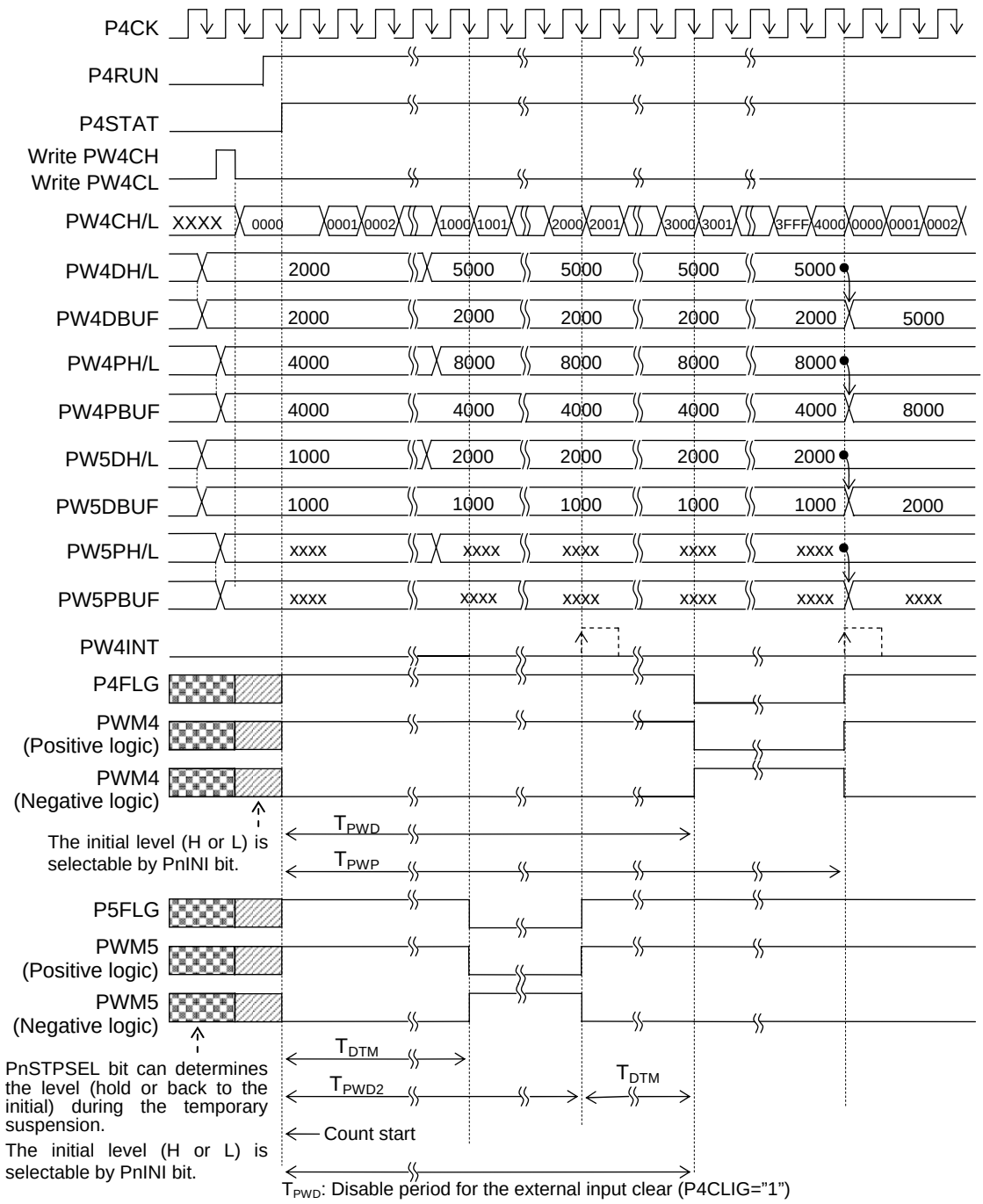


Figure 11-7 PWM4 and PWM5 Operating timing chart (P4MD="0", P45MD="1", P4DTMD="1")

Note:
PWM5 output is initially in a high-impedance output state before setting the port n control register 0 and 1 (PnCON0 and PnCON1). Fix the level with a pull-up or pull-down resister externally if needed.

11.3.6 PWM4 and PWM5, Coupled mode (with dead-time specified) / One shot mode (P45MD="1", P4DTMD="1", P4MD="1")

The PWM4 counter registers (PW4CH, PW4CL) are set to an operating state (P4STAT is set to "1") on the first falling edge of the PWM clock (P4CK) that are selected by the PWM4 control register 0 (PW4CON0) and the PWM4 control register 6 (PW4CON6) when the P4RUN bit of PWM4 control register 1 (PW4CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

Setting P4DTMD bit to "1" enables the dead-time to generate the timing that de-activates both PWM4 and PWM5 at the same time. Specifiy the value of dead-time into PW5DH and PW5DL registers.

When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the [PWM4 duty buffer] + [dead-time] (PW4DBUF + PW5DBUF) coincide, the PWM4 flag (P4FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM5 duty buffer (PW5DBUF) coincide, the PWM5 flag (P5FLG) is set to "0" on the next timer clock falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 duty buffer (PW4DBUF) coincide, the PWM5 flag (P5FLG) is set to "1" on the next falling edge of P4CK.
When the count value of PWM4 counter registers (PW4CH, PW4CL) and the value of the PWM4 period buffer (PW5PBUF) coincide, the PWM4 flag (P4FLG) is set to "1" on the next falling edge of P4CK and the PWM4 counter registers is set to "0000H", stops incremental counting and the P4RUN bit gets cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the P4RUN bit to "1" restarts incremental counting the PWM counter registers.

When the P4RUN bit is set to "0", the PWM4 counter registers (PW4CH, PW4CL) stop counting after counting once the falling of the PWM clock (P4CK). Confirm that PW4CH and PW4CL are stopped by checking that the P4STAT bit of the PWM4 control register 1 (PW4CON1) is "0". When the P4RUN bit is set to "1" again, PW4CH and PW4CL restarts incremental counting from the previous value on the falling edge of P4CK.

To initialize the PWM4 counter registers (PW4CH, PW4CL) to "0000H", perform write operation in either of PW4CH or PW4CL. At that time, P4FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM4 control register 0 (PW4CON0) and PWM4 control register 6 (PW0CON6).
PWM4 interrupt occurrence point and logic of the PWM4 output are selected by PWM4 control register 0 (PW4CON0). The logic of the PWM5 output are selected by PWM5 control register 0 (PW5CON0).

External input can start / stop / clear the PWMn by setting the P4STM1 bit and P4STM0 bit of PWM4 control register 2 (PW4CON2). The control edge or level is selected by the P4TGE0 bit and P4TGE1 bit and the external input pin is selected by P4TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.7 "PWM4/PWM5 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM4 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM5 dead-time (T_{DTM}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW4P + 1}{P4CK\ (Hz)}$$

$$T_{PWD} = \frac{PW4D + PW5D + 2}{P4CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW4D + 1}{P4CK\ (Hz)}$$

$$T_{DTM} = \frac{PW5D + 1}{P4CK\ (Hz)}$$

PW4P: PWM4 period registers (PW4PH, PW4PL) setting value (0001H to 0FFFFH)
PW4D: PWM4 duty registers (PW4DH, PW4DL) setting value (0000H to 0FFFEH)
P4CK: Clock frequency specified by PWM4 control registers
PW5D: PWM5 duty registers (PW5DH, PW5DL) setting value (0000H to 0FFFEH)

After the P4RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-8 shows the operation timing of PWM4 and PWM5 on the condition of coupled mode with dead-time specified (P45MD="1", P4DTMD="1") and one shot mode (P4MD="1").

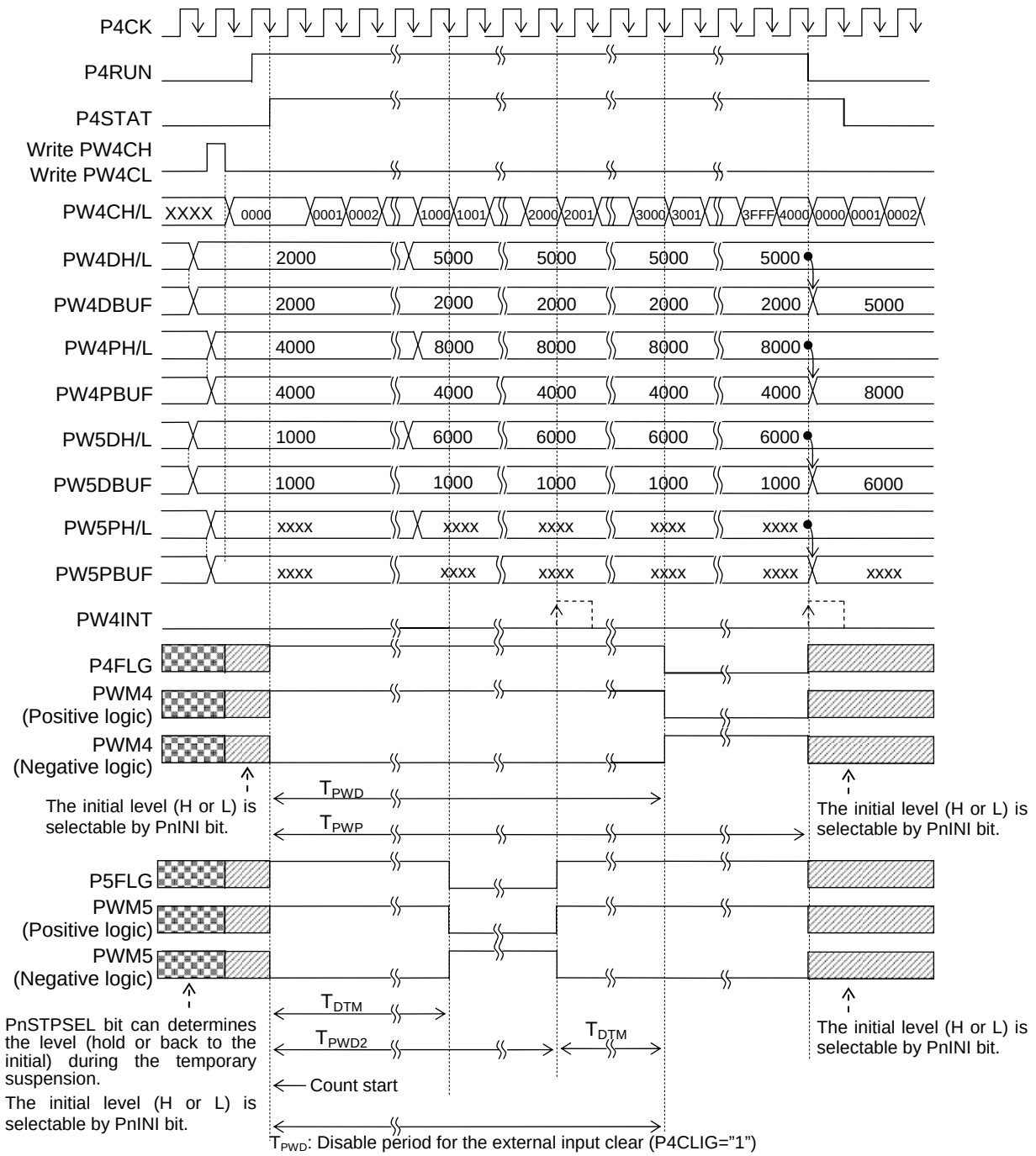
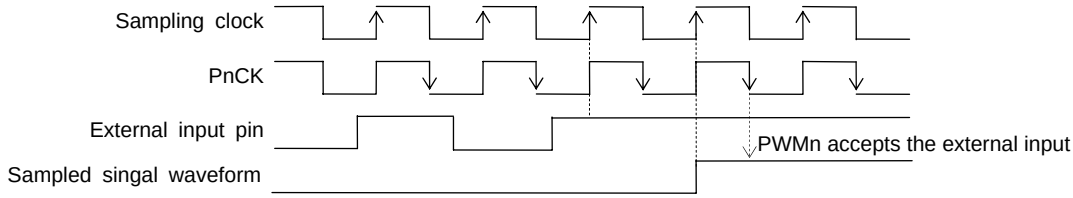


Figure 11-8 PWM4 and PWM5 Operating timing chart (P4MD="1", P45MD="1", P4DTMD="1")

Note:
PWM5 output is initially in a high-impedance output state before setting the port n control register 0 and 1 (PnCON0 and PnCON1). Fix the level with a pull-up or pull-down resister externally if needed.

11.3.7 PWM4/PWM5 start/stop/clear operation by the external control

The PWM counter registers (PWnCH, PWnCL) can be enabled to start, stop and clear with external triggering inputs, by setting PnSTM1 bit, PnSTM0 bit and PnTGSEL bit of PWMn control register 2 (PWnCON2). The external input is sampled with a clock to eliminate one clock or less pulse of noise. The sampling clock is determined by PnCS1 and PnCS0 bit. When OSCLK is selected the OSCLK (approx. 125ns) is used as the sampling clock and in the other cases LSCLK (approx. 30.5us) is used as the sampling clock.



11.3.7.1 Software Start Mode

With the setting of PnSTM1="0" and PnSTM0="0", the PWM counter operates being controlled by the PnRUN bit only. The operation timing is similar to the ones shown in 11.3.1 to 11.3.6.

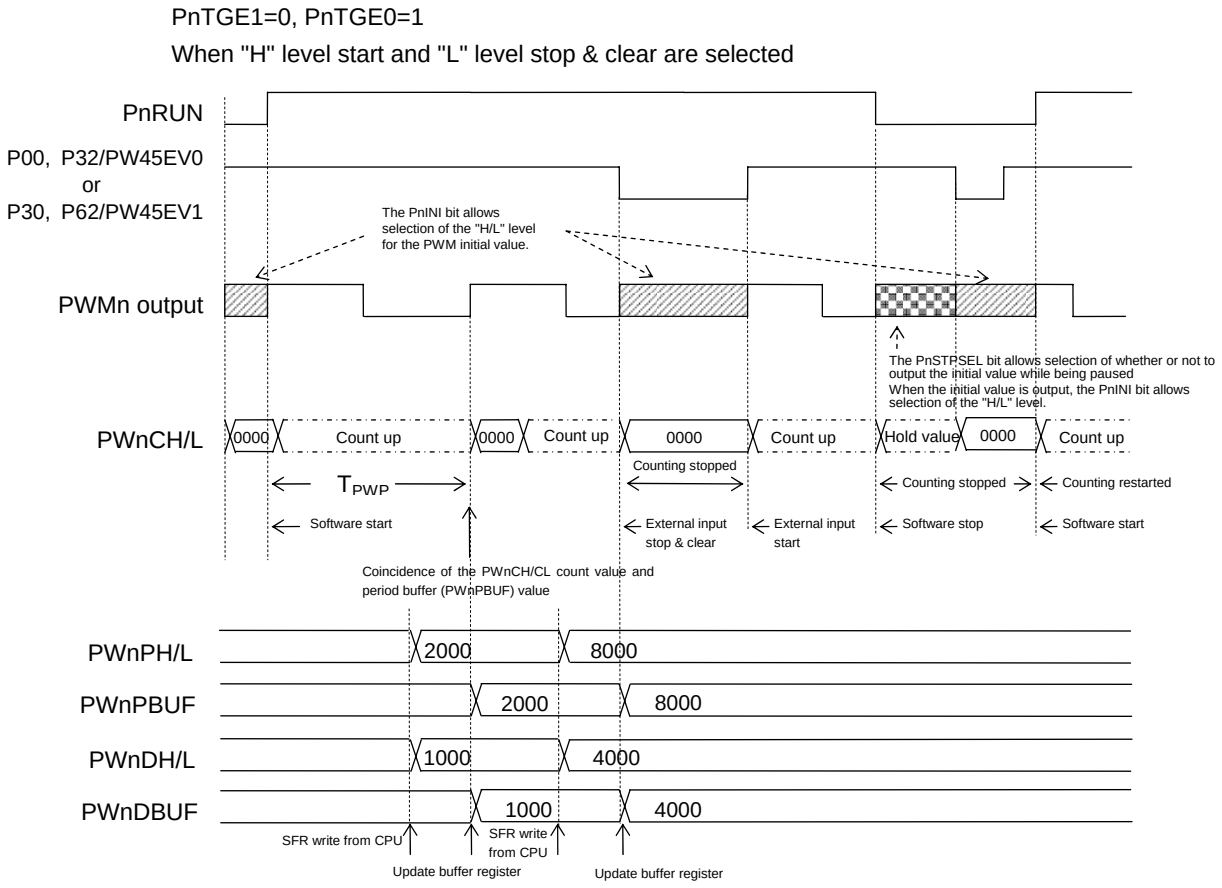
11.3.7.2 Software Start Mode or External Start Mode

With the setting of PnSTM1="0" and PnSTM0="1", the PWM counter operates being controlled by the external input (P00 or P32/PW45EV0, P30 or P62/PW45EV1) that is selected by the PnRUN and PnTGSEL bits.
When the selected external input gets an external input specified by PnTGE1 and PnTGE0 (PWnCON2 register), the PWM counter is started, stopped, or cleared. When the selected external input is fixed at the count start level, the counter operates in the same way as the software start.
However, when the selected external input is at the count stop level on the software start, the counter does not start, and it starts counting when the selected external input becomes the count start level.

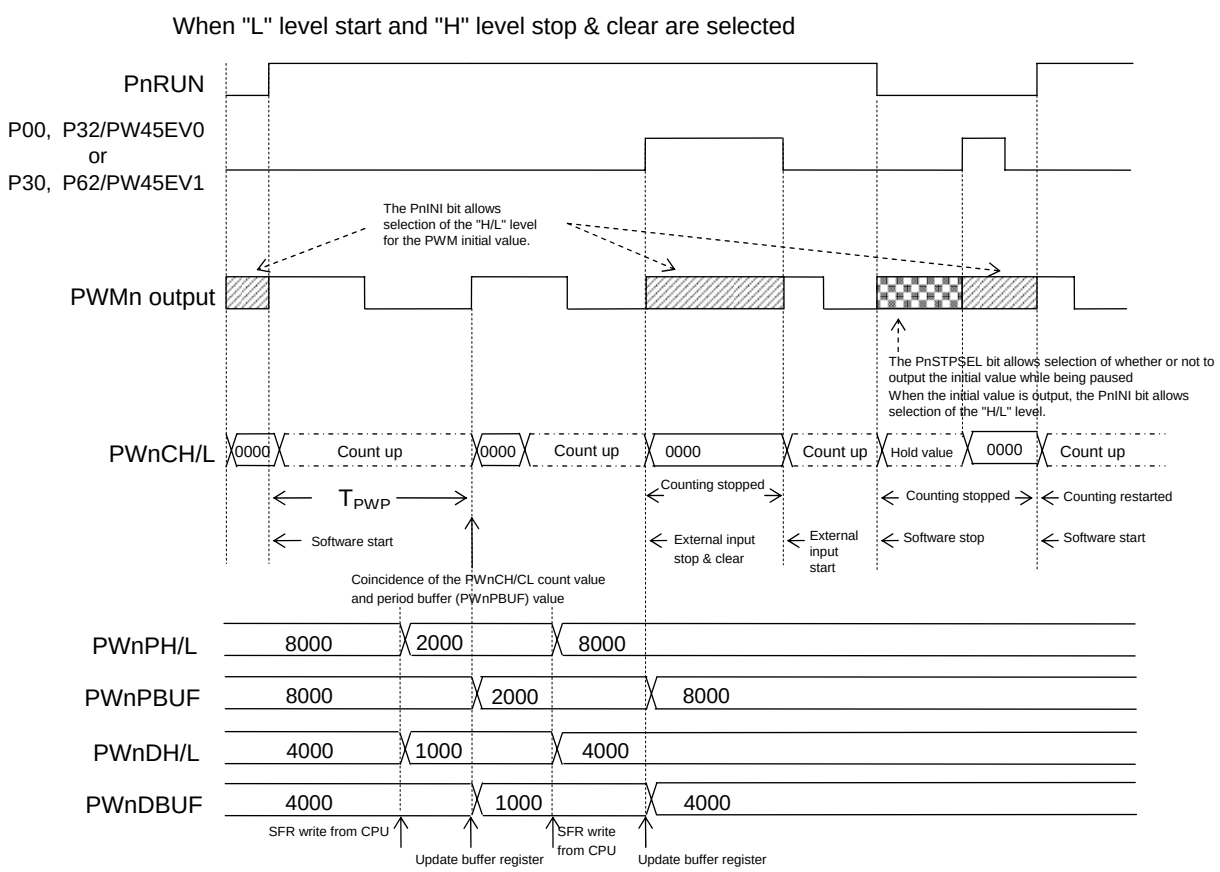
PnTGE1	PnTGE0	Count start edge	Count stop edge	Count start level	Count stop level
0	1	Rising edge	Falling edge	“H” level	“L” level
1	0	Falling edge	Rising edge	“L” level	“H” level

Note:
When stopping the counter by the external input, the counter always gets cleared.

Figure 11-9 shows the operation timing.



(a) Operation Timing Diagram with Software Start or External Input Start (PnTGE1=0, PnTGE0=1)



(b) Operation Timing Diagram with Software Start or External Input Start (PnTGE1=1, PnTGE0=0)

Figure 11-9 Operation Timing Diagram with Software Start or External Input Start (PnSTM1="0", PnSTM0="1")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

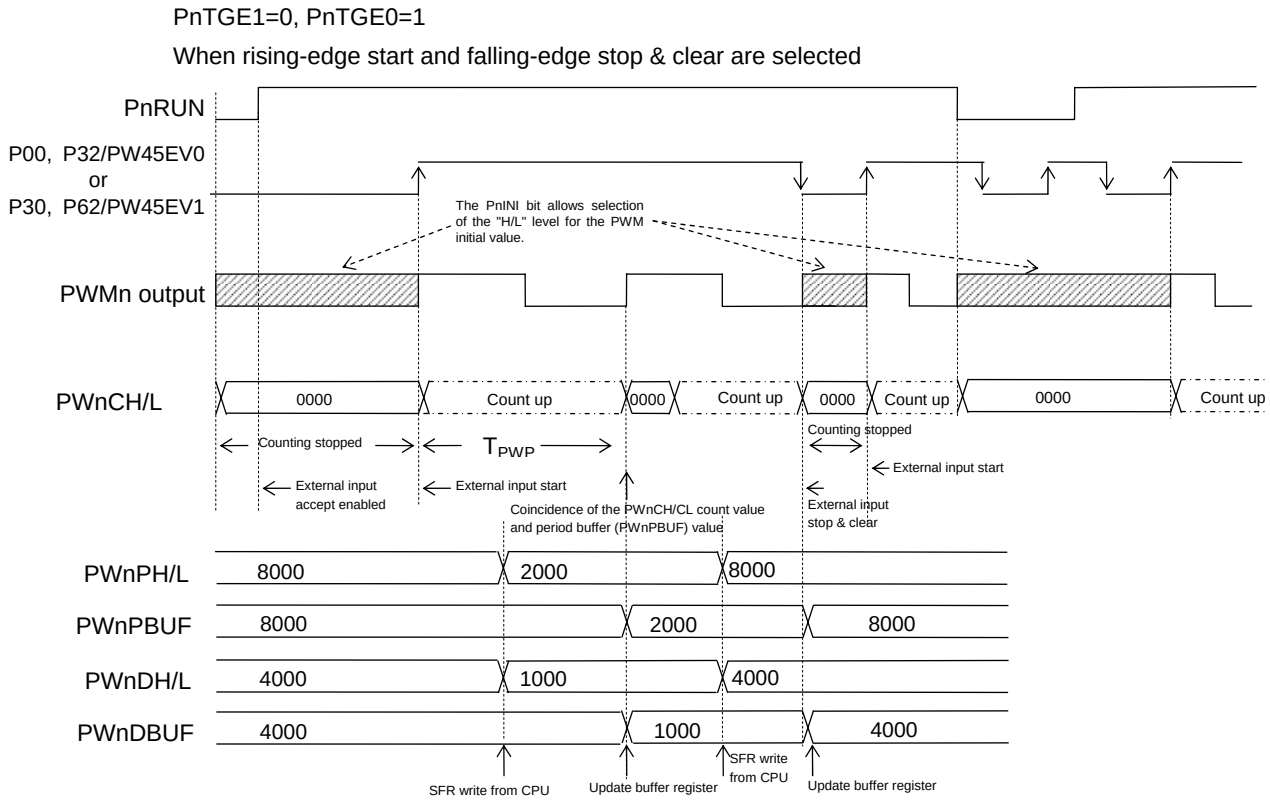
PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

11.3.7.3 External Input Start Mode

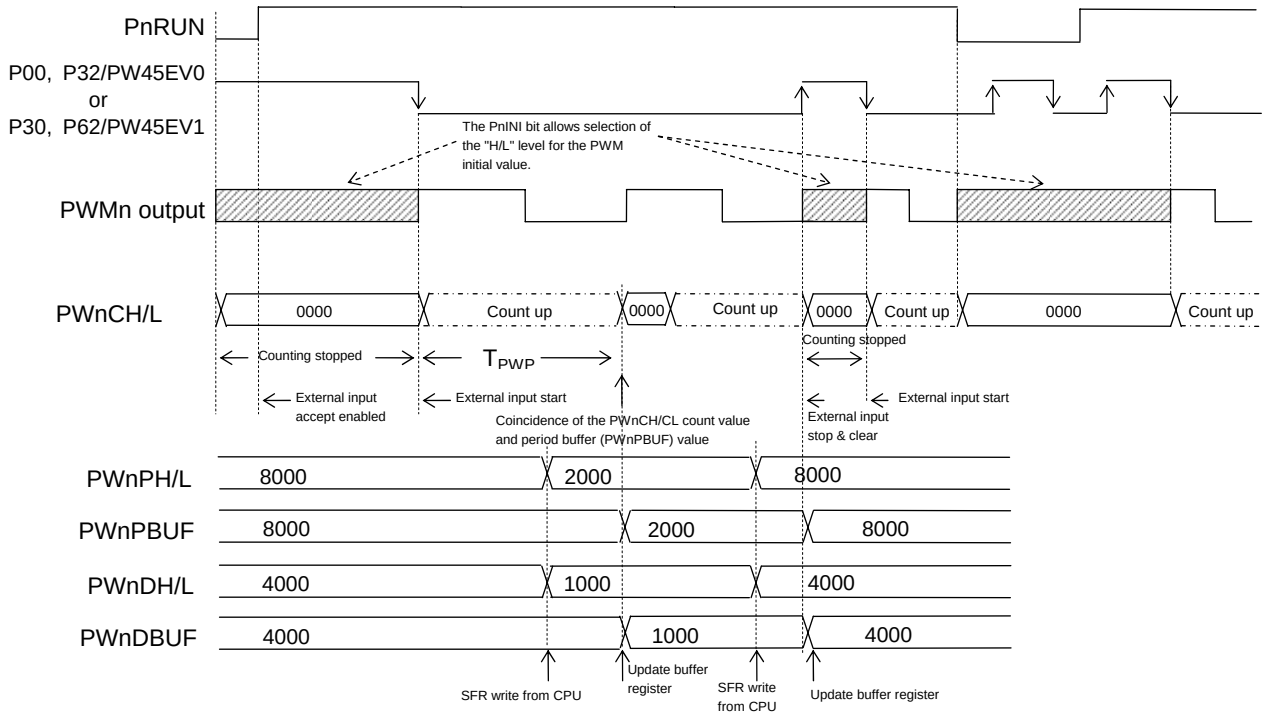
With the setting of PnSTM1="1" and PnSTM0="0" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the edge of the external input that is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2).
Note that the PnRUN bit is set to "1" in advance. If the PnRUN bit is "0", PWM will not operates even when the edge input occurs on the selected external input.
Figure 11-10 shows the operation timing.



(a) Operation Timing Diagram with External Input Start

PnTGE1=1, PnTGE0=0

When falling-edge start and rising-edge stop & clear are selected



(b) Operation Timing Diagram with External Input Start

Figure 11-10 Operation Timing Diagram with External Input Start (PnSTM1="1", PnSTM0="0")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

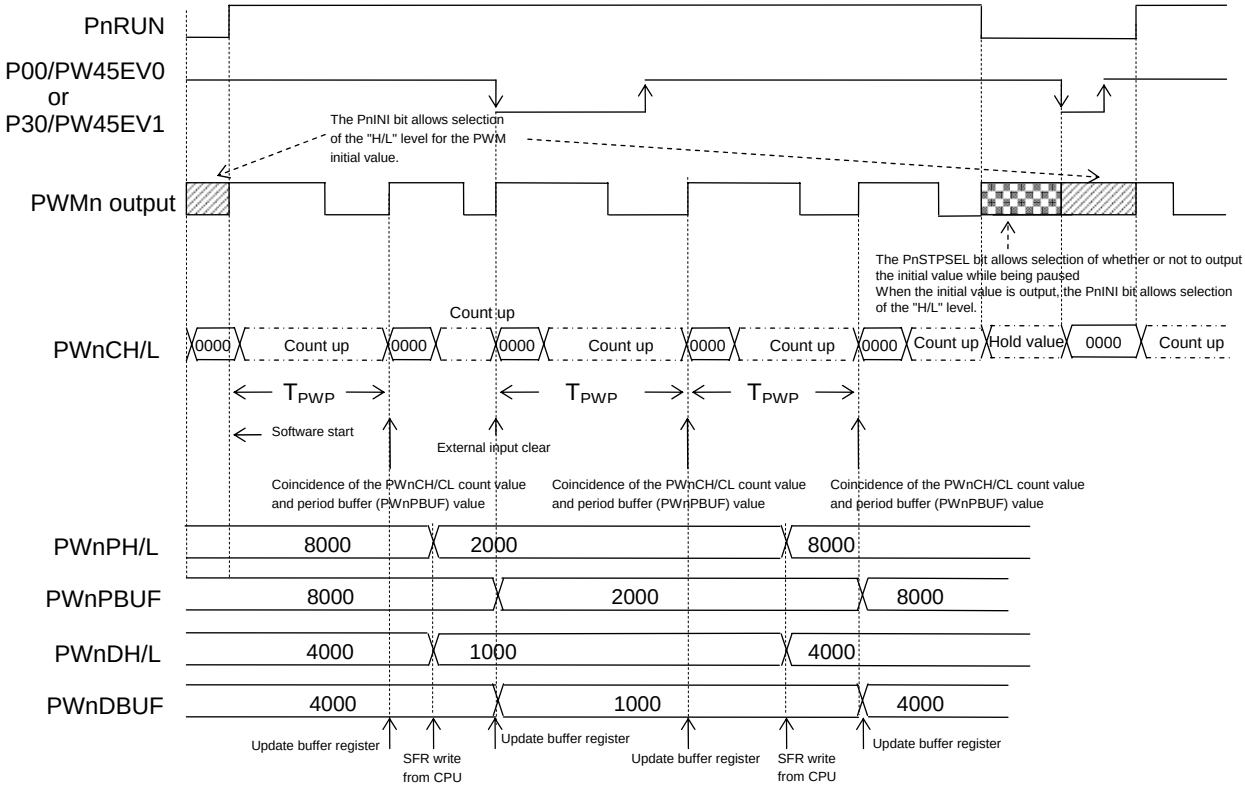
② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

11.3.7.4 Software Start or External Input Clear Mode

With the setting of PnSTM1="1" and PnSTM0="1" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the PnRUN bit.
When there is no edge input on the external input selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2), the counter operates in the same way as the software start. When the selected external input gets an edge input specified by PnTGE1 and PnTGE0, the PWM counter is cleared. The PnCLIG bit of the PWMn control register 0 (PWnCON0) allows enable/disable of the external clear input at the "H" level of the PWMn output flag (PnFLG).
Figure 11-11 shows the operation timing.

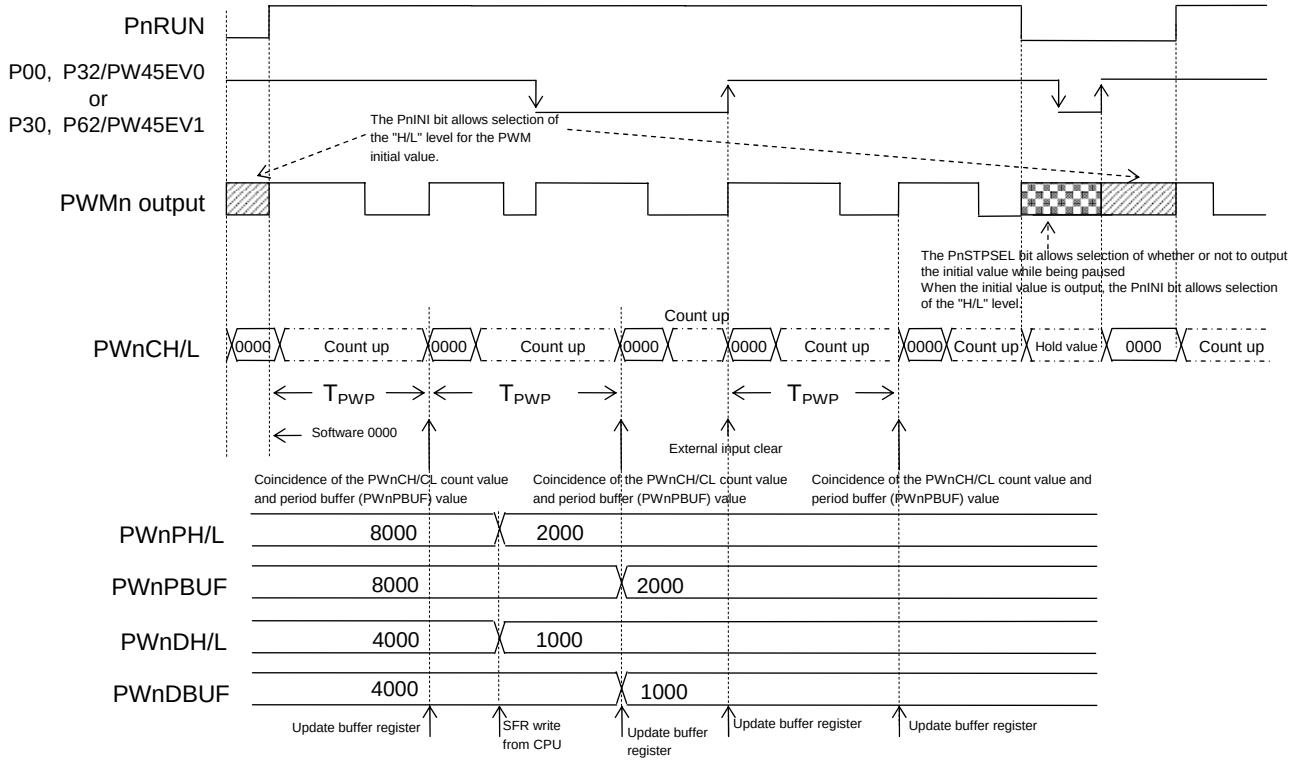
PnTGE1=0, PnTGE0=1
When falling-edge clear is selected



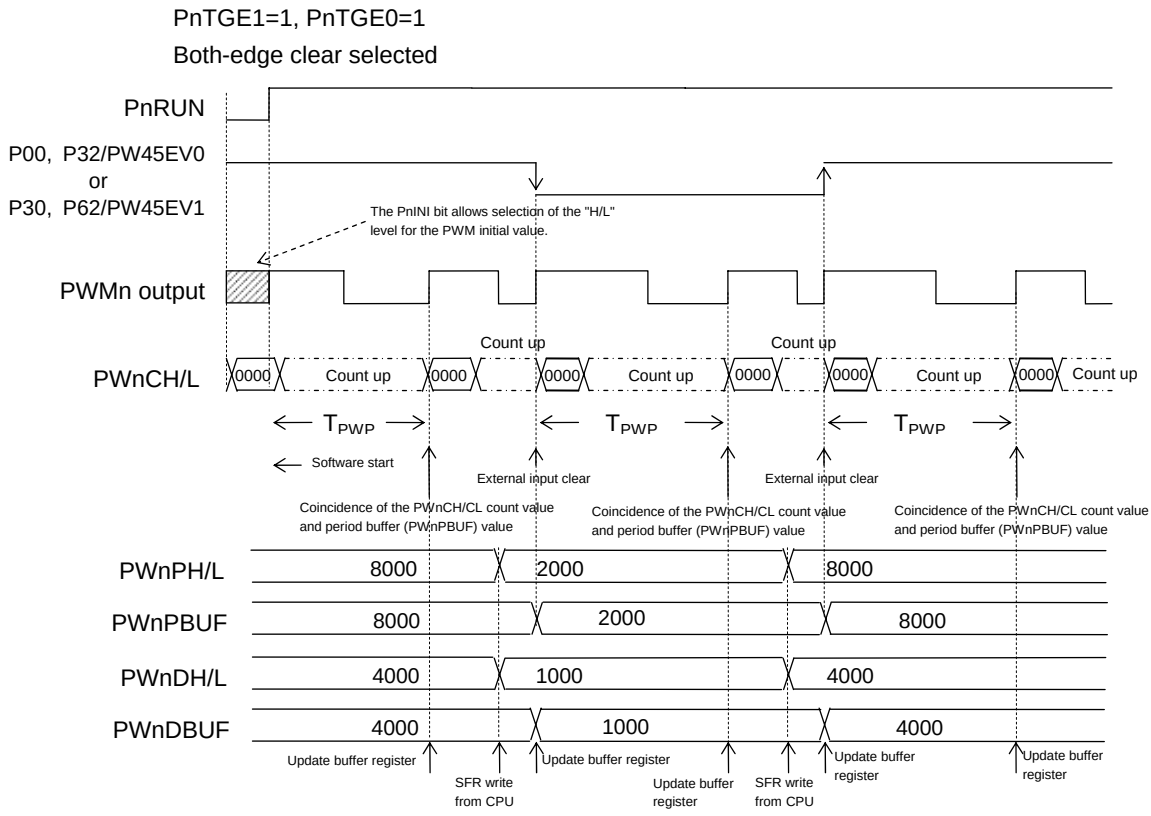
(a) Operation Timing Diagram with Software Start and External Input Clear

PnTGE1=1, PnTGE0=0

When rising-edge clear is selected



(b) Operation Timing Diagram with Software Start and External Input Clear



(c) Operation Timing Diagram with Software Start and External Input Clear

Figure 11-11 Operation Timing Diagram with Software Start and External Input Clear

For clear control by the external input, the values of the PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) are transferred to the PWMn duty buffer (PWnDBUF) and PWMn period buffer (PWnPBUF) respectively at the timing of the external input pins and edges specified by PnTGSEL, PnTGE1, and PnTGE0.

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the software start or external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P4CK/P5CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

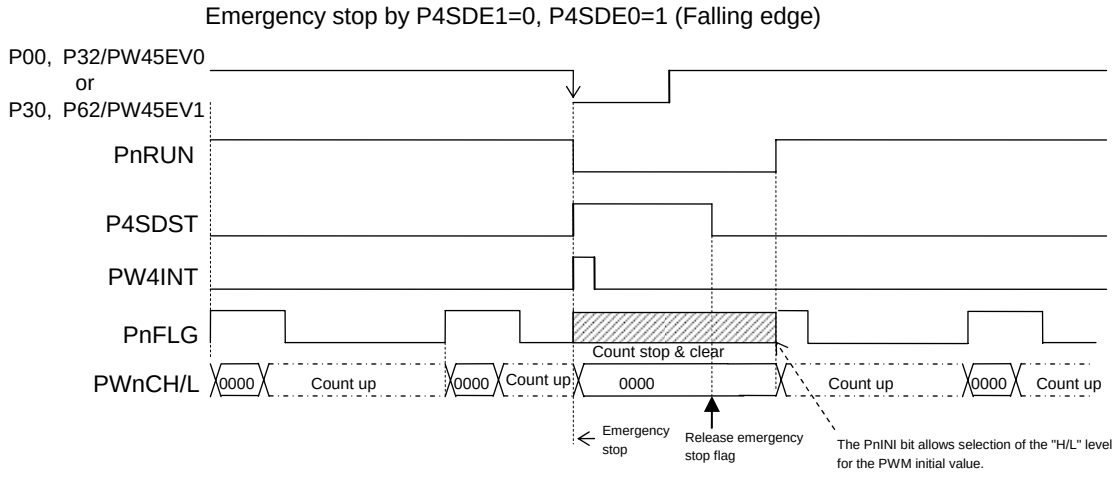
② When the external input clear control is done at a timing when PWMnPH/L or PWMnDH/L is changed while the PWM count is being paused, transfer to the PWMn duty buffer (PWnDBUF) or PWMn period buffer (PWnPBUF) may delay for one PWM clock.

11.3.8 Emergency Stop Operation

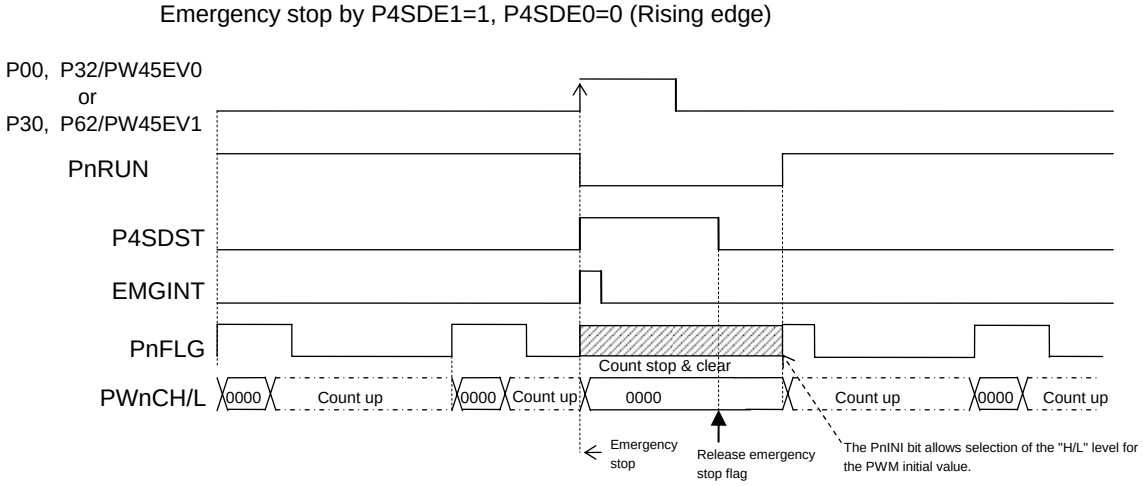
Setting the P4SDE1 and P4SDE0 bits of the PWM4 control register 3 (PW4CON3) enables the emergency stop function with the external input that is selected by P4TGSEL. Note that the emergency stop function is valid only in the cooperation mode (P45MD="1").

When the external input that is selected by the P4TGSEL bit gets an edge input specified by P4SDE1 an P4SDE0, the emergency stop flag (P4SDST) is set to "1", an emergency stop interrupt (PW4INT) is generated, and the PWM counter is stopped/cleared. Because the PWM flag output (PnFLG) is cleared, the PWM4 and PWM5 outputs are turned off simultaneously.

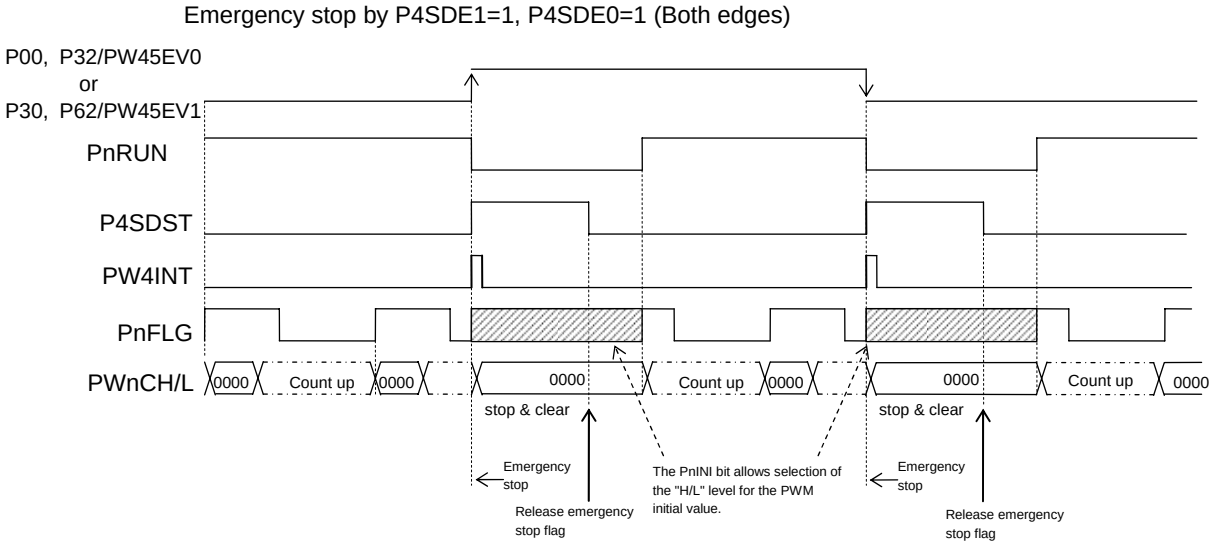
To release the emergency stop flag, write "1" to P4SDST of the PWM4 control register 3 (PW4CON3).
Figure 11-12 shows the operation timing.



(a) Timing with Falling-edge operation



(b) Timing with Rising-edge operation



(c) Timing with Both-edge operation

Figure 11-12 Operation Timing Diagram at Emergency Stop

11.3.9 PWM6 and PWM7, Single mode / Repeat mode (P67MD="0", PnMD="0")

The PWM counter registers (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that are selected by the PWMn control register 0 (PWnCON0) when the PnRUN bit of PWMn control register 1 (PWnCON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn duty buffer (PWnDBUF) coincide, the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn period buffer (PWnPBUF) coincide, the PWM flag (PnFLG) is set to "1" on the next falling edge of PnCK and PWMn counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the PnRUN bit is set to "0", the PWM counter registers (PWnCH, PWnCL) stop counting after counting once the falling of the PWM clock (PnCK). Confirm that PWnCH and PWnCL are stopped by checking that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, PWnCH and PWnCL restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWM counter registers (PWnCH, PWnCL) to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWMn control register 0 (PWnCON0) and PWMn control register 6 (PW0CON6).
PWMn interrupt occurrence point and logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

External input can start / stop / clear the PWMn by setting the PnSTM1 bit and PnSTM0 bit of PWMn control register 2 (PWnCON2). The control edge or level is selected by the PnTGE0 bit and PnTGE1 bit and the external input pin is selected by PnTGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency

n=6, 7

After the PnRUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-13 shows the operation timing of PWMn on the condition of single mode and repeat mode (P67MD="0", PnMD="0").

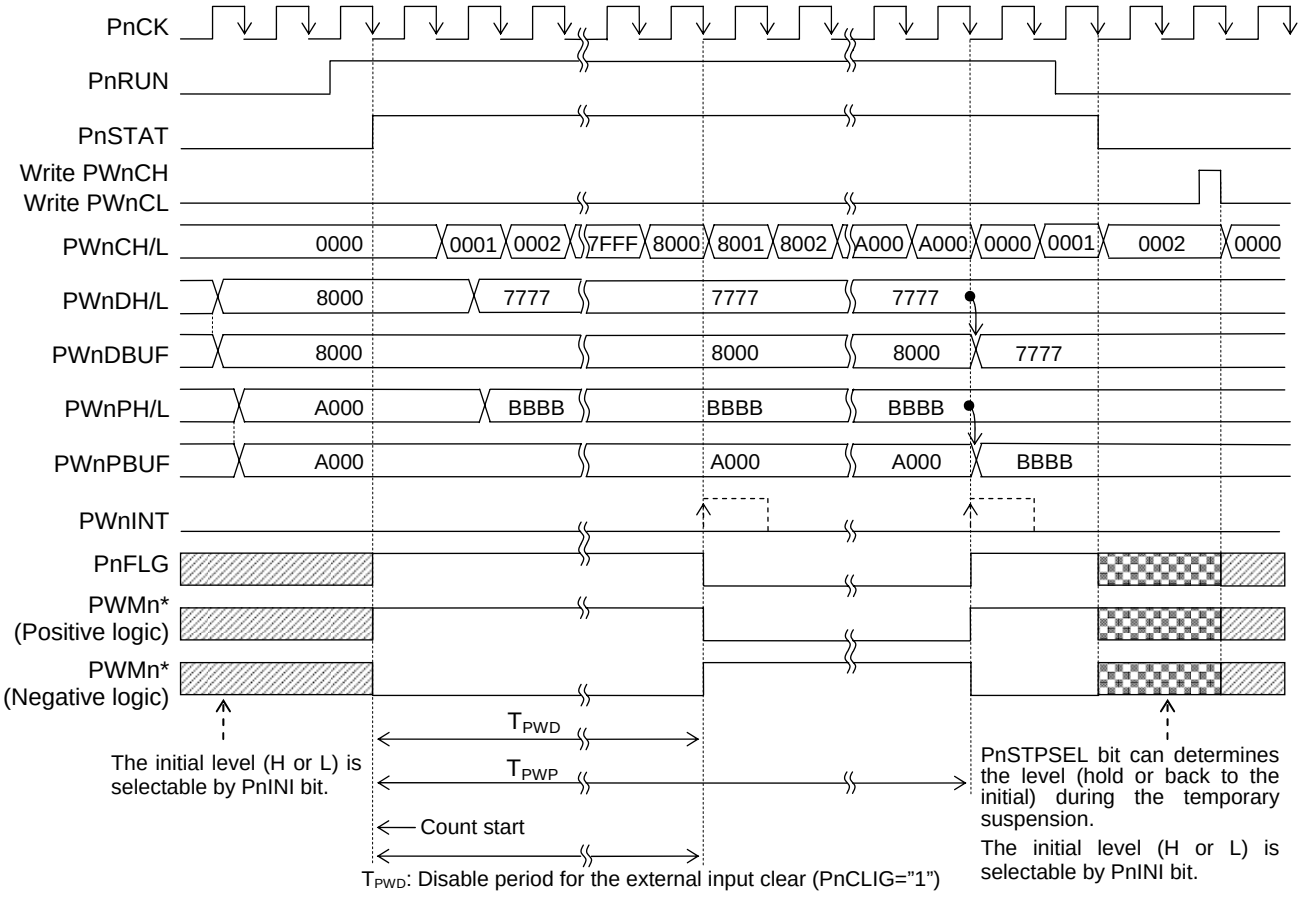


Figure 11-13 (1/2) PWMn Operating timing chart (PnMD="0", P67MD="0")

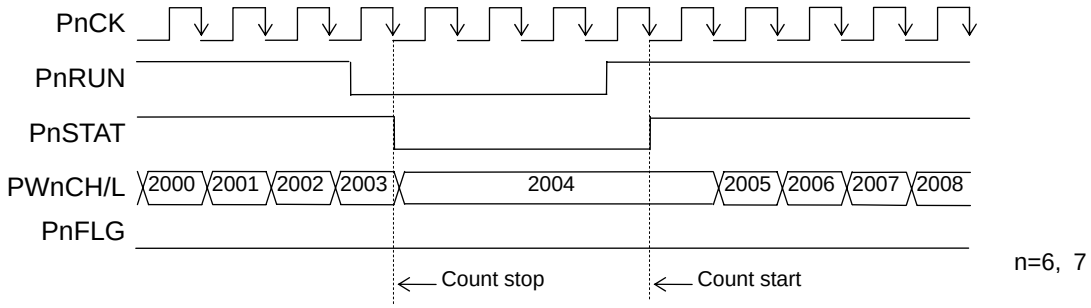


Figure 11-13 (2/2) PWMn Operating timing chart

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

11.3.10 PWM6 and PWM7, Single mode / One shot mode (P67MD="0", PnMD="1")

The PWM counter registers (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWM clock (PnCK) that are selected by the PWMn control register 0 (PWnCON0) when the PnRUN bit of PWMn control register 1 (PWnCON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn duty buffer (PWnDBUF) coincide, the PWM flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the count value of PWM counter registers (PWnCH, PWnCL) and the value of the PWMn period buffer (PWnPBUF) coincide, the PWM flag (PnFLG) is set to "1" on the next falling edge of PnCK and PWMn counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the PnRUN bit to "1" restarts incremental counting the PWM counter registers.

When the PnRUN bit is set to "0", the PWM counter registers (PWnCH, PWnCL) stop counting after counting once the falling of the PWM clock (PnCK). Confirm that PWnCH and PWnCL are stopped by checking that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, PWnCH and PWnCL restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWM counter registers (PWnCH, PWnCL) to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWMn control register 0 (PWnCON0) and PWMn control register 6 (PW0CON6).
PWMn interrupt occurrence point and logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

External input can start / stop / clear the PWMn by setting the PnSTM1 bit and PnSTM0 bit of PWMn control register 2 (PWnCON2). The control edge or level is selected by the PnTGE0 bit and PnTGE1 bit and the external input pin is selected by PnTGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency

n=6, 7

After the PnRUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued.
Figure 11-14 shows the operation timing of PWMn on the condition of single mode and repeat mode (P67MD="0", PnMD="1").

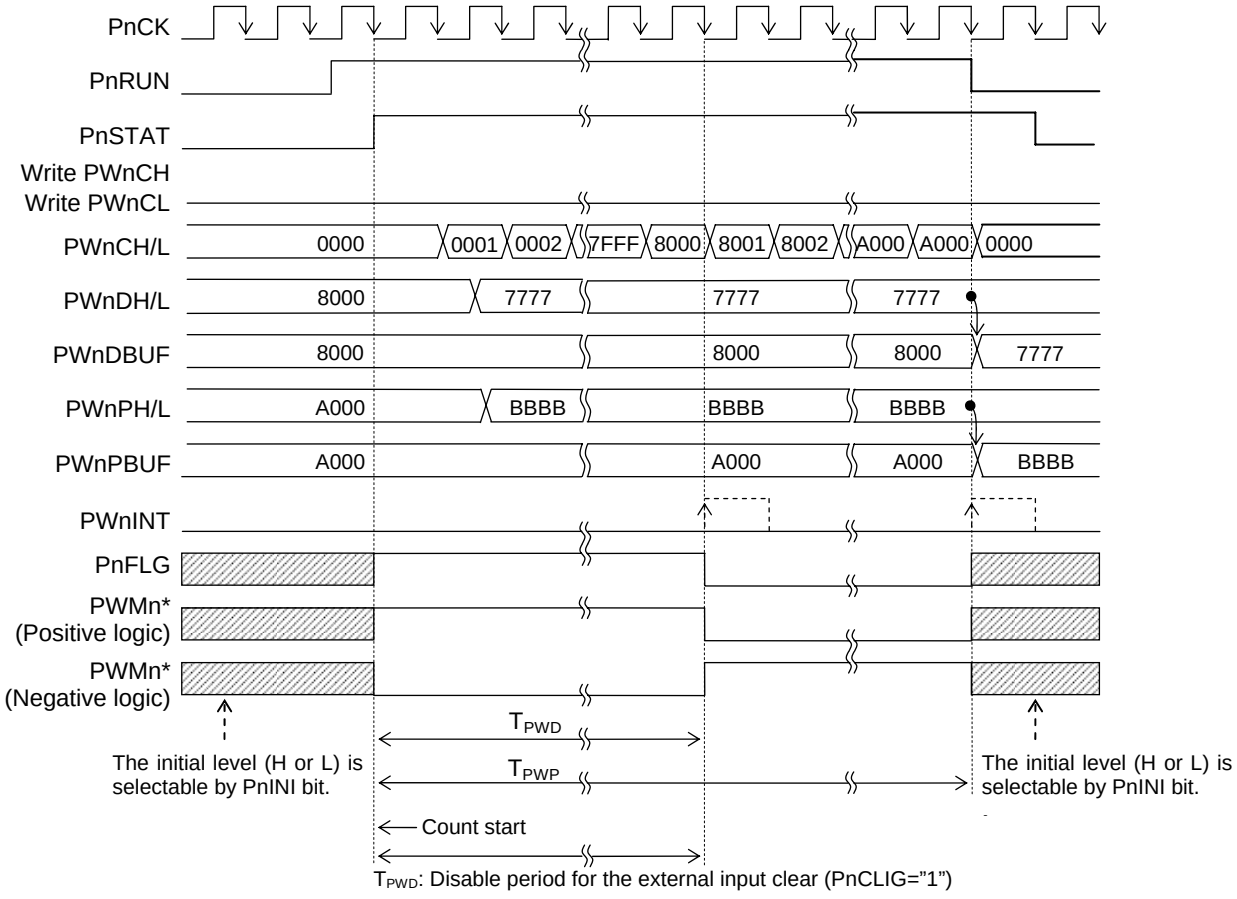


Figure 11-14 (1/2) PWMn Operating timing chart (PnMD="1", P67MD="0")

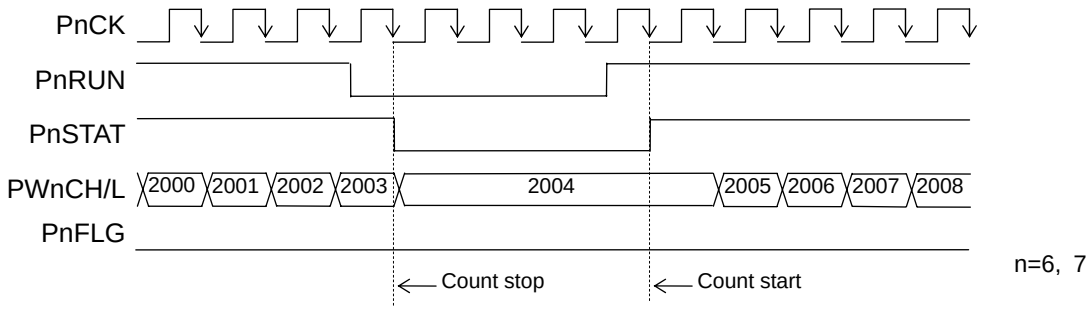


Figure 11-14 (2/2) PWMn Operating timing chart

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWM clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.

11.3.11 PWM6 and PWM7, Coupled mode (with no dead-time specified) / Repeat mode (P67MD="1", P6DTMD="0", P6MD="0")

The PWM6 counter registers (PW6CH, PW6CL) are set to an operating state (P6STAT is set to "1") on the first falling edge of the PWM clock (P6CK) that are selected by the PWM6 control register 0 (PW6CON0) and the PWM6 control register 6 (PW6CON6) when the P6RUN bit of PWM6 control register 1 (PW6CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 duty buffer (PW6DBUF) coincide, the PWM6 flag (P6FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 duty buffer (PW7DBUF) coincide, the PWM7 flag (P7FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 period buffer (PW7PBUF) coincide, the PWM7 flag (P7FLG) is set to "1" on the next falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 period buffer (PW7PBUF) coincide, the PWM6 flag (P6FLG) is set to "1" on the next falling edge of P6CK and the PWM6 counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P6RUN bit is set to "0", the PWM6 counter registers (PW6CH, PW6CL) stop counting after counting once the falling of the PWM clock (P6CK). Confirm that PW6CH and PW6CL are stopped by checking that the P6STAT bit of the PWM6 control register 1 (PW6CON1) is "0". When the P6RUN bit is set to "1" again, PW6CH and PW6CL restarts incremental counting from the previous value on the falling edge of P6CK.

To initialize the PWM6 counter registers (PW6CH, PW6CL) to "0000H", perform write operation in either of PW6CH or PW6CL. At that time, P6FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM6 control register 0 (PW6CON0) and PWM6 control register 6 (PW0CON6).
PWM6 interrupt occurrence point and logic of the PWM6 output are selected by PWM6 control register 0 (PW6CON0). The logic of the PWM7 output are selected by PWM7 control register 0 (PW7CON0).

External input can start / stop / clear the PWMn by setting the P6STM1 bit and P6STM0 bit of PWM6 control register 2 (PW6CON2). The control edge or level is selected by the P6TGE0 bit and P6TGE1 bit and the external input pin is selected by P6TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM6 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM7 signal delay1 (T_{PWD1}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW6P + 1}{P6CK\ (Hz)}$$

$$T_{PWD} = \frac{PW6D + 1}{P6CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW7D + 1}{P6CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW7P + 1}{P6CK\ (Hz)}$$

PW6P:	PWM6 period registers (PW6PH, PW6PL) setting value (0001H to 0FFFFH)
PW6D:	PWM6 duty registers (PW6DH, PW6DL) setting value (0000H to 0FFFEH)
P6CK:	Clock frequency specified by PWM6 control registers
PW7P:	PWM7 period registers (PW7PH, PW7PL) setting value (0001H to 0FFFFH)
PW7D:	PWM7 duty registers (PW7DH, PW7DL) setting value (0000H to 0FFFEH)

After the P6RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-15 shows the operation timing of PWM6 and PWM7 on the condition of coupled mode with no dead-time specified (P67MD="1", P6DTMD="0") and repeat mode (P6MD="0").

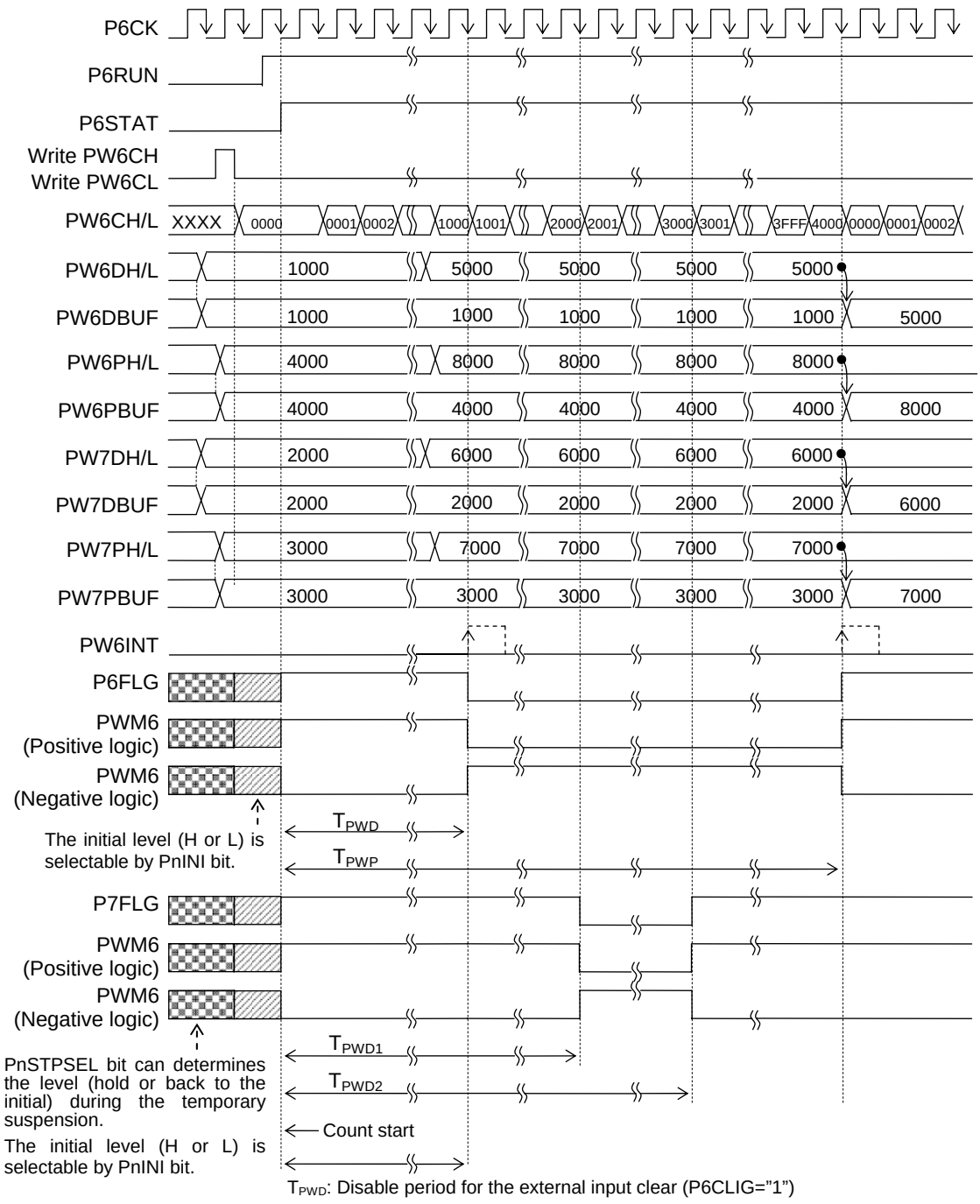


Figure 11-15 PWM6 and PWM7 Operating timing chart (P6MD="0", P67MD="1", P6DTMD="0")

11.3.12 PWM6 and PWM7, Coupled mode (with no dead-time specified) / One shot mode (P67MD="1", P6DTMD="0", P6MD="1")

The PWM6 counter registers (PW6CH, PW6CL) are set to an operating state (P6STAT is set to "1") on the first falling edge of the PWM clock (P6CK) that are selected by the PWM6 control register 0 (PW6CON0) and the PWM6 control register 6 (PW6CON6) when the P6RUN bit of PWM6 control register 1 (PW6CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 duty buffer (PW6DBUF) coincide, the PWM6 flag (P6FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 duty buffer (PW7DBUF) coincide, the PWM7 flag (P7FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 period buffer (PW7PBUF) coincide, the PWM7 flag (P7FLG) is set to "1" on the next falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 period buffer (PW7PBUF) coincide, the PWM6 flag (P6FLG) is set to "1" on the next falling edge of P6CK and the PWM6 counter registers is set to "0000H", stops incremental counting and the P6RUN bit gets cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the P6RUN bit to "1" restarts incremental counting the PWM counter registers.

When the P6RUN bit is set to "0", the PWM6 counter registers (PW6CH, PW6CL) stop counting after counting once the falling of the PWM clock (P6CK). Confirm that PW6CH and PW6CL are stopped by checking that the P6STAT bit of the PWM6 control register 1 (PW6CON1) is "0". When the P6RUN bit is set to "1" again, PW6CH and PW6CL restarts incremental counting from the previous value on the falling edge of P6CK.

To initialize the PWM6 counter registers (PW6CH, PW6CL) to "0000H", perform write operation in either of PW6CH or PW6CL. At that time, P6FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM6 control register 0 (PW6CON0) and PWM6 control register 6 (PW0CON6).
PWM6 interrupt occurrence point and logic of the PWM6 output are selected by PWM6 control register 0 (PW6CON0).

External input can start / stop / clear the PWMn by setting the P6STM1 bit and P6STM0 bit of PWM6 control register 2 (PW6CON2). The control edge or level is selected by the P6TGE0 bit and P6TGE1 bit and the external input pin is selected by P6TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM6 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM7 signal delay1 (T_{PWD1}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW6P + 1}{P6CK\ (Hz)}$$

$$T_{PWD} = \frac{PW6D + 1}{P6CK\ (Hz)}$$

$$T_{PWD1} = \frac{PW7D + 1}{P6CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW7P + 1}{P6CK\ (Hz)}$$

PW6P:	PWM6 period registers (PW6PH, PW6PL) setting value (0001H to 0FFFFH)
PW6D:	PWM6 duty registers (PW6DH, PW6DL) setting value (0000H to 0FFFEH)
P6CK:	Clock frequency specified by PWM6 control registers
PW7P:	PWM7 period registers (PW7PH, PW7PL) setting value (0001H to 0FFFFH)
PW7D:	PWM7 duty registers (PW7DH, PW7DL) setting value (0000H to 0FFFEH)

After the P6RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-16 shows the operation timing of PWM6 and PWM7 on the condition of coupled mode with no dead-time specified (P67MD="1", P6DTMD="0") and one shot mode (P6MD="1").

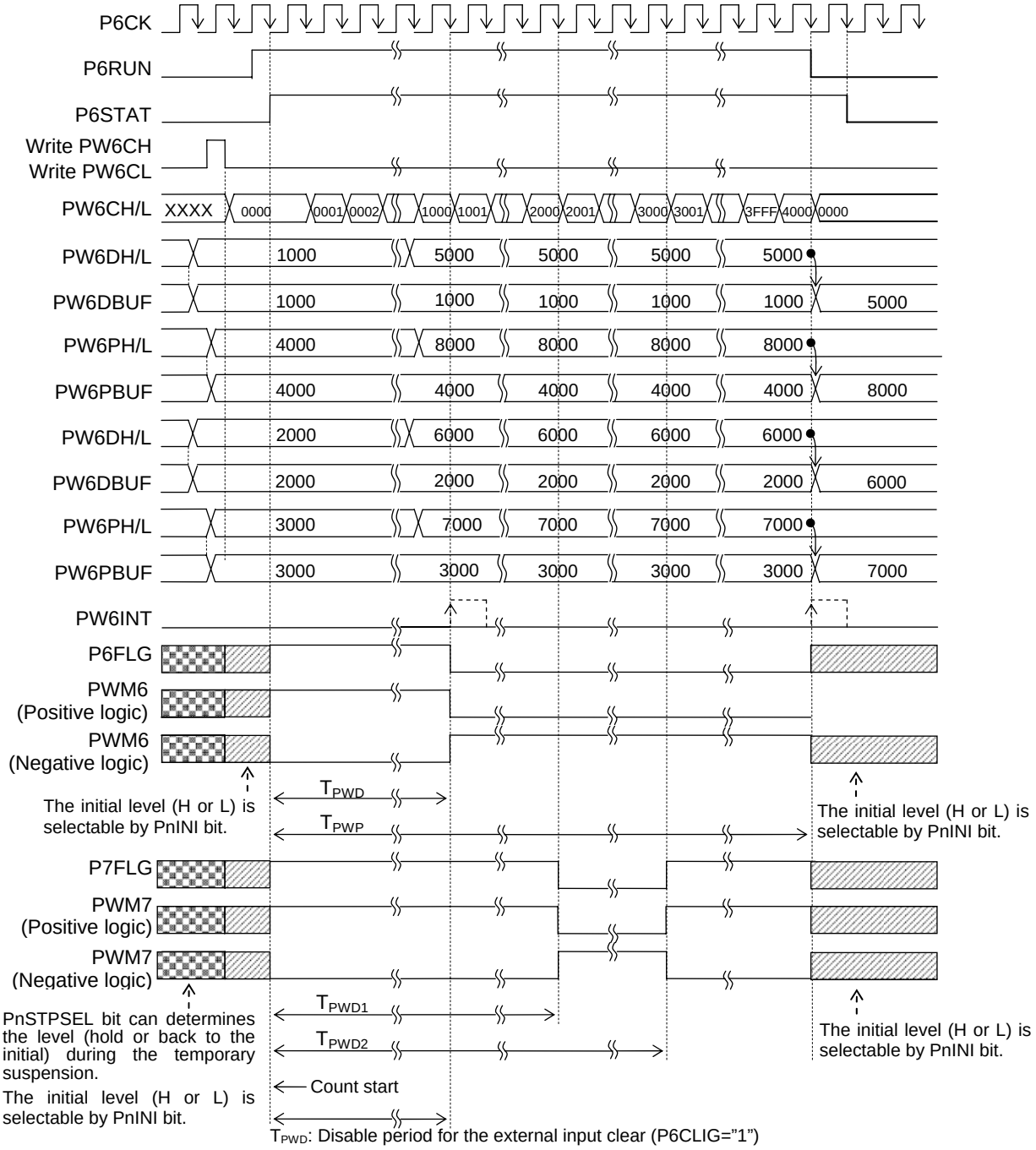


Figure 11-6 PWM6 and PWM7 Operating timing chart (P6MD="1", P67MD="1", P6DTMD="0")

11.3.13 PWM6 and PWM7, Coupled mode (with dead-time specified) / Repeat mode (P67MD="1", P6DTMD="1", P6MD="0")

The PWM6 counter registers (PW6CH, PW6CL) are set to an operating state (P6STAT is set to "1") on the first falling edge of the PWM clock (P6CK) that are selected by the PWM6 control register 0 (PW6CON0) and the PWM6 control register 6 (PW6CON6) when the P6RUN bit of PWM6 control register 1 (PW6CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

Setting P6DTMD bit to "1" enables the dead-time to generate the timing that de-activates both PWM6 and PWM7 at the same time. Specifiy the value of dead-time into PW7DH and PW7DL registers.

When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the [PWM6 duty buffer] + [dead-time] (PW6DBUF + PW7DBUF) coincide, the PWM6 flag (P6FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 duty buffer (PW7DBUF) coincide, the PWM7 flag (P7FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 duty buffer (PW6DBUF) coincide, the PWM7 flag (P7FLG) is set to "1" on the next falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 period buffer (PW7PBUF) coincide, the PWM6 flag (P6FLG) is set to "1" on the next falling edge of P6CK and the PWM6 counter registers is set to "0000H" and contines incremental counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the P6RUN bit is set to "0", the PWM6 counter registers (PW6CH, PW6CL) stop counting after counting once the falling of the PWM clock (P6CK). Confirm that PW6CH and PW6CL are stopped by checking that the P6STAT bit of the PWM6 control register 1 (PW6CON1) is "0". When the P6RUN bit is set to "1" again, PW6CH and PW6CL restarts incremental counting from the previous value on the falling edge of P6CK.

To initialize the PWM6 counter registers (PW6CH, PW6CL) to "0000H", perform write operation in either of PW6CH or PW6CL. At that time, P6FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM6 control register 0 (PW6CON0) and PWM6 control register 6 (PW0CON6).
PWM6 interrupt occurrence point and logic of the PWM6 output are selected by PWM6 control register 0 (PW6CON0). The logic of the PWM7 output are selected by PWM7 control register 0 (PW7CON0).

External input can start / stop / clear the PWMn by setting the P6STM1 bit and P6STM0 bit of PWM6 control register 2 (PW6CON2). The control edge or level is selected by the P6TGE0 bit and P6TGE1 bit and the external input pin is selected by P6TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM6 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM7 dead-time (T_{DTM}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW6P + 1}{P6CK\ (Hz)}$$

$$T_{PWD} = \frac{PW6D + PW7D + 2}{P6CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW6D + 1}{P6CK\ (Hz)}$$

$$T_{DTM} = \frac{PW7D + 1}{P6CK\ (Hz)}$$

PW6P: PWM6 period registers (PW6PH, PW6PL) setting value (0001H to 0FFFFH)
PW6D: PWM6 duty registers (PW6DH, PW6DL) setting value (0000H to 0FFFEH)
P6CK: Clock frequency specified by PWM6 control registers
PW7D: PWM7 duty registers (PW7DH, PW7DL) setting value (0000H to 0FFFEH)

After the P6RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-17 shows the operation timing of PWM6 and PWM7 on the condition of coupled mode with dead-time specified (P67MD="1", P6DTMD="1") and repeat mode (P6MD="0").

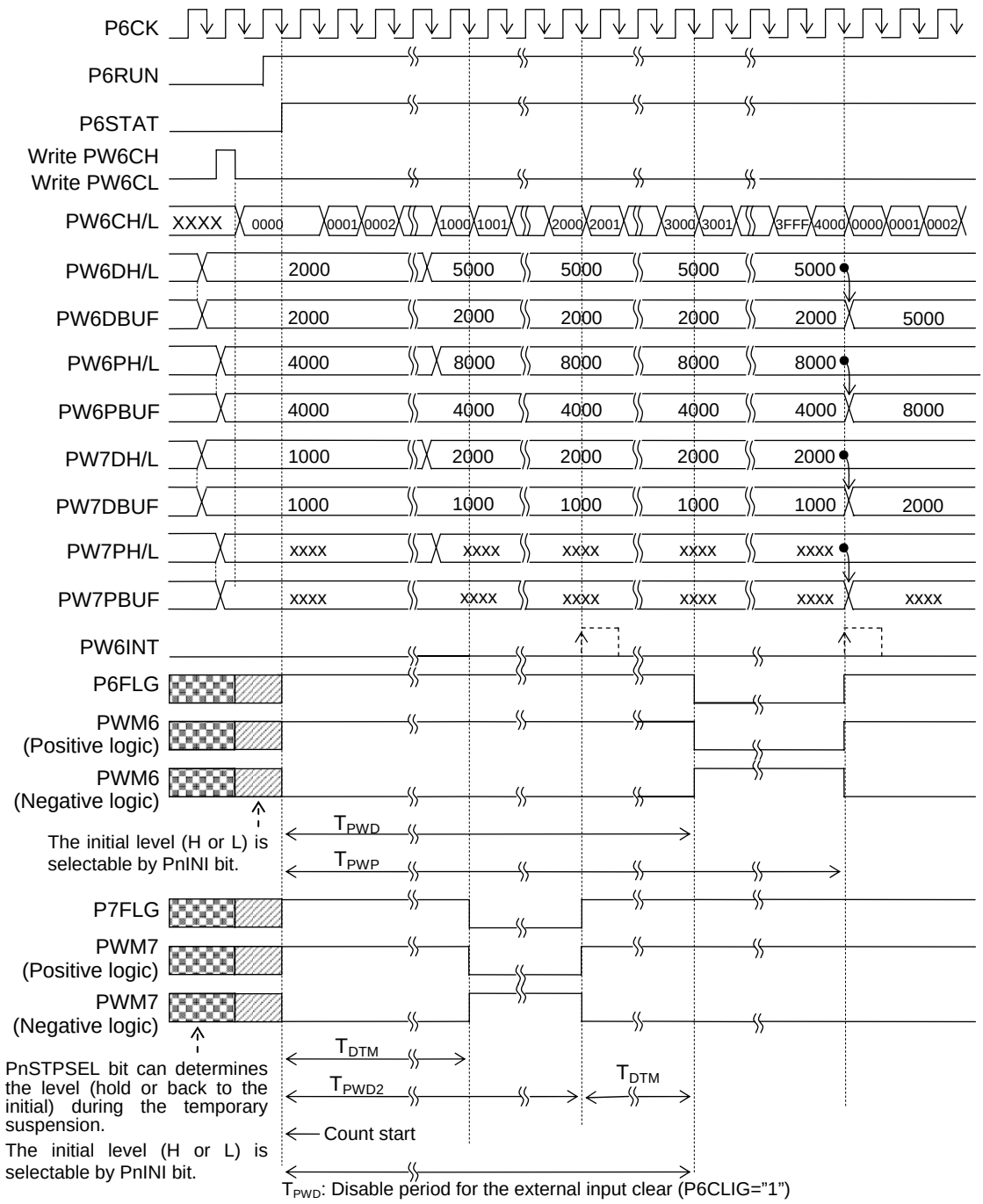


Figure 11-17 PWM6 and PWM7 Operating timing chart (P6MD="0", P67MD="1", P6DTMD="1")

Note:
PWM7 output is initially in a high-impedance output state before setting the port n control register 0 and 1 (PnCON0 and PnCON1). Fix the level with a pull-up or pull-down resister externally if needed.

11.3.14 PWM6 and PWM7, Coupled mode (with dead-time specified) / One shot mode (P67MD="1", P6DTMD="1", P6MD="1")

The PWM6 counter registers (PW6CH, PW6CL) are set to an operating state (P6STAT is set to "1") on the first falling edge of the PWM clock (P6CK) that are selected by the PWM6 control register 0 (PW6CON0) and the PWM6 control register 6 (PW6CON6) when the P6RUN bit of PWM6 control register 1 (PW6CON1) is set to "1" and starts incrementing the count value on the 2nd falling edge.

Setting P6DTMD bit to "1" enables the dead-time to generate the timing that de-activates both PWM6 and PWM7 at the same time. Specifiy the value of dead-time into PW7DH and PW7DL registers.

When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the [PWM6 duty buffer] + [dead-time] (PW6DBUF + PW7DBUF) coincide, the PWM6 flag (P6FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM7 duty buffer (PW7DBUF) coincide, the PWM7 flag (P7FLG) is set to "0" on the next timer clock falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 duty buffer (PW6DBUF) coincide, the PWM7 flag (P7FLG) is set to "1" on the next falling edge of P6CK.
When the count value of PWM6 counter registers (PW6CH, PW6CL) and the value of the PWM6 period buffer (PW7PBUF) coincide, the PWM6 flag (P6FLG) is set to "1" on the next falling edge of P6CK and the PWM6 counter registers is set to "0000H", stops incremental counting and the P6RUN bit gets cleared to "0". At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Setting the P6RUN bit to "1" restarts incremental counting the PWM counter registers.

When the P6RUN bit is set to "0", the PWM6 counter registers (PW6CH, PW6CL) stop counting after counting once the falling of the PWM clock (P6CK). Confirm that PW6CH and PW6CL are stopped by checking that the P6STAT bit of the PWM6 control register 1 (PW6CON1) is "0". When the P6RUN bit is set to "1" again, PW6CH and PW6CL restarts incremental counting from the previous value on the falling edge of P6CK.

To initialize the PWM6 counter registers (PW6CH, PW6CL) to "0000H", perform write operation in either of PW6CH or PW6CL. At that time, P6FLG is also set to "1". When data is written in the PWMn duty register (PWnDH, PWnDL) during count stop (PnRUN is in a "1" state), the data is transferred to the PWMn duty buffer (PWnDBUF) and when data is written in the PWMn period register (PWnPH, PWnPL), the data is transferred to the PWMn period buffer (PWnPBUF).

The PWM clock is selected by PWM6 control register 0 (PW6CON0) and PWM6 control register 6 (PW0CON6).
PWM6 interrupt occurrence point and logic of the PWM6 output are selected by PWM6 control register 0 (PW6CON0). The logic of the PWM7 output are selected by PWM7 control register 0 (PW7CON0).

External input can start / stop / clear the PWMn by setting the P6STM1 bit and P6STM0 bit of PWM6 control register 2 (PW6CON2). The control edge or level is selected by the P6TGE0 bit and P6TGE1 bit and the external input pin is selected by P6TGSEL bit. For more details about transfer timings between the PWMn duty registers and the duty buffer or PWMn period registers and the period buffer, see 11.3.15 "PWM6/PWM7 start/stop/clear operation by the external control" with notice for some operational restrictions.

The period of the PWM6 signal (T_{PWP}), the first half duration (T_{PWD}) of the duty, the duration of the PWM7 dead-time (T_{DTM}) and the delay2(T_{PWD2}), are expressed by the following equations.

$$T_{PWP} = \frac{PW6P + 1}{P6CK\ (Hz)}$$

$$T_{PWD} = \frac{PW6D + PW7D + 2}{P6CK\ (Hz)}$$

$$T_{PWD2} = \frac{PW6D + 1}{P6CK\ (Hz)}$$

$$T_{DTM} = \frac{PW7D + 1}{P6CK\ (Hz)}$$

PW6P: PWM6 period registers (PW6PH, PW6PL) setting value (0001H to 0FFFFH)
PW6D: PWM6 duty registers (PW6DH, PW6DL) setting value (0000H to 0FFFEH)
P6CK: Clock frequency specified by PWM6 control registers
PW7D: PWM7 duty registers (PW7DH, PW7DL) setting value (0000H to 0FFFEH)

After the P6RUN bit is set to "1", counting starts in synchronization with the PWM clock. This causes an error of up to 1 clock pulse to the time the first PWM interrupt is issued. The PWM interrupt period from the second time is fixed.
Figure 11-18 shows the operation timing of PWM6 and PWM7 on the condition of coupled mode with dead-time specified (P67MD="1", P6DTMD="1") and one shot mode (P6MD="1").

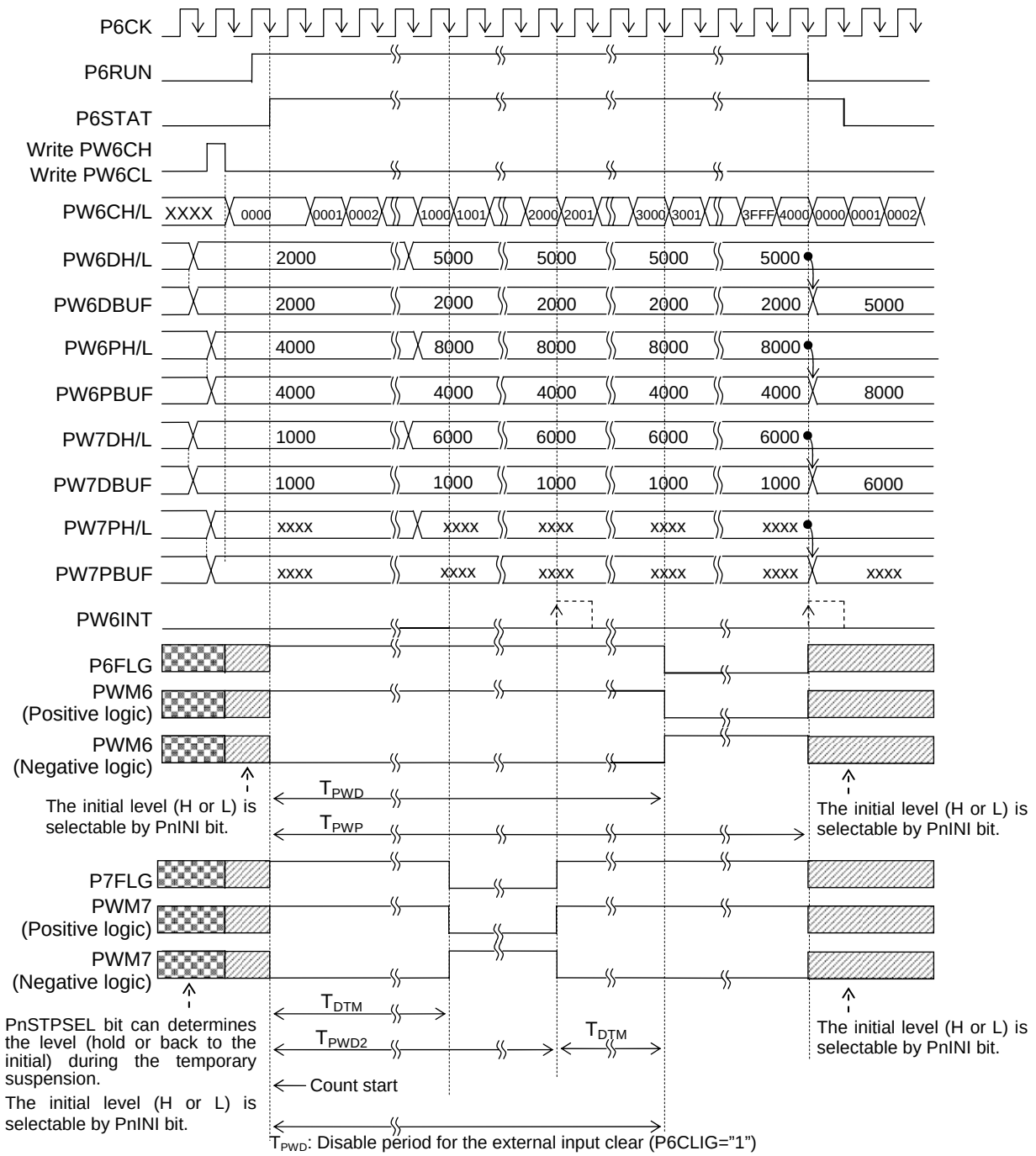
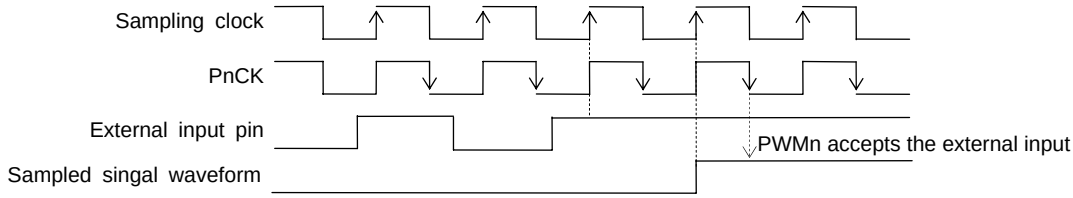


Figure 11-18 PWM6 and PWM7 Operating timing chart (P6MD="1", P67MD="1", P6DTMD="1")

Note:
PWM7 output is initially in a high-impedance output state before setting the port n control register 0 and 1 (PnCON0 and PnCON1). Fix the level with a pull-up or pull-down resister externally if needed.

11.3.15 PWM6/PWM7 start/stop/clear operation by the external control

The PWM counter registers (PWnCH, PWnCL) can be enabled to start, stop and clear with external triggering inputs, by setting PnSTM1 bit, PnSTM0 bit and PnTGSEL bit of PWMn control register 2 (PWnCON2). The external input is sampled with a clock to eliminate one clock or less pulse of noise. The sampling clock is determined by PnCS1 and PnCS0 bit. When OSCLK is selected the OSCLK (approx. 125ns) is used as the sampling clock and in the other cases LSCLK (approx. 30.5us) is used as the sampling clock.



11.3.15.1 Software Start Mode

With the setting of PnSTM1="0" and PnSTM0="0", the PWM counter operates being controlled by the PnRUN bit only. The operation timing is similar to the ones shown in 11.3.9 to 11.3.14.

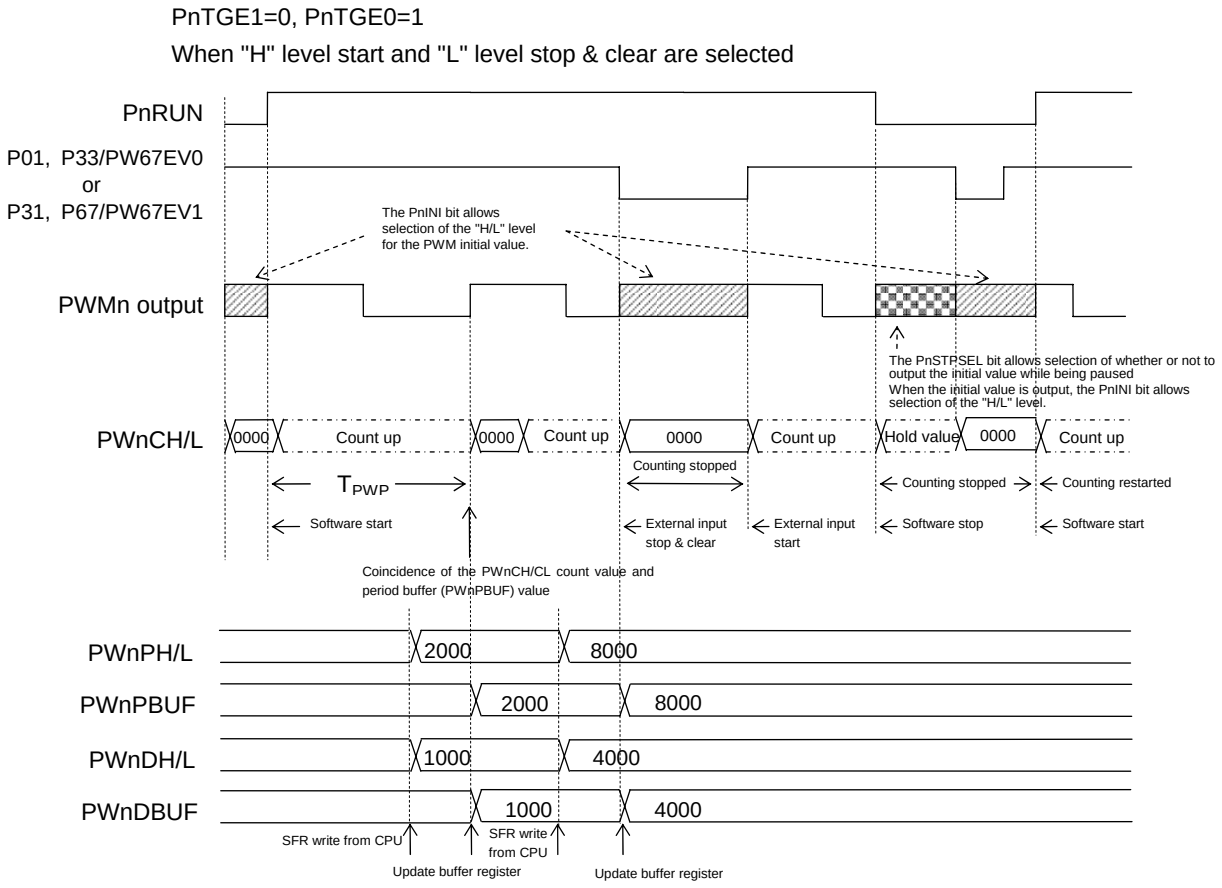
11.3.15.2 Software Start Mode or External Start Mode

With the setting of PnSTM1="0" and PnSTM0="1", the PWM counter operates being controlled by the external input (P01 or P33/PW67EV0, P31 or P63/PW67EV1) that is selected by the PnRUN and PnTGSEL bits.
When the selected external input gets an external input specified by PnTGE1 and PnTGE0 (PWnCON2 register), the PWM counter is started, stopped, or cleared. When the selected external input is fixed at the count start level, the counter operates in the same way as the software start.
However, when the selected external input is at the count stop level on the software start, the counter does not start, and it starts counting when the selected external input becomes the count start level.

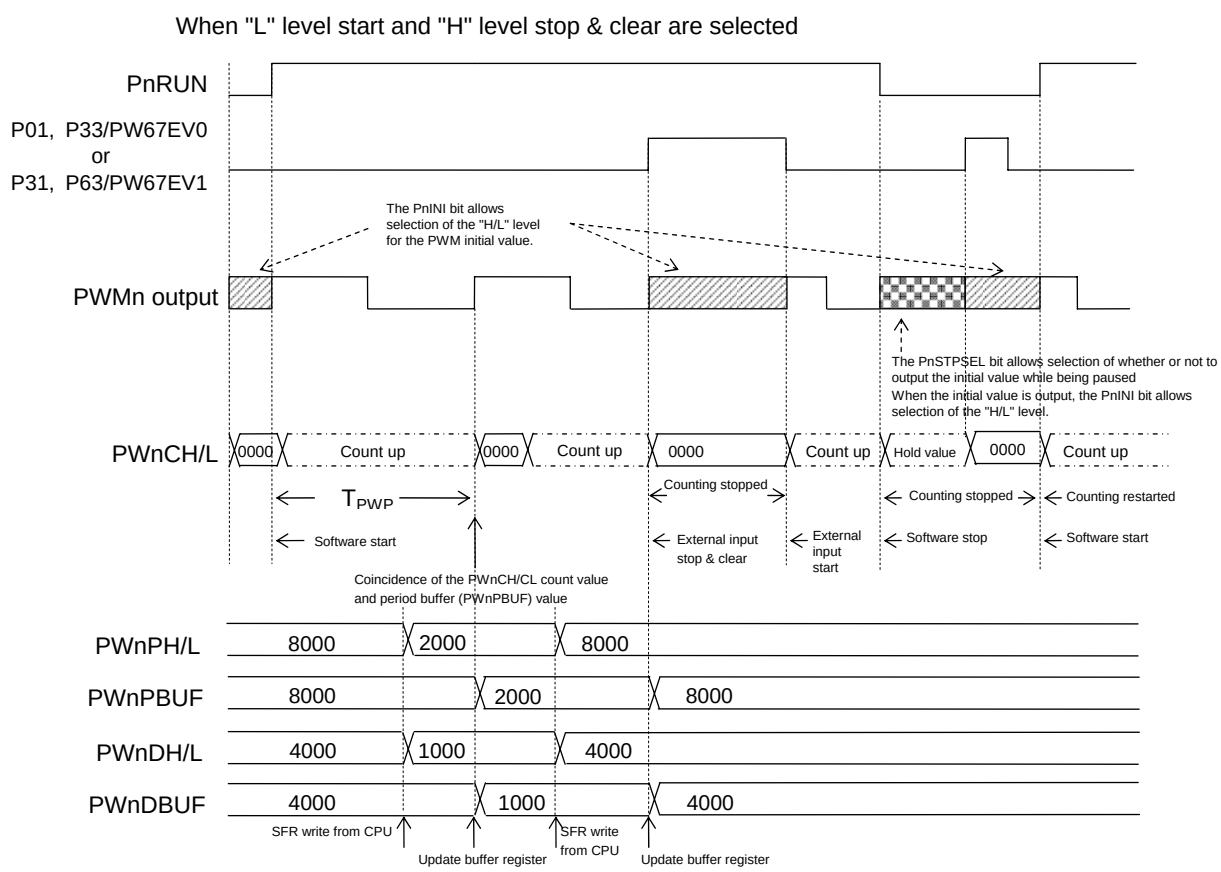
PnTGE1	PnTGE0	Count start edge	Count stop edge	Count start level	Count stop level
0	1	Rising edge	Falling edge	“H” level	“L” level
1	0	Falling edge	Rising edge	“L” level	“H” level

Note:
When stopping the counter by the external input, the counter always gets cleared.

Figure 11-19 shows the operation timing.



(a)Operation Timing Diagram with Software Start or External Input Start (PnTGE1=0, PnTGE0=1)



(b)Operation Timing Diagram with Software Start or External Input Start (PnTGE1=1, PnTGE0=0)

Figure 11-19 Operation Timing Diagram with Software Start or External Input Start (PnSTM1="0", PnSTM0="1")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P6CK/P7CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

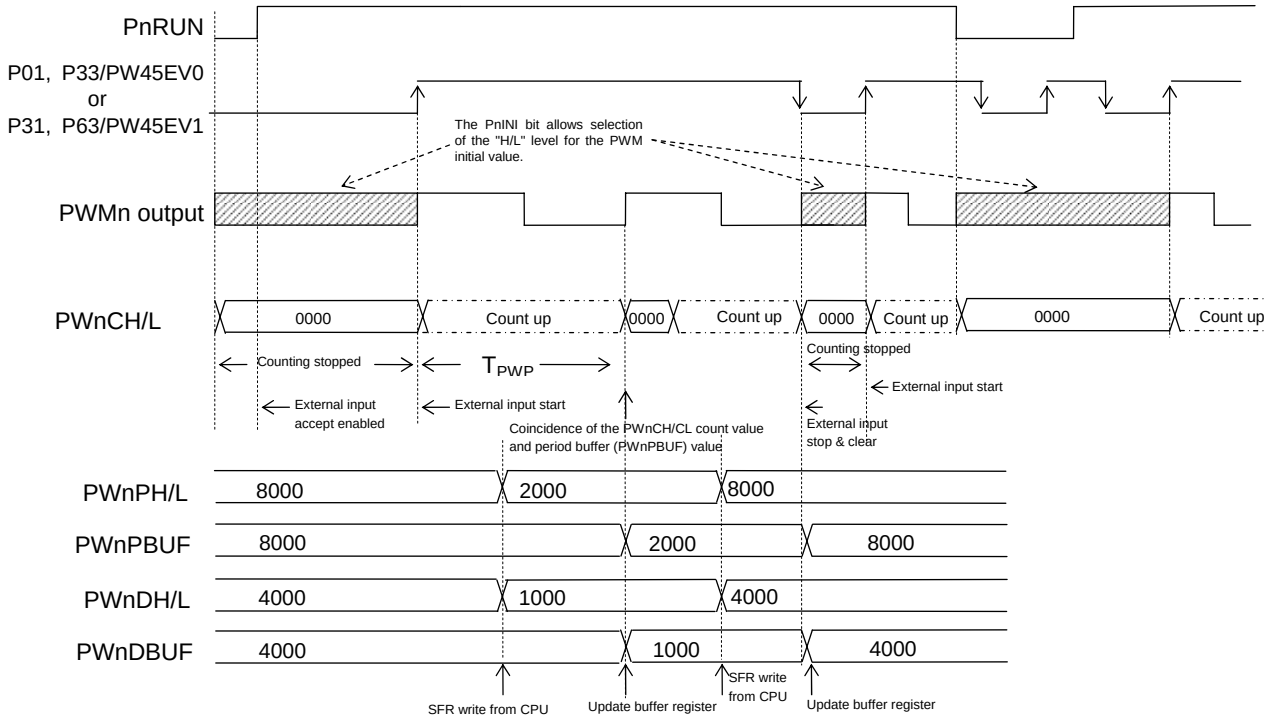
③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

11.3.15.3 External Input Start Mode

With the setting of PnSTM1="1" and PnSTM0="0" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the edge of the external input that is selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2).
Note that the PnRUN bit is set to "1" in advance. If the PnRUN bit is "0", PWM will not operates even when the edge input occurs on the selected external input.
Figure 11-20 shows the operation timing.

PnTGE1=0, PnTGE0=1

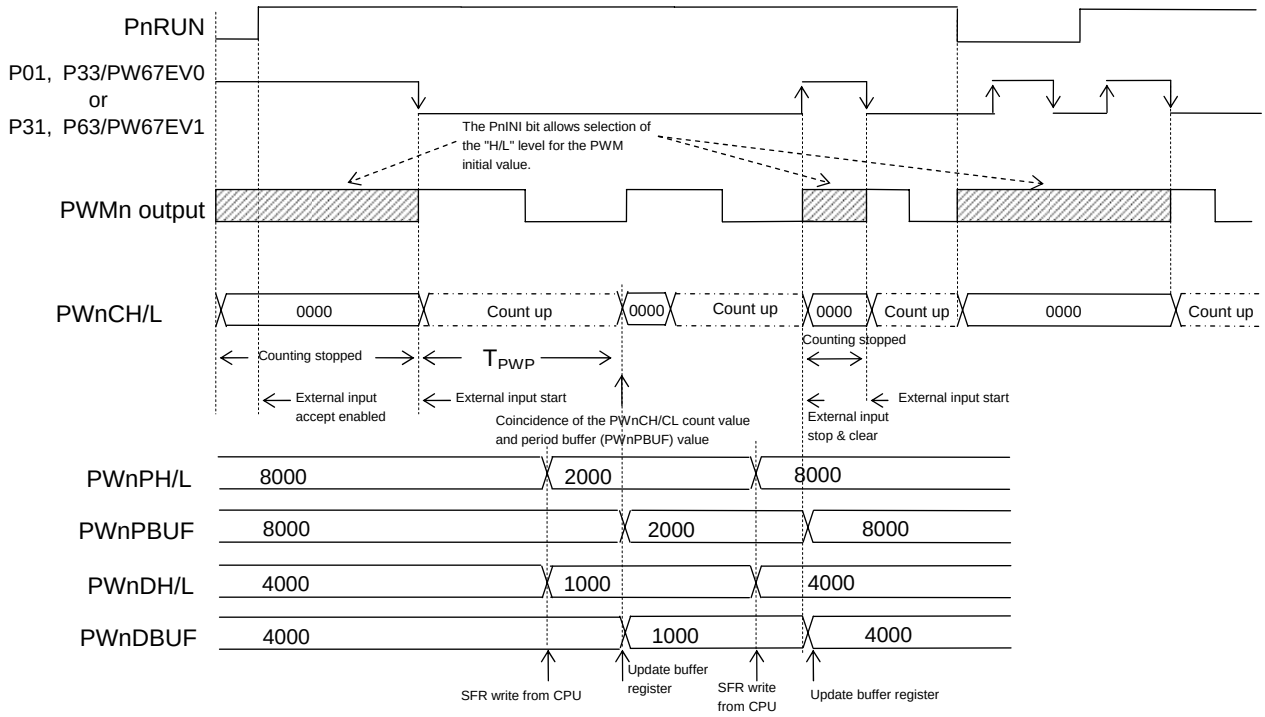
When rising-edge start and falling-edge stop & clear are selected



(a)Operation Timing Diagram with External Input Start

PnTGE1=1, PnTGE0=0

When falling-edge start and rising-edge stop & clear are selected



(b)Operation Timing Diagram with External Input Start

Figure 11-20 Operation Timing Diagram with External Input Start (PnSTM1="1", PnSTM0="0")

When cleared by the external input, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P6CK/P7CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

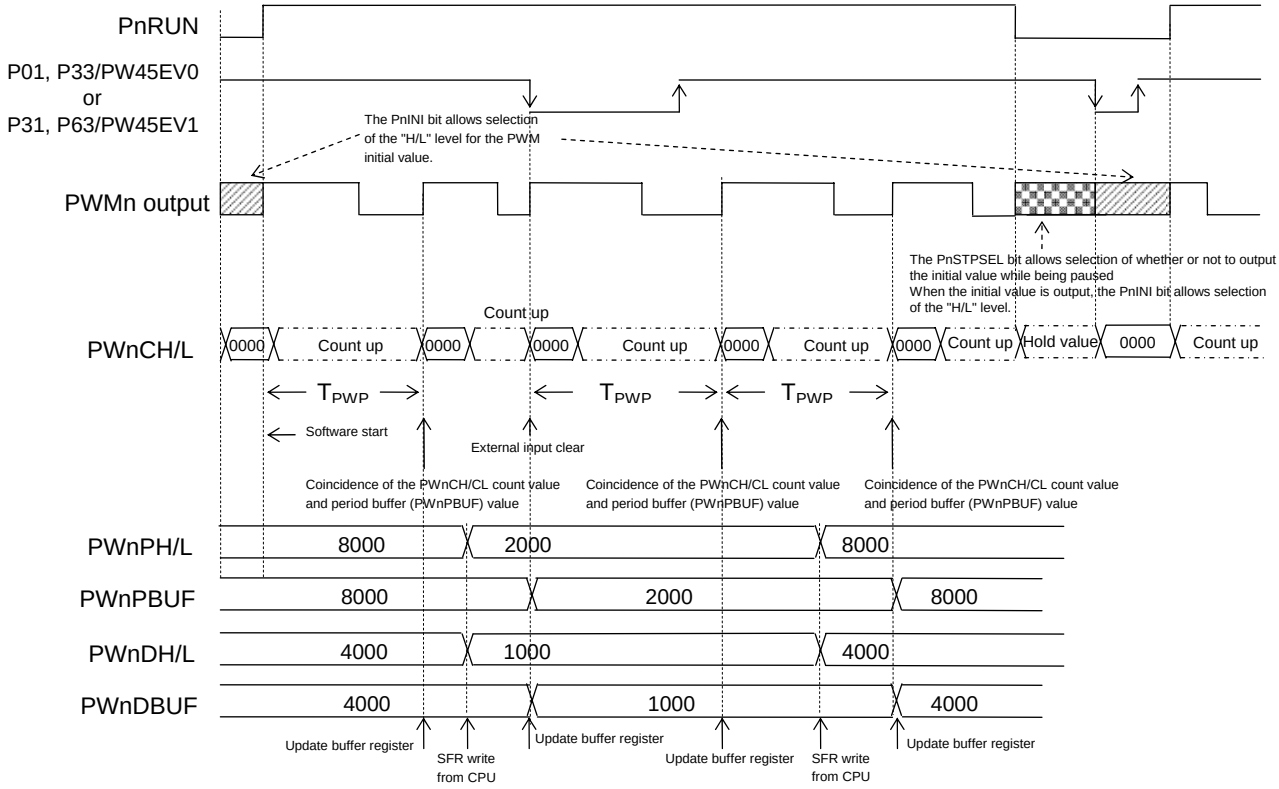
② A pulse shorter than one internal PWM1 clock may not be accepted as the external input.

③ The PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) should not be written to after the PWM count is stopped by the external input during PWM operation (PnRUN="1").

11.3.15.4 Software Start or External Input Clear Mode

With the setting of PnSTM1="1" and PnSTM0="1" on the PWMn control register 2 (PWnCON2), the PWM counter operates being controlled by the PnRUN bit.
When there is no edge input on the external input selected by the PnTGSEL bit of the PWMn control register 2 (PWnCON2), the counter operates in the same way as the software start. When the selected external input gets an edge input specified by PnTGE1 and PnTGE0, the PWM counter is cleared. The PnCLIG bit of the PWMn control register 0 (PWnCON0) allows enable/disable of the external clear input at the "H" level of the PWMn output flag (PnFLG).
Figure 11-21 shows the operation timing.

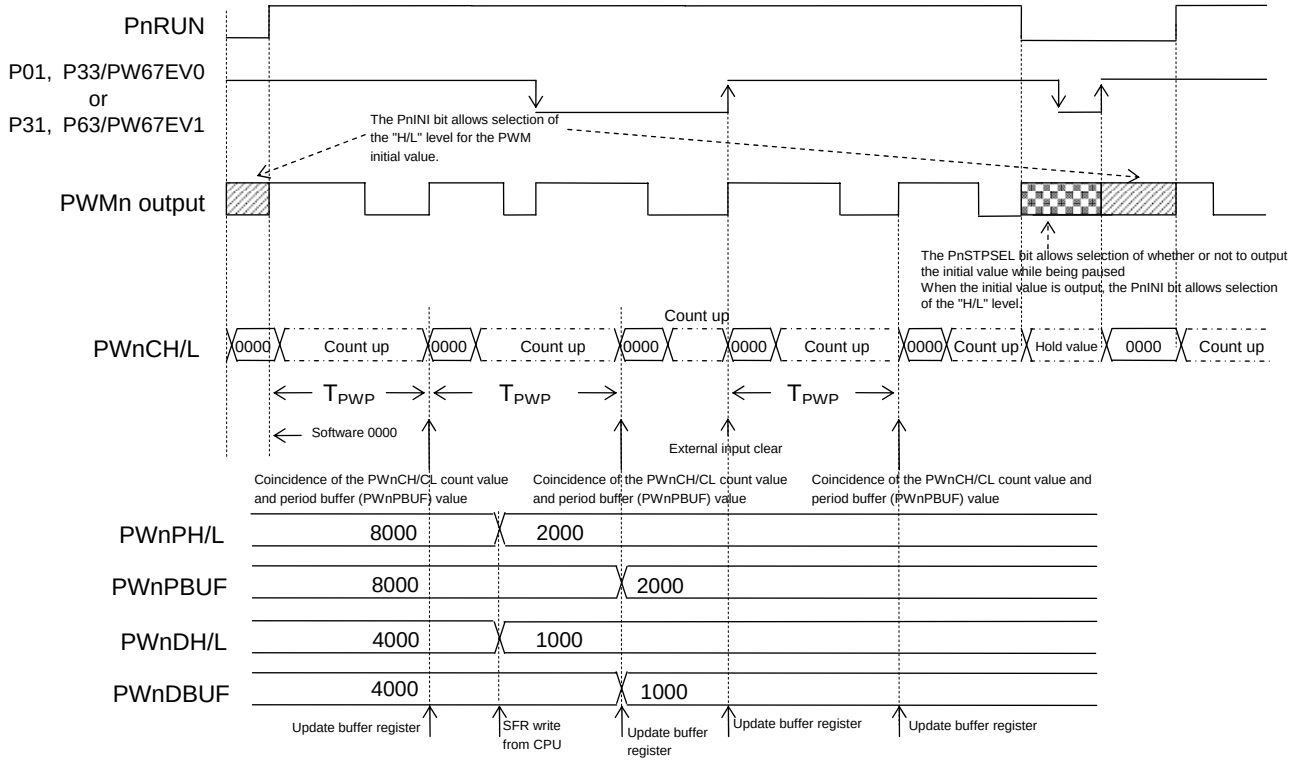
PnTGE1=0, PnTGE0=1
When falling-edge clear is selected



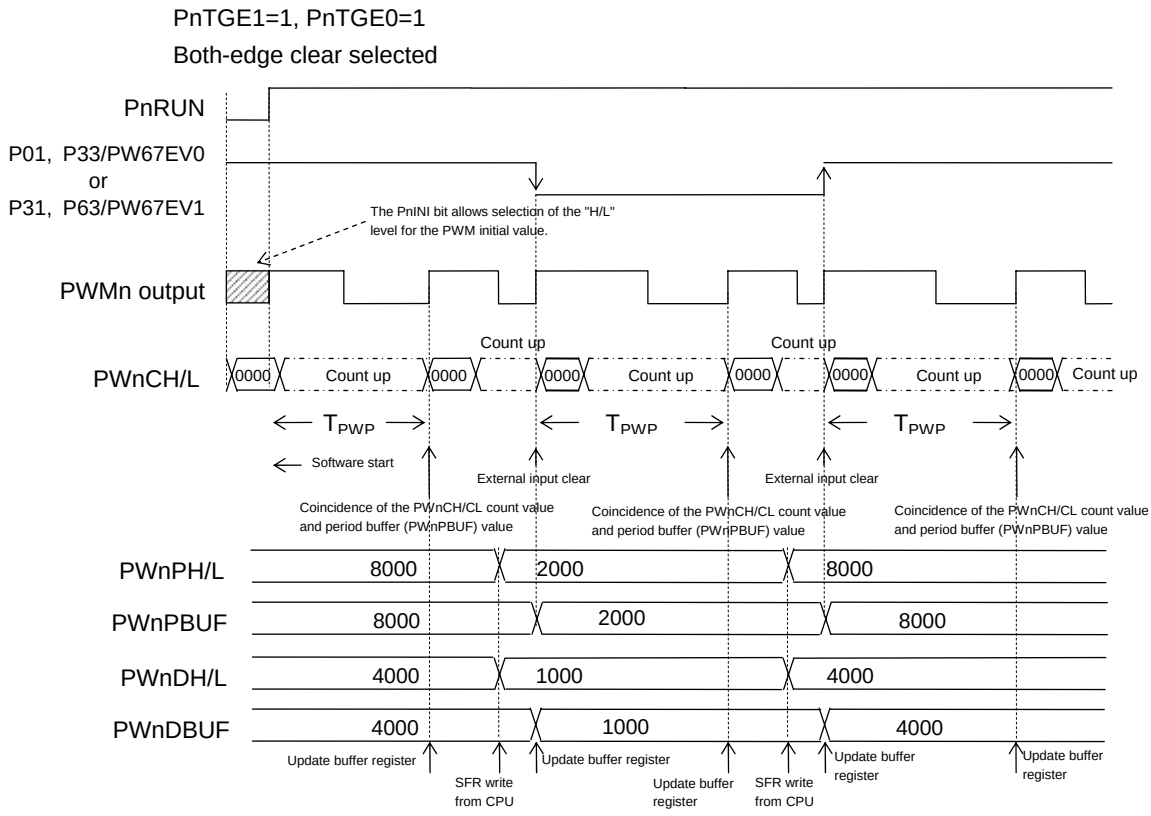
(a) Operation Timing Diagram with Software Start and External Input Clear

PnTGE1=1, PnTGE0=0

When rising-edge clear is selected



(b) Operation Timing Diagram with Software Start and External Input Clear



(c) Operation Timing Diagram with Software Start and External Input Clear

Figure 11-21 Operation Timing Diagram with Software Start and External Input Clear

For clear control by the external input, the values of the PWMn duty registers (PWnDH, PWnDL) and PWMn period registers (PWnPH, PWnPL) are transferred to the PWMn duty buffer (PWnDBUF) and PWMn period buffer (PWnPBUF) respectively at the timing of the external input pins and edges specified by PnTGSEL, PnTGE1, and PnTGE0.

Note that there are the following restrictions.

① When PWMnPH/L or PWMnDH/L is changed during PWM operation to use the software start or external input start, the system clock/PWM clock must be one of the following combinations.

PWM clock P6CK/P7CK	System clock SYSCLK
LSCLK	LSCLK
HTBCLK	HSCLK

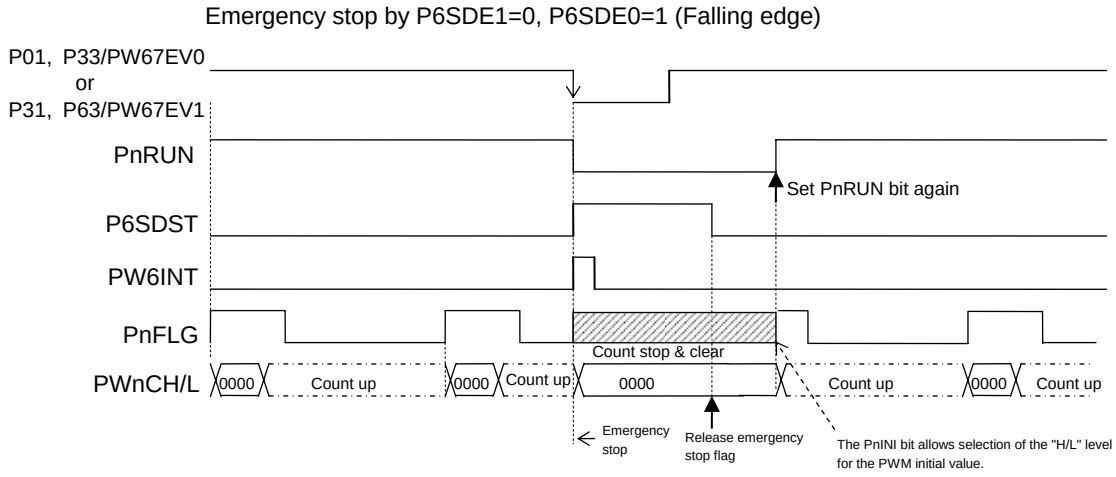
② When the external input clear control is done at a timing when PWMnPH/L or PWMnDH/L is changed while the PWM count is being paused, transfer to the PWMn duty buffer (PWnDBUF) or PWMn period buffer (PWnPBUF) may delay for one PWM clock.

11.3.16 Emergency Stop Operation

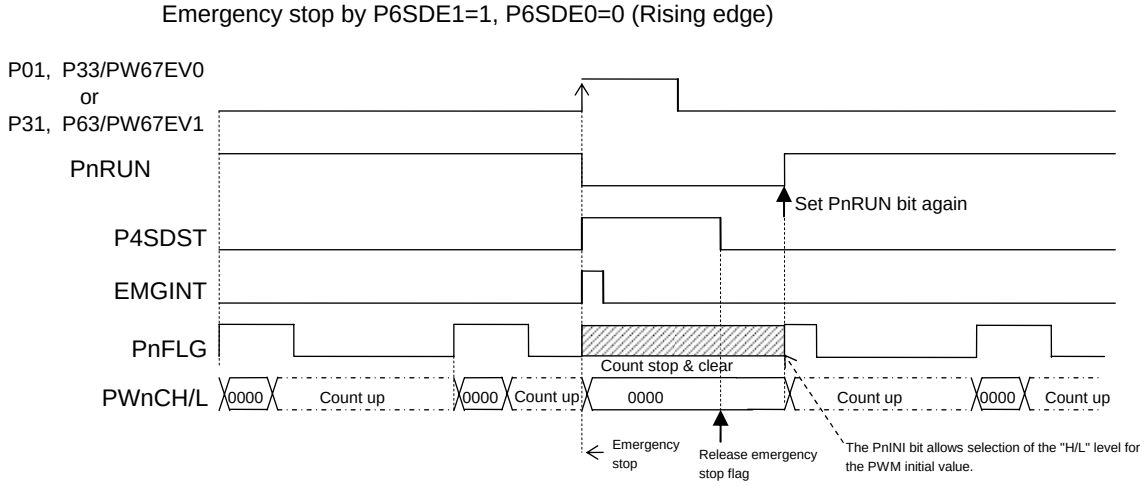
Setting the P6SDE1 and P6SDE0 bits of the PWM6 control register 3 (PW6CON3) enables the emergency stop function with the external input that is selected by P6TGSEL. Note that the emergency stop function is valid only in the cooperation mode (P67MD="1").

When the external input that is selected by the P6TGSEL bit gets an edge input specified by P6SDE1 an P6SDE0, the emergency stop flag (P6SDST) is set to "1", an emergency stop interrupt (PW6INT) is generated, and the PWM counter is stopped/cleared. Because the PWM flag output (PnFLG) is cleared, the PWM6 and PWM7 outputs are turned off simultaneously.

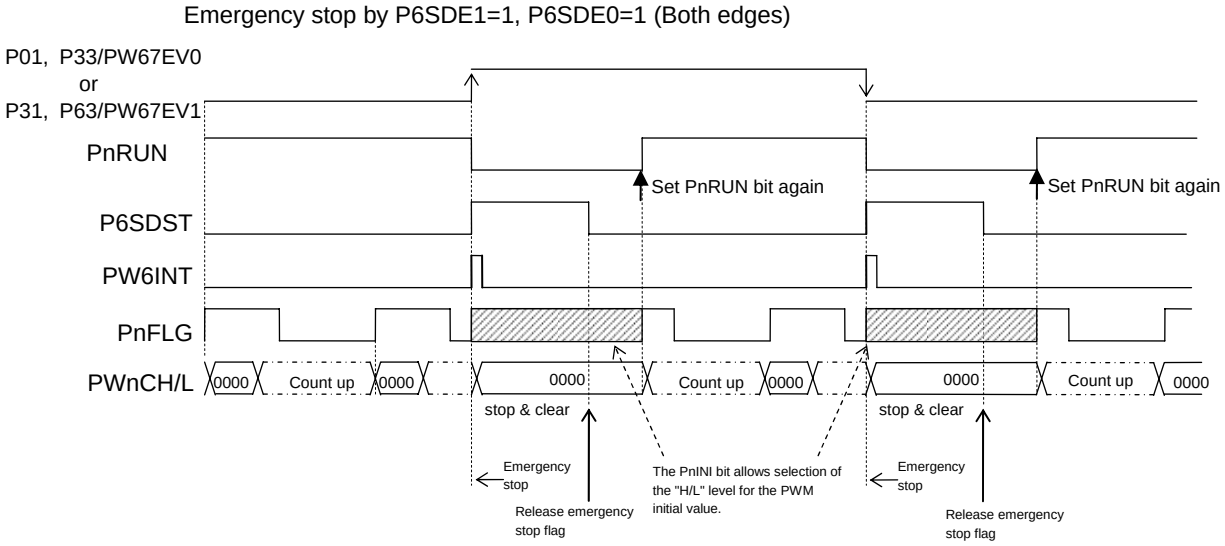
To release the emergency stop flag, write "1" to P6SDST of the PWM6 control register 3 (PW6CON3).
Figure 11-22 shows the operation timing.



(a)Timing with Falling-edge operation



(b)Timing with Rising-edge operation



(c)Timing with Both-edge operation

Figure 11-22 Operation Timing Diagram at Emergency Stop

Chapter 12 Synchronous Serial Port

12 Synchronous Serial Port (SSIO)

12.1 General Description

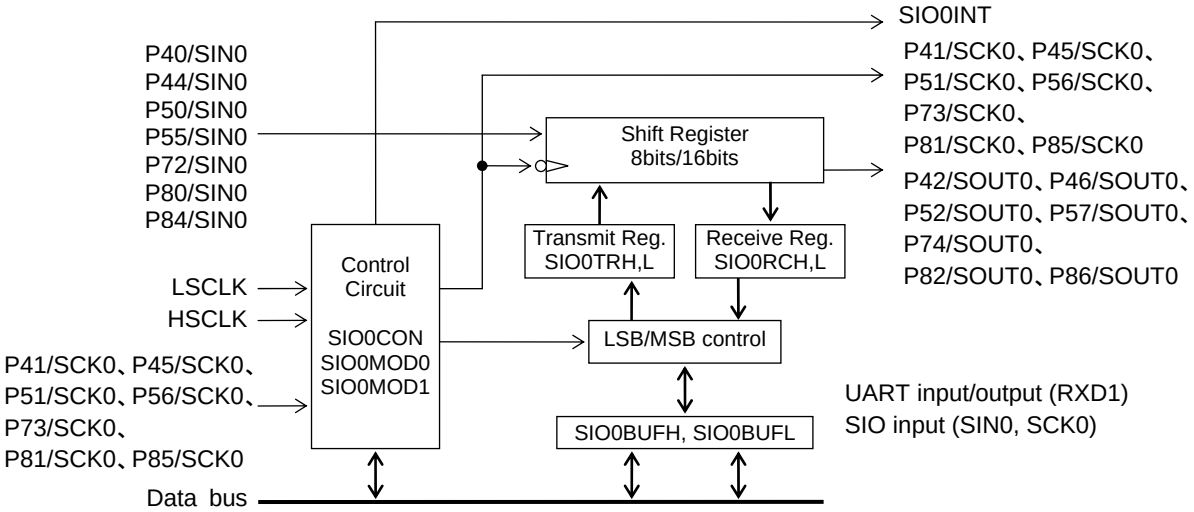
This LSI includes one channel of 8/16-bit synchronous serial ports (SSIO). It can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
When the synchronous serial port is used, the tertiary functions of Port must be set. For the tertiary function setting of Port, see Chapter 19, "Port 4", Chapter 20, "Port 5", Chapter 22, "Port 7" and Chapter 23, "Port 8".
The synchronous serial ports (SSIO) is enable to work when DSIO0 bit of BLKCON2 register is “0”. If the DSIO0 bit is “1”, all functions of the synchronous serial ports (SSIO) are in a reset status. For more details about the BLKCON2 register, see Chapter 4, “MCU Control Function”.

12.1.1 Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable fro the data length

12.1.2 Configuration

Figure 12-1 shows the configuration of the synchronous serial port.



SIO0BUFL : Serial port transmit/receive buffer L
SIO0BUFH : Serial port transmit/receive buffer H
SIO0CON : Serial port control register
SIO0MOD0 : Serial port mode register 0
SIO0MOD1 : Serial port mode register 1

Figure 12-1 Configuration of Synchronous Serial Port

12.1.3 List of Pins

Pin name	I/O	Function
P40/SIN0	I	Received data input. Used for the tertiary function of the P40 pins.
P41/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P41 pins
P42/SOUT0	O	Transmitted data output. Used for the tertiary function of the P42 pins
P44/SIN0	I	Received data input. Used for the tertiary function of the P44 pins.
P45/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P45 pins
P46/SOUT0	O	Transmitted data output. Used for the tertiary function of the P46 pins
P50/SIN0	I	Received data input. Used for the tertiary function of the P50 pins.
P51/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P51 pins
P52/SOUT0	O	Transmitted data output. Used for the tertiary function of the P52 pins
P55/SIN0	I	Received data input. Used for the tertiary function of the P55 pins.
P56/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P56 pins
P57/SOUT0	O	Transmitted data output. Used for the tertiary function of the P57 pins
P72/SIN0	I	Received data input. Used for the tertiary function of the P72 pins.
P73/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P73 pins
P74/SOUT0	O	Transmitted data output. Used for the tertiary function of the P74 pins
P80/SIN0	I	Received data input. Used for the tertiary function of the P80 pins.
P81/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P81 pins
P82/SOUT0	O	Transmitted data output. Used for the tertiary function of the P82 pins
P84/SIN0	I	Received data input. Used for the tertiary function of the P84 pins.
P85/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P85 pins
P86/SOUT0	O	Transmitted data output. Used for the tertiary function of the P86 pins

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F700H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F701H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F702H	Serial port 0 control register	SIO0CON	−	R/W	8	00H
0F704H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F705H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H

12.2.2 Serial Port 0 Transmit/Receive Buffers (SIO0BUFL and SIO0BUFH)

Address: 0F700H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F701H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUFL and SIO0BUFH are special function registers (SFRs) to write transmitted data and to read received data of the synchronous serial port 0.
When data is written in SIO0BUFL and SIO0BUFH, the data is written in the transmit registers (SIO0TRL and SIO0TRH). When data is read from SIO0BUFL and SIO0BUFH, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

12.2.3 Serial Port 0 Control Register (SIO0CON)

Address: 0F702H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0CON	—	—	—	—	—	—	—	S0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port 0.

[Description of Bits]

- **S0EN** (bit 0)
  The S0EN bit is used to specify start of synchronous serial communication. Writing a "1" to S0EN starts 8-/16-bit data communication. The S0EN bit is set to "0" automatically when 8-/16-bit data communication is terminated.
  The S0EN bit is set to "0" at a system reset.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

12.2.4 Serial Port 0 Mode Register 0 (SIO0MOD0)

Address: 0F704H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	—	—	—	—	S0LG	S0MD1	S0MD0	S0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD0 is a special function register (SFR) to set mode of the synchronous serial port 0.

[Description of Bits]

- **S0LG** (bit 3)
  S0LG is the bit that specifies the transmit/receive buffer bit length. Either 8-bit length or 16-bit length can be selected.
  The S0LG bit is set to "0" at a system reset.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

- **S0MD1 and S0MD0** (bits 2 and 1)
  The S0MD1 and S0MD0 bits are used to select the transmit/receive mode of the synchronous serial port 0. The Receive mode, Transmit mode, or Transmit/Receive mode is selectable.

S0MD1	**S0MD0**	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S0DIR** (bit 0)
  S0DIR is the bit for selecting LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

[Note]
• Do not change any of the SIO0MOD0 register settings during transmission/reception.
• When the synchronous serial port is used, the tertiary functions of Port 4, Port5, Port 7 or Port 8 must be specified. For the tertiary functions of Ports, see the each chapter in this manual.

12.2.5 Serial Port 0 Mode Register 1 (SIO0MOD1)

Address: 0F705H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD1	—	—	—	S0CKT	S0CK3	S0CK2	S0CK1	S0CK0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD1 is a special function register (SFR) to set mode of the synchronous serial port 0.

[Description of Bits]

- **S0CKT** (bit 4)
  The S0CKT bit is used to select the phase of the transfer clock output.

S0CKT	Description
0	Clock type 0: Output at the “H” level by default (initial value).
1	Clock type 1: Output at the “L” level by default.

- **S0CK3 to S0CK0** (bits 3 to 0)
  The S0CK3 to S0CK0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK3	S0CK2	S0CK1	S0CK0	Description
0	0	0	0	1/1 LSCLK (Initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	Do not use
0	1	1	1	Do not use
1	0	0	0	External clock 0 (P41/SCK0)
1	0	0	1	External clock 1 (P45/SCK0)
1	0	1	0	Do not use
1	0	1	1	External clock 2 (P56/SCK0)
1	1	0	0	External clock 3 (P73/SCK0)
1	1	0	1	Do not use
1	1	1	0	External clock 4 (P81/SCK0)
1	1	1	1	External clock 5 (P85/SCK0)

[Note]
- Do not change any of the SIO0MOD1 register settings during transmission/reception.
- Specify the transfer clock of the synchronous serial port 4.2MHz or slower.

12.3 Description of Operation

12.3.1 Transmit Operation

When “1” is written to the S0MD1 bit and "0" is written to the S0MD0 bit of the serial port mode register (SIO0MOD0), this LSI is set to the transmit mode.
When transmitted data is written to the serial port transmit/receive buffer (SIO0BUFL, "H") and the S0EN bit of the serial port control register (SIO0CON) is set to “1”, transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the SnEN bit is set to “0”.
The transmitted data is output from the Port's tertiary functions (P42/SOUT0, P46/SOUT0, P52/SOUT0, P57/SOUT0, P74/SOUT0, P82/SOUT0, P86/SOUT0).
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first/LSB first.
The transmitted data output pin (P42/SOUT0, P46/SOUT0, P52/SOUT0, P57/SOUT0, P74/SOUT0, P82/SOUT0, P86/SOUT0) and the transfer clock input/output pin (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) need to be set to the tertiary function for the each Port.
The transmission operation waveforms of the synchronous serial port (8-bit length, LSB first) are shown in Figures 12-2 and 12-3.

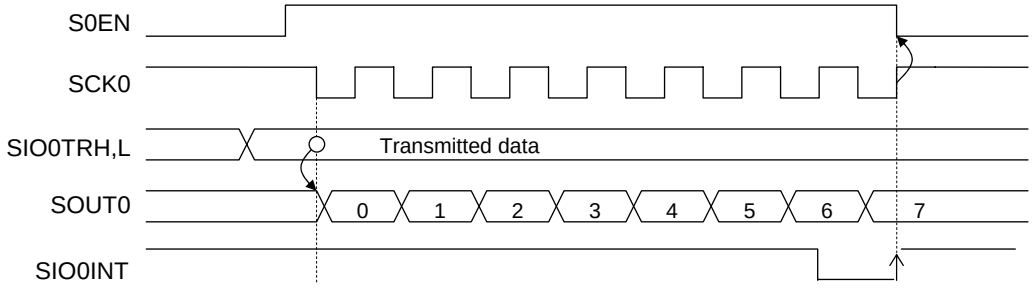


Figure 12-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit length, LSB first)

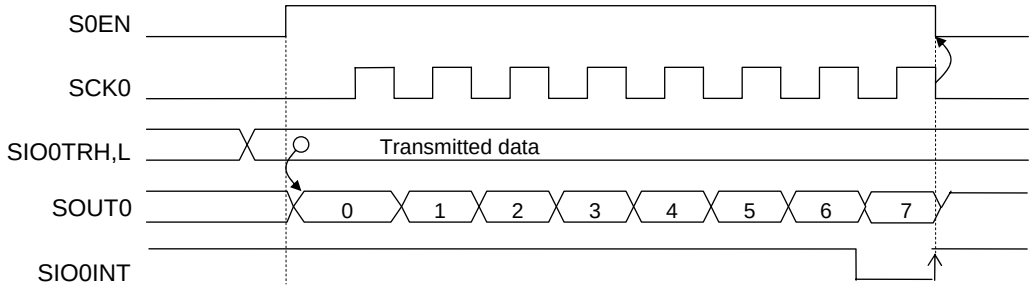


Figure 12-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit length, LSB first)

12.3.2 Receive Operation

When "0" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial port mode register (SIO0MOD0), this LSI is set to a receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the SnEN bit is set to "0".
The received data is input from the tertiary function pins (P40/SIN0, P44/SIN0, P50/SIN0, P55/SIN0, P72/SIN0, P80/SIN0, P84/SIN0) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first/LSB first.
The received data input pin (P40/SIN0, P44/SIN0, P50/SIN0, P55/SIN0, P72/SIN0, P80/SIN0, P84/SIN0) and the transfer clock input/output pin (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) need to be set to the tertiary function for the each Port.
The receive operation waveforms of the synchronous serial port (8-bit length, MSB first) are shown in Figures 12-4 and P12-5.

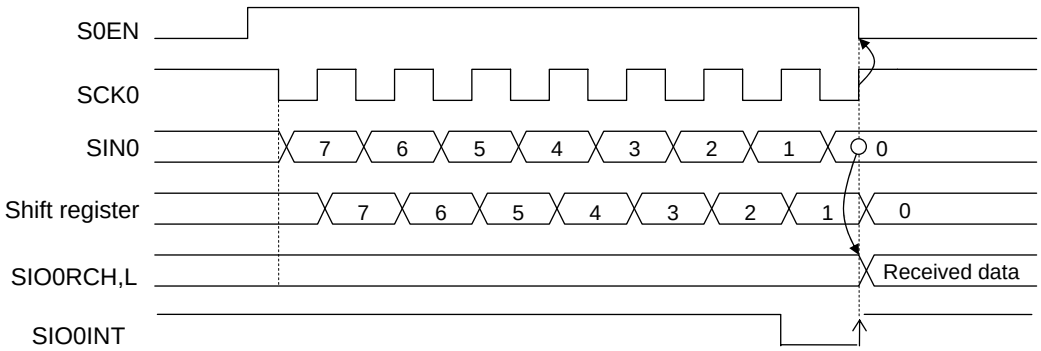


Figure 12-4 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit length, MSB first)

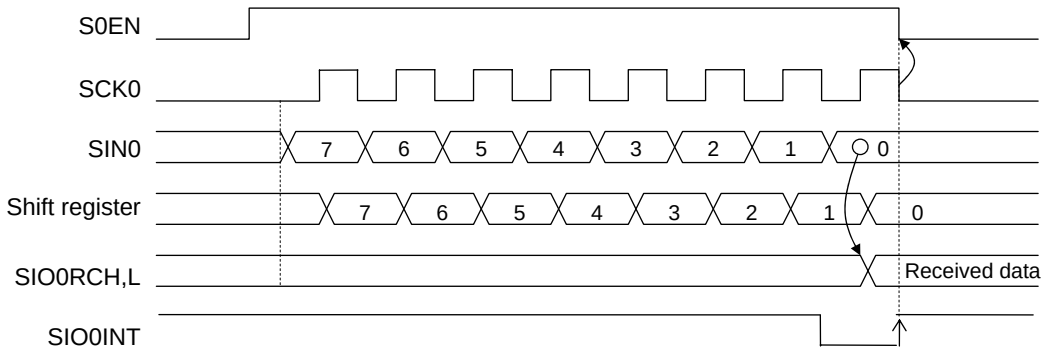


Figure 12-5 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit length, MSB first)

[Note]
When the SOUT0 pin is set to the tertiary function output in receive mode, a "H" level is output from the SOUT0 pin.

12.3.3 Transmit/Receive Operation

When “1” is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial port mode register (SIO0MOD0), this LSI is set to the transmit/receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to “1”, transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to “0”.
The received data is input from the tertiary function pins (P40/SIN0, P44/SIN0, P50/SIN0, P55/SIN0, P72/SIN0, P80/SIN0, P84/SIN0) of GPIO, and the transmitted data is output from the tertiary function pins (P42/SOUT0, P46/SOUT0, P52/SOUT0, P57/SOUT0, P74/SOUT0, P82/SOUT0, P86/SOUT0) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first/LSB first.
The received data input pin (P40/SIN0, P44/SIN0, P50/SIN0, P55/SIN0, P72/SIN0, P80/SIN0, P84/SIN0), the transmitted data output pin (P42/SOUT0, P46/SOUT0, P52/SOUT0, P57/SOUT0, P74/SOUT0, P82/SOUT0, P86/SOUT0), and the transfer clock input/output pin (P41/SCK0, P45/SCK0, P51/SCK0, P56/SCK0, P73/SCK0, P81/SCK0, P85/SCK0) need to be set to the tertiary function for the each Port.
Figure 12-6 shows the transmit/receive operation waveforms of the synchronous serial port (16-bit length, LSB first, clock types 0).

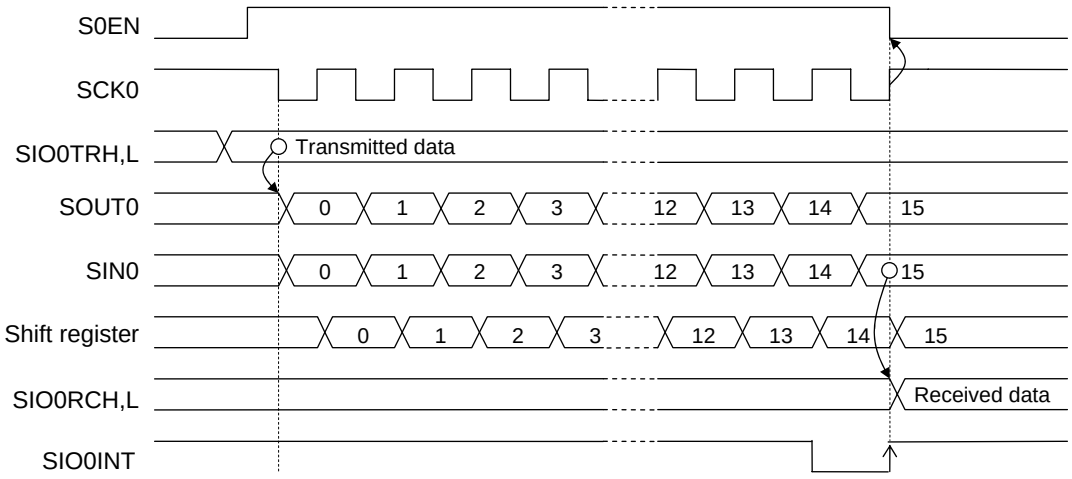


Figure 12-6 Transmit/Receive Operation Waveforms of Synchronous Serial Port (16-bit Length, LSB First, Clock Type 0)

12.4 Specifying port registers

To enable the SSIO0 function, the applicable bit of each related port register needs to be set. See Chapter 19, "Port 4", Chapter 20, "Port 5", Chapter 22, "Port 7" and Chapter 23, "Port 8" for detail about the port registers.

12.4.1 Functioning P42 (SOUT0: Output), P41 (SCK0: Input/output), and P40 (SIN0: Input) as the SSIO0/ “Master mode”

Set the P42MD1 to P40MD1 bits (P4MOD1 register bits 2 to 0) to “1” and the P42MD0 to P40MD0 bits (P4MOD0 register bits 2 to 0) to “0” for selecting the SSIO as the tertiary function of the P42, P41 and P40.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
Setting value	*	*	*	*	*	**1**	**1**	**1**

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
Setting value	*	*	*	*	*	**0**	**0**	**0**

Set P42C1-P41MC1 bits(bit2-bit1 of P4CON1 register) to “1”, set P42C0-P41C0 bits(bit2-bit1 of P4CON0 register) to “1”, and set P42DIR-P41DIR bits(bit2-bit1 of P4DIR register) to “0” for selecting the state mode of the P42 and P41 pins to CMOS output. Set the P40DIR bit (P4DIR register bit 0) to “1” for selecting the P40 as an input pin.
The set value ($) is arbitrary for the P40C1 and P40C0 bits. Select an arbitrary state mode depending on the state of the external circuit to which the P40 pin is connected.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
Setting value	*	*	*	*	*	**1**	**1**	**$**

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
Setting value	*	*	*	*	*	**1**	**1**	**$**

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
Setting value	*	*	*	*	*	**0**	**0**	**1**

The data of the P42D to P40D bits (P4D register bits 2 to 0) can either be "0" or "1".

Register name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	**P42D**	**P41D**	**P40D**
Setting value	*	*	*	*	*	****	****	****

* : Bit not related to the SSIO0 function
** : Don’t care $: Optional

12.4.2 Functioning P42 (SOUT0: Output), P41 (SCK0: Input/output), and P40 (SIN0: Input) as the SSIO0/ ”Slave mode”

Set the P42MD1 to P40MD1 bits (P4MOD1 register bits 2 to 0) to “1” and the P42MD0 to P40MD0 bits (P4MOD0 register bits 2 to 0) to “0” for selecting the SSIO as the tertiary function of the P42, P41 and P40. They are the same setting as those in the case of master mode.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	**P41MD1**	**P40MD1**
Setting value	*	*	*	*	*	**1**	**1**	**1**

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	**P41MD0**	**P40MD0**
Setting value	*	*	*	*	*	**0**	**0**	**0**

Set the P42C1 bit (P4CON1 register bit 2) to "1", the P42C0 bit (P4CON0 register bit 2) to "1", and the P42DIR bit (P4DIR register bit 2) to "0" for selecting the P42 pin state mode to CMOS output.
Set P41DIR to P40DIR bits (P4DIR register bit 1 to 0) to “1” for specifying the P41 and P40 as input pins.
The set value ($) is arbitrary for the P41C1 to P40C1 bits and for the P41C0 to P40C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P41 or P40 pin is connected.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	**P41C1**	**P40C1**
Setting value	*	*	*	*	*	**1**	**$**	**$**

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	**P41C0**	**P40C0**
Setting value	*	*	*	*	*	**1**	**$**	**$**

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
Setting value	*	*	*	*	*	**0**	**1**	**1**

The data of the P42D to P40D bits (P4D register bits 2 to 0) can either be "0" or "1".

Register name	P4 register (Address: 0F220H)							
Bit	7	6	5	4	3	**2**	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	**P42D**	**P41D**	**P40D**
Setting value	*	*	*	*	*	****	****	****

* : Bit not related to the SSIO0 function
** : Don’t care $: Optional

Chapter 13 UART

13 UART

13.1 General Description

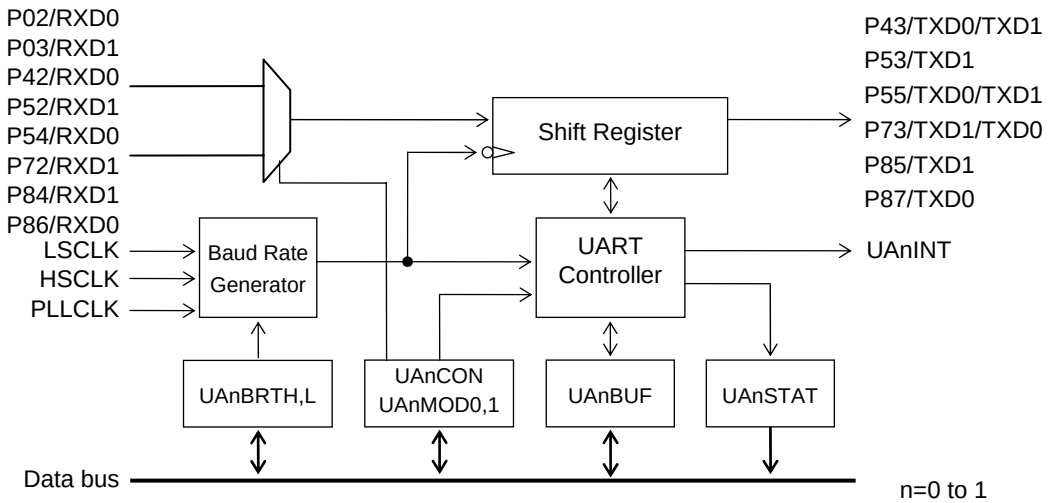
This LSI includes one channel of UART (Universal Asynchronous Receiver Transmitter), a full-duplex communication start-stop synchronous serial interface. This one full-duplex communication channel can be used as two independent half-duplex communication channels.
For input clocks, see Chapter 6, "Clock Generation Circuit".
To use the UART, it needs to be set to the secondary and quartic functions of Port 4, 5, 7, and 8. For the port 4 secondary/quartic function setting, see Chapter 19, "Port 4". For the port 5 secondary/quartic function setting, see Chapter 20, "Port 5". For the port 7 secondary/quartic function setting, see Chapter 22, "Port 7". For the port 8 secondary function setting, see Chapter 23, "Port 8".
The UART operates only when the DUA0 and DUA1 bits of the block control register 2 (BLKCON2) are "0". When the DUA0 and DUA1 bits are "1", each UART function becomes the reset state. For block control registers, see Chapter 4, "MCU Control Function".

13.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bits selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 2400 to 115200 bps.
- Internal baud rate generator.

13.1.2 Configuration

Figure 13-1 shows the configuration of the UART.



[Note] For full-duplex communication, RXD0 and TXD1 are used.

UAnBUF : UARTn transmit/receive buffer
UAnBRTH,L : UARTn baud rate registers H and L
UAnCON : UARTn control register
UAnMOD0,1 : UARTn mode registers 0, 1
UAnSTAT : UARTn status register

Figure 13-1 Configuration of UART

13.1.3 List of Pins

Pin name	I/O	Function
P02/RXD0	I	UART0 data input pin Used as the primary function of the P02 pin.
P42/RXD0	I	UART0 data input pin Used as the secondary function of the P42 pin.
P43/TXD0/TXD1	O	UART0/1 data output pin Used as the secondary or quartic function of the P43 pin.
P55/TXD0/TXD1	O	UART0/1 data output pin Used as the secondary or quartic function of the P55 pin.
P54/RXD0	I	UART0 data input pin Used as the secondary function of the P54 pin.
P52/RXD1	I	UART1 data input pin Used as the secondary function of the P52 pin.
P86/RXD0	I	UART0 data input pin Used as the secondary function of the P86 pin.
P03/RXD1	I	UART1 data input pin Used as the primary function of the P03 pin.
P53/TXD1	O	UART1 data output pin Used as the secondary function of the P53 pin.
P85/TXD1	O	UART1 data output pin Used as the secondary function of the P85 pin.
P87/TXD0	O	UART0 data output pin Used as the secondary function of the P87 pin.
P84RXD1	I	UART1 data input pin Used as the secondary function of the P84 pin.
P72/RXD1	I	UART1 data input pin Used as the secondary function of the P72 pin.
P73/TXD1/TXD0	O	UART0/1 data output pin Used as the secondary or quartic function of the P73 pin.

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F710H	UART0 transmit/receive buffer	UA0BUF	-	R/W	8	00H
0F711H	UART0 control register	UA0CON	-	R/W	8	00H
0F712H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F713H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F714H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F715H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F716H	UART0 status register	UA0STAT	-	R/W	8	00H
0F718H	UART1 transmit/receive buffer	UA1BUF	-	R/W	8	00H
0F719H	UART1 control register	UA1CON	-	R/W	8	00H
0F71AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F71BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F71CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F71DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F71EH	UART1 status register	UA1STAT	-	R/W	8	00H

13.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F710H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) used to store the receive data in the full-duplex communication.
It functions as a receive buffer in the full-duplex communication. The received data is stored in UA0BUF at termination of reception. Read the content of UABUF using the UART0 interrupt of termination of reception. At continuous reception, UA0BUF is updated whenever reception terminates. Any write to UA0BUF is disabled in receive mode. When the 5- to 7-bit data length is selected, unnecessary bits become "0".

It functions as a transmit/receive buffer in the half-duplex communication.
In transmit mode of half-duplex communication, write the transmitted data to UA0BUF. To transmit data consecutively, confirm the U0FUL flag of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to UA0BUF. Any value written to UA0BUF can be read. When the 5- to 7-bit data length is selected, unnecessary bits become invalid in the transmit mode.
The function in receive mode of half-duplex communication is the same as in the full-duplex communication.

[Note]
For operation in transmit mode of full-duplex or half-duplex communication, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting the transmitted data in UA0BUF.

13.2.3 UART1 Transmit/Receive Buffer (UA1BUF)

Address: 0F718H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1BUF	U1B7	U1B6	U1B5	U1B4	U1B3	U1B2	U1B1	U1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1BUF is a special function register (SFR) used to store the transmit data in the full-duplex communication.
It functions as a transmit buffer in the full-duplex communication. Write data to be transmitted in the UA1BUF. To transmit data consecutively, confirm the U1FUL flag of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to UA1BUF. Any value written to UA1BUF can be read. When the 5- to 7-bit data length is selected, unnecessary bits become invalid in the transmit mode.

It functions as a transmit/receive buffer in the half-duplex communication.
In transmit mode of half-duplex communication, write the transmitted data to UA1BUF. To transmit data consecutively, confirm the U1FUL flag of the UART1 status register (UA1STAT) becomes "0", then write the next transmitted data to UA1BUF. Any value written to UA1BUF can be read.
In receive mode of half-duplex communication, the data received is stored in UA1BUF at termination of reception. Read the content of UABUF using the UART1 interrupt of termination of reception. At continuous reception, UA1BUF is updated whenever reception terminates. Any write to UA1BUF is disabled in receive mode.
When the 5- to 7-bit data length is selected, unnecessary bits become "0" in the receive mode.

[Note]
For operation in transmit mode of half-duplex communication, be sure to set the transmit mode (UA1MOD0 and UA1MOD1) before setting the transmitted data in UA1BUF.

13.2.4 UART0 Control Register (UA0CON)

Address: 0F711H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) used to start/stop communication of the UART.

Description of bits

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. The full-duplex communication continues the communication operation. To terminate the communication, set the bit to "0" by software.
  In transmit mode of half-duplex communication, this bit is automatically set to "0" at termination of transmission. In receive mode of half-duplex communication, receive operation is continued. To terminate the reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication (initial value)
1	Start communication

13.2.5 UART1 Control Register (UA1CON)

Address: 0F719H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1CON	—	—	—	—	—	—	—	U1EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA1CON is a special function register (SFR) used to start/stop communication of the UART.

Description of bits

- **U1EN** (bit 0)
  This bit is enabled in half-duplex communication of UART1. In full-duplex communication, this bit is disabled.
  The U1EN bit is used to specify the UART communication operation start in half-duplex communication. When U1EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate the reception, set the bit to "0" by software.

U1EN	Description
0	Stops communication (initial value)
1	Start communication

13.2.6 UART0 Mode Register 0 (UA0MOD0)

Address: 0F712H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	U01HD	U0RSS	U0RSEL1	U0RSEL0	-	U0CK1	U0CK0	U0IO
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) used to set the transfer mode of the UART.

Description of bits

- **U01HD** (bit 7)
  The U01HD bit is set when one full-duplex communication channel is used as two half-duplex communication channels.
  When U01HD is set to "0", the combination of UART0 and UART1 operates as full-duplex communication. UART0 is fixed to receive mode and UART1 to transmit mode.
  When U01HD is set to "1", UART0 and UART1 independently operate as half-duplex communication.

U01HD	Description
0	Full-duplex communication mode (initial value)
1	Half-duplex communication mode

- **U0RSS** (bit 6)
  U0RSS is used to select the UART0 received data input sampling timing.

U0RSS	Description
0	Value set in the UA0BRTH and UA0BRTL registers/2 (initial value)
1	Value set in the UA0BRTH and UA0BRTL registers/2-1

- **U0RSEL1, U0RSEL0** (bits 5-4)
  The U0RSEL1 and U0RSEL0 bits are used to select the received data input pin for UART0.

U0RSEL1	U0RSEL0	Description
0	0	Selects the P02 pin. (Initial value)
0	1	Selects the P42 pin.
1	0	Selects the P86 pin.
1	1	Selects the P54 pin.

- **U0CK1, U0CK0** (bits 2-1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	Do not use
1	0	HSCLK
1	1	PLLCLK

- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode. Be sure to set this bit to "1" in full-duplex communication.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

Enable/disable of registers depending on full/half-duplex communication mode setting

Name	Symbol (Byte)	Full-duplex communication mode **U01HD = 1**	Half-duplex communication mode **U01HD = 0**
UART0 transmit/receive buffer	UA0BUF	○ (Only the receive buffer is enabled)	○
UART0 control register	UA0CON	○	○
UART0 mode register 0	UA0MOD0	○	○
UART0 mode register 1	UA0MOD1	○	○
UART0 baud rate register L	UA0BRTL	○	○
UART0 baud rate register H	UA0BRTH	○	○
UART0 status register	UA0STAT	○	○
UART1 transmit/receive buffer	UA1BUF	○ (Only the transmit buffer is enabled)	○
UART1 control register	UA1CON	-	○
UART1 mode register 0	UA1MOD0	-	○
UART1 mode register 1	UA1MOD1	-	○
UART1 baud rate register L	UA1BRTL	-	○
UART1 baud rate register H	UA1BRTH	-	○
UART1 status register	UA1STAT	-	○

○•••Enabled,-•••Disabled

[Note]
- Always set UA0MOD0 while communication is stopped, and do not rewrite it during communication.
- When selecting the P42 pin as the received data input pin, it is necessary to configure settings for the Port 4 secondary functions. For the secondary functions of Port 4, see Chapter 19, "Port 4".
- When selecting the P54 pin as the received data input pin, it is necessary to configure settings for the Port 5 secondary functions. For the secondary functions of Port 5, see Chapter 20, "Port 5".
- When selecting the P86 pin as the received data input pin, it is necessary to configure settings for the Port 8 secondary functions. For the secondary functions of Port 8, see Chapter 23, "Port 8".

13.2.7 UART1 Mode Register 0 (UA1MOD0)

Address: 0F71AH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1MOD0	-	U1RSS	U1RSEL1	U1RSEL0	-	U1CK1	U1CK0	U1IO
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD0 is a special function register (SFR) used to set the transfer mode of the UART.
In full-duplex communication, this register is disabled.

Description of bits

- **U1RSS** (bit 6)
  U1RSS is the bit that selects the UART1 received data input sampling timing.

U1RSS	Description
0	Value set in the UA1BRTH and UA1BRTL registers/2 (initial value)
1	Value set in the UA1BRTH and UA1BRTL registers/2-1

- **U1RSEL1, U1RSEL0** (bits 5-4)
  The U1RSEL1 and U1RSEL0 bits are used to select the received data input pin for UART1.

U1RSEL1	U1RSEL0	Description
0	0	Selects the P03 pin. (Initial value)
0	1	Selects the P84 pin.
1	0	Selects the P52 pin.
1	1	Selects the P72 pin.

- **U1CK1, U1CK0** (bits 2-1)
  The U1CK1 and U1CK0 bits are used to select the clock to be input to the baud rate generator of the UART1.

U1CK1	U1CK0	Description
0	0	LSCLK (initial value)
0	1	Do not use
1	0	HSCLK
1	1	PLLCLK

- **U1IO** (bit 0)
  The U1IO bit is used to select transmit or receive mode.

U1IO	Description
0	Transmit mode (initial value)
1	Receive mode

[Note]

- Always set UA1MOD0 while communication is stopped, and do not rewrite it during communication.
- When selecting the P52 pin as the received data input pin, it is necessary to configure settings for the Port 5 secondary functions. For the secondary functions of Port 5, see Chapter 20, "Port 5".
- When selecting the P72 pin as the received data input pin, it is necessary to configure settings for the Port 7 secondary functions. For the secondary functions of Port 7, see Chapter 22, "Port 7".
- When selecting the P84 pin as the received data input pin, it is necessary to configure settings for the Port 8 secondary functions. For the secondary functions of Port 8, see Chapter 23, "Port 8".

13.2.8 UART0 Mode Register 1 (UA0MOD1)

Address: 0F713H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	-	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) used to set the transfer mode of the UART.

Description of bits

- **U0DIR** (bit 6)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

- **U0NEG** (bit 5)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0STP** (bit 4)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bit

- **U0PT1, U0PT0** (bits 3-2)
  The U0PT1 and U0PT0 bits are used to select "even parity", "odd parity", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0LG1, U0LG0** (bits 1-0)
  The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

[Note]
Always set UA0MOD1 while communication is stopped, and do not rewrite it during communication.

13.2.9 UART1 Mode Register 1 (UA1MOD1)

Address: 0F71BH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1MOD1	-	U1DIR	U1NEG	U1STP	U1PT1	U1PT0	U1LG1	U1LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD1 is a special function register (SFR) used to set the transfer mode of the UART.
In full-duplex communication, this register is disabled.

Description of bits

- **U1DIR** (bit 6)
  The U1DIR bit is used to select LSB first or MSB first in the communication of the UART.

U1DIR	Description
0	LSB first (initial value)
1	MSB first

- **U1NEG** (bit 5)
  The U1NEG bit is used to select positive logic or negative logic in the communication of the UART.

U1NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U1STP** (bit 4)
  The U1STP bit is used to select the stop bit length in the communication of the UART.

U1STP	Description
0	1 stop bit (initial value)
1	2 stop bit

- **U1PT1, U1PT0** (bits 3-2)
  The U1PT1 and U1PT0 bits are used to select "even parity", "odd parity", or "no parity" in the communication of the UART.

U1PT1	U1PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U1LG1, U1LG0** (bits 1-0)
  The U1LG1 and U1LG0 bits are used to specify the data length in the communication of the UART.

U1LG1	U1LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

[Note]
Always set UA1MOD1 while communication is stopped, and do not rewrite it during communication.

13.2.10 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F714H
Access: R/W
Access size: 8/16 bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F715H
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 13.3.2, "Baud Rate".

[Note]
Always set UA0BRTL and UA0BRTH while communication is stopped, and do not rewrite it during communication.

13.2.11 UART1 Baud Rate Registers L, H (UA1BRTL, UA1BRTH)

Address: 0F71CH
Access: R/W
Access size: 8/16 bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA1BRTL	U1BR7	U1BR6	U1BR5	U1BR4	U1BR3	U1BR2	U1BR1	U1BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F71DH
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA1BRTH	—	—	—	—	U1BR11	U1BR10	U1BR9	U1BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA1BRTL and UA1BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks. In full-duplex communication, these registers are disabled.
For the relationship between the count value of the baud rate generator and baud rate, see Section 13.3.2, "Baud Rate".

[Note]
Always set UA1BRTL and UA1BRTH while communication is stopped. Do not rewrite them during communication.

13.2.12 UART0 Status Register (UA0STAT)

Address: 0F716H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	-	-	-	-	U0FUL	U0PER	U0OER	U0FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) used to indicate the UART state in receive operations.
When any data is written to UA0STAT, all the flags are initialized to "0".

Description of bits

- **U0FUL** (bit 3)
  U0FUL indicates the UART transmit/receive buffer state.
  When the transmitted data is written in UA0BUF in transmit mode, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U0FUL flag becomes "0", then write the next transmitted data to the UA0BUF.
  The U0FUL bit is fixed to "0" in receive mode.
  Note that, in full-duplex communication mode, the U0FUL flag reflects the U1FUL flag as the transmit mode.

U0FUL	Description
0	Full-duplex communication mode: No data in the transmit buffer (UA1BUF)(initial value)
	Half-duplex communication mode: No data in the transmit buffer (UA0BUF) during transmit operation (initial value)
1	Full-duplex communication mode: Data present in the transmit buffer (UA1BUF)
	Half-duplex communication mode: Data present in the transmit buffer (UA0BUF) during transmit operation

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1".
  U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, this bit is set to "1". U0FER is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	With framing error

13.2.13 UART1 Status Register (UA1STAT)

Address: 0F71EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1STAT	-	-	-	-	U1FUL	U1PER	U1OER	U1FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1STAT is a special function register (SFR) used to indicate the UART state in receive operations.
When any data is written to UA1STAT, all the flags are initialized to "0".
In full-duplex communication, this register is disabled.

Description of bits

- **U1FUL** (bit 3)
  U1FUL indicates the UART transmit/receive buffer state.
  When the transmitted data is written in UA1BUF in transmit mode, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U1FUL flag becomes "0", then write the next transmitted data to the UA1BUF.
  The U1FUL bit is fixed to "0" in receive mode.

U1FUL	Description
0	No data in the transmit/receive buffer (Initial value)
1	Data present in the transmit/receive buffer.

- **U1PER** (bit 2)
  The U1PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1".
  U1PER is updated each time reception is completed.
  The U1PER bit is fixed to "0" in transmit mode.

U1PER	Description
0	No parity error (initial value)
1	Parity error

- **U1OER** (bit 1)
  The U1OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA1BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U1EN bit and then reception is restarted, this bit is set to "1" unless the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U1OER bit is fixed to "0" in transmit mode.

U1OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U1FER** (bit 0)
  The U1FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, this bit is set to "1". U1FER is updated each time reception is completed.
  The U1FER bit is fixed to "0" in transmit mode.

U1FER	Description
0	No framing error (initial value)
1	With framing error

13.3 Description of Operation

13.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UARTn mode register (UAnMOD1).
Figure 13-2 and Figure 13-3 show the positive logic input/output format and negative logic input/output format, respectively.

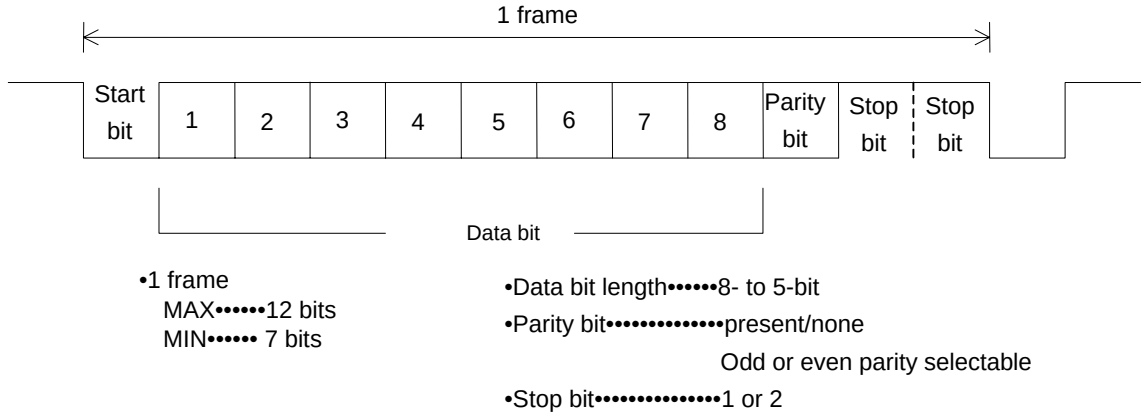


Figure 13-2 Positive Logic Input/Output Format

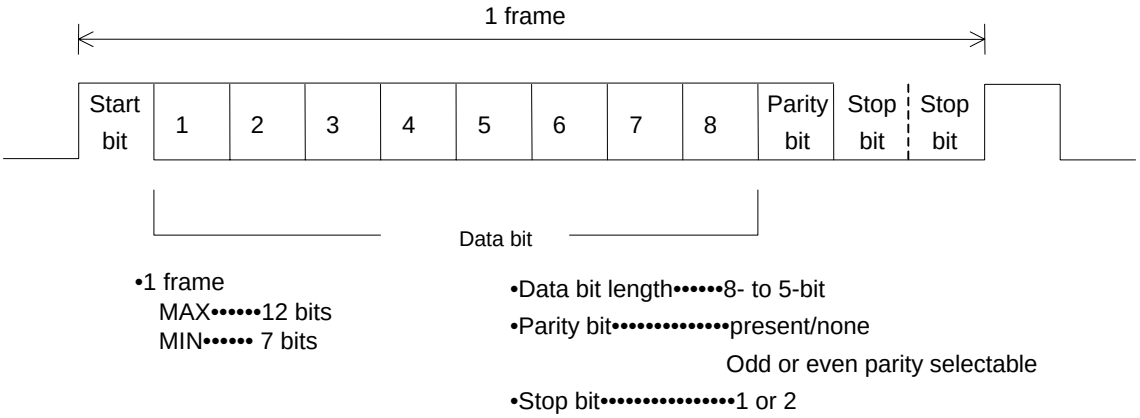


Figure 13-3 Negative Logic Input/Output Format

13.3.2 Baud Rate

Baud rates are generated by the baud rate generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (UnCK1, UnCK0) of the UARTn mode register 0 (UAnMOD0). The count value of the baud rate generator can be set by writing it in the UARTn baud rate register H or L (UAnBRTH, UAnBRTL). The maximum count is 4096.
The setting values of UAnBRTH and UAnBRTL are expressed by the following equation.

$$\text{UAnBRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 13-1 lists the count values for typical baud rates.

Table 13-1 Count Values for Typical Baud Rates

Baud rate	Baud rate generator clock selection	Baud rate generator counter value				Error
	Baud rate clock	Count value	Cycle of 1 bit	UAnBRTH	UAnBRTL	
2400 bps	8.192MHz	3413	Approx. 417 µs	0DH	054H	0.01%
4800 bps		1707	Approx. 208 µs	06H	0AAH	-0.02%
9600 bps		853	Approx. 104 µs	03H	054H	0.04%
19200 bps		427	Approx. 52 µs	01H	0AAH	-0.08%
38400 bps		213	Approx. 26 µs	00H	0D4H	0.16%
57600 bps		142	Approx. 17.4 µs	00H	08DH	0.16%
115200 bps		71	Approx. 8.7 µs	00H	046H	0.16%

13.3.3 Transmitted Data Direction

Figure 13-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

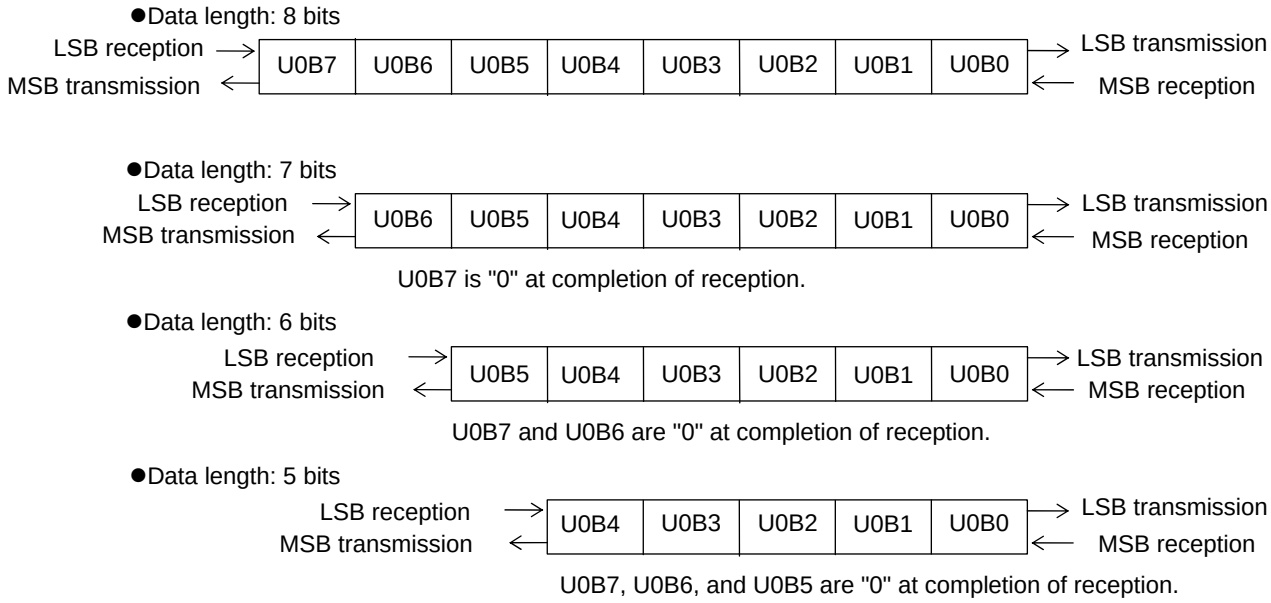


Figure 13-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

[Note]

When the TXDn pin is set to serve the secondary function output in receive mode, "H" level is output from the TXDn pin.

13.3.4 Transmit Operation

Transmission is started by setting the UnIO bit of the UARTn mode register 0 (UAnMOD0) to "0" to select the transmit mode and setting the UnEN bit of the UARTn control register (UAnCON) to "1".
Figure 13-5 shows the operation timing for transmission.

When the UnEN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmit operation.
The start bit is output to the TXDn pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UARTn interrupt is requested. In the UARTn interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UAnBUF).
When the next data to be transmitted is written to the transmit/receive buffer (UAnOBUF), the transmit buffer status flag (UnFUL) is set to "1" (③) and a UARTn interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. At this time if the UARTn interrupt routine is terminated without writing the next data to the transmit/receive buffer, the UnFUL bit is not set to "1" (⑤). The transmit operation stops when the stop bit is sent, the UnEN bit is reset to "0", and the UARTn interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

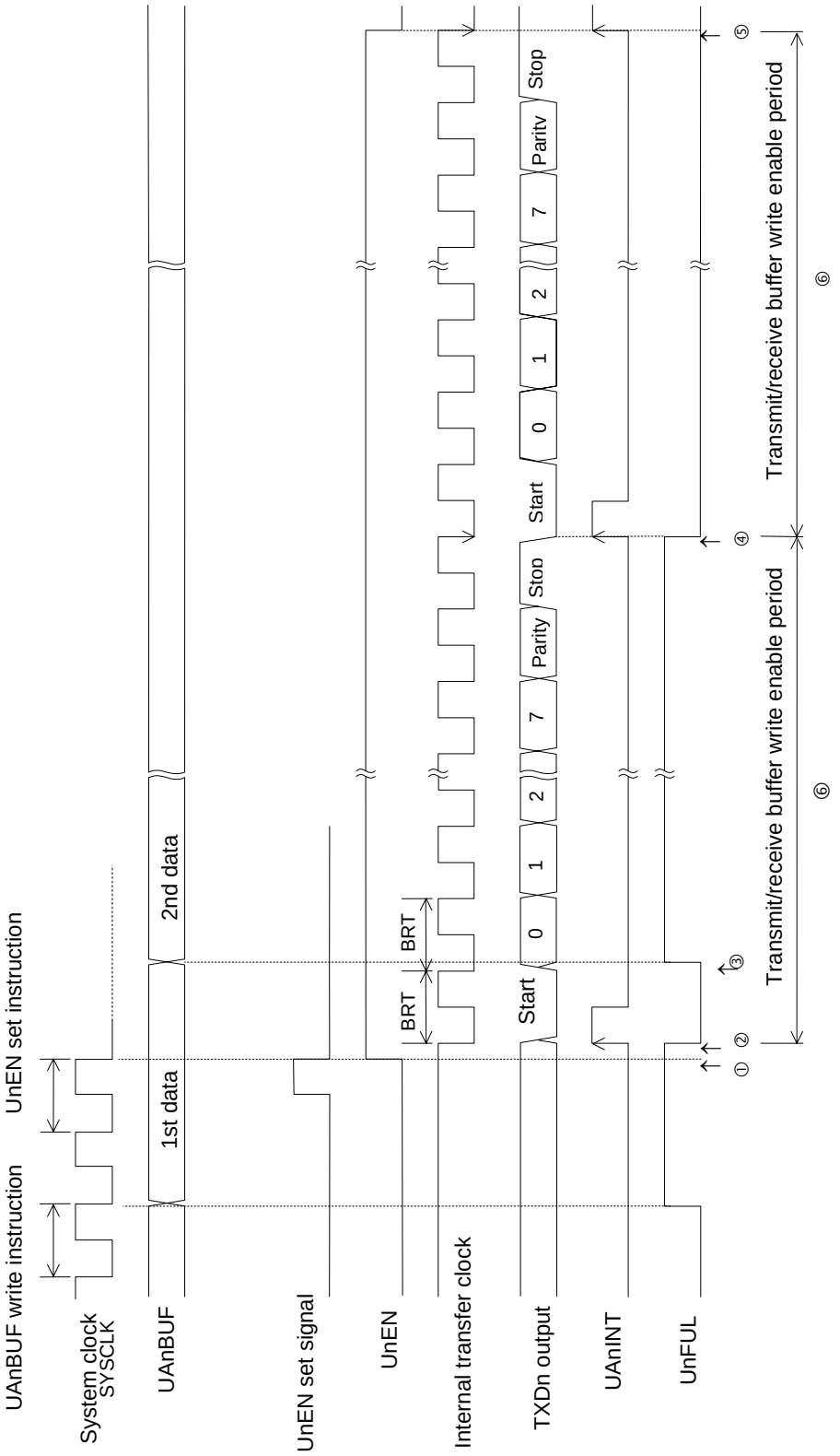


Figure 13-5 Operation Timing in Transmission

13.3.5 Receive Operation

Select the receive data pin using the UnRSEL bit of the UARTn mode register 0 (UAnMOD0). Reception is started by setting the UnIO bit of the UARTn mode register 0 (UAnMOD0) to "1" to select the receive mode and setting the UnEN bit of the UARTn control register (UAnCON) to "1".
Figure 13-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXDn and waits for the arrival of a start bit. When detecting a start bit (②), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXDn on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the transmit/receive buffer (UAnBUF) concurrently with the falling edge of the internal transfer clock of ③.
The LSI requests a UARTn interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UARTn status register (UAnSTAT) to "1".

Parity error : SnPER =“1”
Overrun error : SnOER =“1”
Framing error : SnFER =“1”

As shown in Figure 13-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the UnEN bit is reset to "0" by the program. When the UnEN bit is reset to "0" during reception, the received data may be destroyed. When the UnEN bit is reset to "0" during the "UnEN reset enable period" in Figure 13-6, the received data is protected.

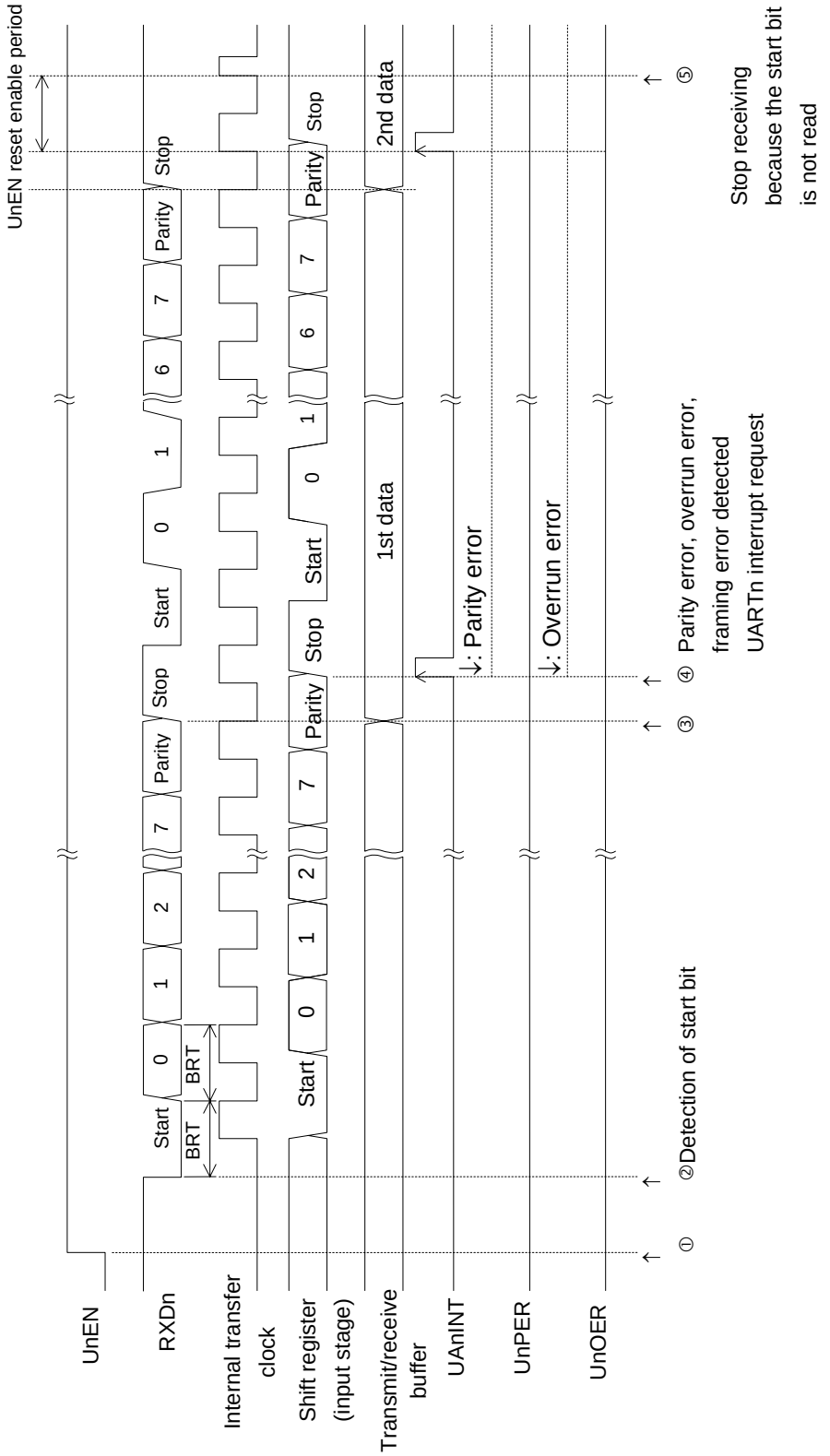


Figure 13-6 Operation Timing in Reception

13.3.5.1 Detection of Start Bit

The start bit is sampled with the baud rate generator clock (HSCLK). Therefore, the start bit detection may be delayed for one cycle of the baud rate generator clock at the maximum.
Figure 13-7 shows the start bit detection timing.

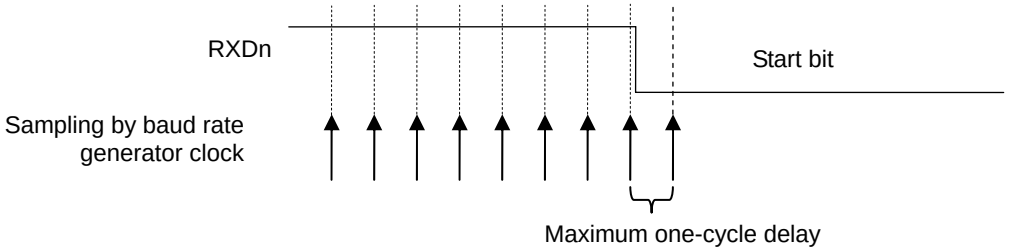
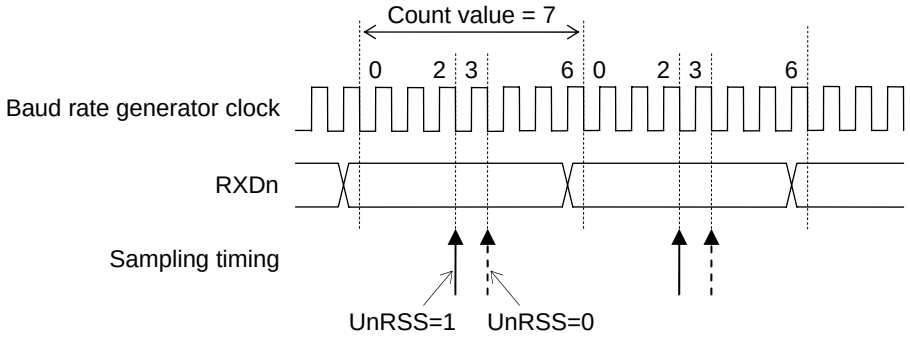


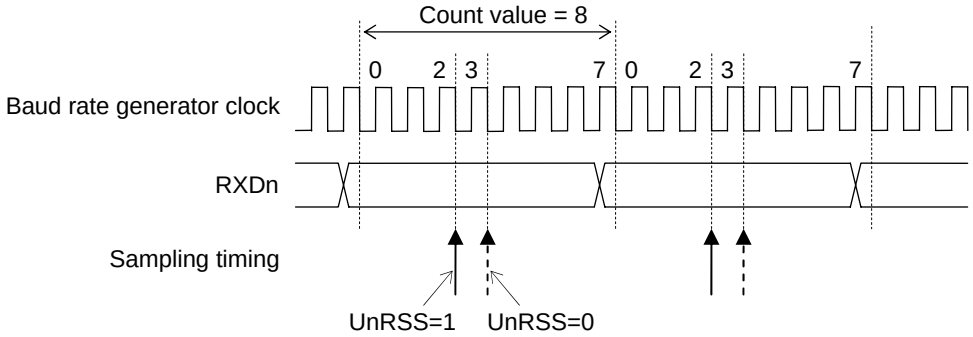
Figure 13-7 Start Bit Detection Timing (Positive Logic)

13.3.5.2 Sampling Timing

When the start bit is detected, the received data that was input to the RXDn is sampled almost at the center of the baud rate, then loaded to the shift register.
The loading sampling timing of this shift register can be adjusted for one clock of the baud rate generator clock, using the UnRSS bit of the UARTn mode register 0 (UAnMOD0).
Figure 13-8 shows the relationship between the UnRSS bit and the sampling timing.



(1) When the baud rate generator count value is "7" (odd)



(2) When the baud rate generator count value is "8" (even)

Figure 13-8 Relationship between UnRSS Bit and Sampling Timing

13.3.5.3 Receive Margin

If there is an error between the sender baud rate and the baud rate generated by the baud rate generator of this LSI, the error accumulates until the last stop bit loading in one frame, decreasing the receive margin.
Figure 13-9 shows the baud rate errors and receive margin waveforms.

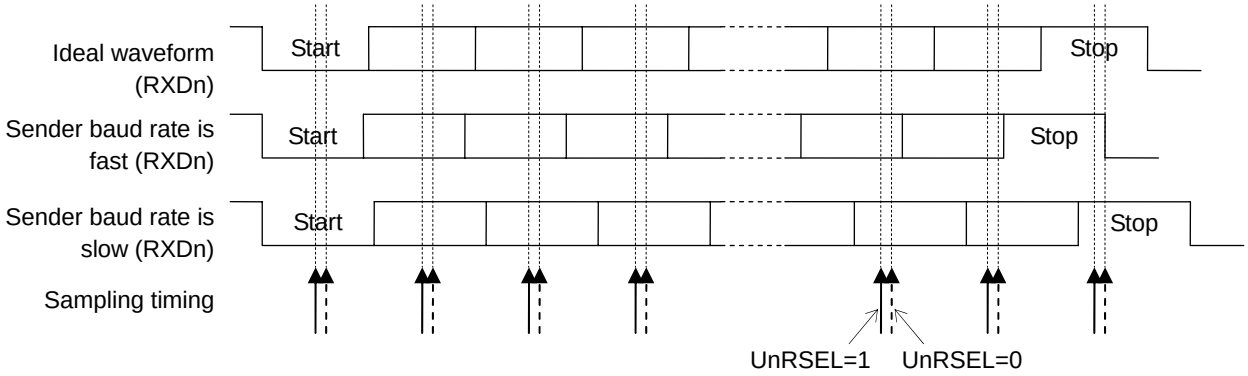


Figure 13-9 Baud Rate Error and Receive Margin

[Note]

In system designing, ensure a sufficient receive margin considering the baud rate difference between sender and receiver, start bit detection delay, distortion in receive data, and influence of noise.

13.4 Specifying Port Registers

To enable the UART function, the applicable bit of each related port register needs to be set. See Chapter 15, "Port 0", Chapter 19, "Port 4", Chapter 20, "Port 5", Chapter 22, "Port 7", and Chapter 23, "Port 8" for details about the port registers.

13.4.1 Functioning P53 (TXD1: Output) and P54 pins (RXD0: Input) as the UART (Full-duplex)

Set the P54MD1 to P53MD1 bits (bits 4 to 3 of P5MOD1 register) to "0", and set the P54MD0 to P53MD0 bits (bits 4 to 3 of P5MOD0 register) to "1", for specifying the UART as the secondary function of P53 and P54.

Register name	P5MOD1 register (address: 0F257H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57MD1	P56MD1	P55MD1	**P54MD1**	**P53MD1**	P52MD1	P51MD1	P50MD1
Setting value	*	*	*	**0**	**0**	*	*	*

Register name	P5MOD0 register (address: 0F256H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57MD0	P56MD0	P55MD0	**P54MD0**	**P53MD0**	P52MD0	P51MD0	P50MD0
Setting value	*	*	*	**1**	**1**	*	*	*

Set the P53C1 bit (bit 3 of P5CON1 register) to "1", the P53C0 bit (bit 3 of P5CON0 register) to "1", and the P53DIR bit (bit 3 of P5DIR register) to "0", for specifying the state mode of the P53 pin to CMOS output.
Set the P54DIR bit (bit 4 of P5DIR register) to "1" for selecting the P54 as an input pin.
The set value ($) is arbitrary for the P54C1 and P54C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P54 pin is connected.

Register name	P5CON1 register (address: 0F255H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57C1	P56C1	P55C1	**P54C1**	**P53C1**	P52C1	P51C1	P50C1
Setting value	*	*	*	**$**	**1**	*	*	*

Register name	P5CON0 register (address: 0F254H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57C0	P56C0	P55C0	**P54C0**	**P53C0**	P52C0	P51C0	P50C0
Setting value	*	*	*	**$**	**1**	*	*	*

Register name	P5DIR register (address: 0F253H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57DIR	P56DIR	P55DIR	**P54DIR**	**P53DIR**	P52DIR	P51DIR	P50DIR
Setting value	*	*	*	**1**	**0**	*	*	*

The data for the P54D to D53D bits (bits 4 to 3 of P5D register) can be "0" or "1".

Register name	P5D register (address: 0F252H)							
Bit	7	6	5	**4**	**3**	2	1	0
Bit name	P57D	P56D	P55D	**P54D**	**P53D**	P52D	P51D	P50D
Setting value	*	*	*	******	******	*	*	*

* : Bit not related to the UART function
** : Don't care $: Arbitrarily

13.4.2 Functioning P43 (TXD1: Output) and P02 pins (RXD0: Input) as the UART (Full-duplex)

Set the P43MD1 bit (bit 3 of P4MOD1 register) to "1" and set the P43MD0 bit (bit 3 of P4MOD0 register) to "1", to specify the UART as the quartic function of P43.

Register name	P4MOD1 register (Address: 0F249H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	*	**1**	$	*	*

Register name	P4MOD0 register (Address: 0F248H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	*	**1**	$	*	*

Set the P43C1 bit (bit 3 of P4CON1 register) to "1", the P43C0 bit (bit 3 of P4CON0 register) to "1", and the P43DIR bit (bit 3 of P4DIR register) to "0" for specifying the state mode of the P43 pin to CMOS output.

Register name	P4CON1 register (Address: 0F247H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4CON0 register (Address: 0F246H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4DIR register (Address: 0F245H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	*	**0**	*	*	*

The data for the P43D bit (bit 3 of P4D register) can be "0" or "1".

Register name	P4D register (Address: 0F244H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Setting value	*	*	*	*	**	*	*	*

The P02 pin is an input-only pin and does not need input/output selection by the register. The set value ($) is arbitrary for the P02C1 and P02C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P02 pin is connected.

Register name	P0CON1 register (Address: 0F20FH)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	P05C1	P04C1	P03C1	**P02C1**	P01C1	P00C1
Setting value	-	-	*	*	*	**$**	*	*

Register name	P0CON0 register (Address: 0F20EH)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	P05C0	P04C0	P03C0	**P02C0**	P01C0	P00C0
Setting value	-	-	*	*	*	**$**	*	*

The data for the P02D bit (bit 2 of P0D register) can be "0" or "1".

Register name	P0D register (Address: 0F20CH)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	P05D	P04D	P03D	**P02D**	P01D	P00D
Setting value	-	-	*	*	*	****	*	*

- : Bit that does not exist
* : Bit not related to the UART function
** : Don’t care $: Arbitrarily

[Note]
- The receive pin (RXD) is selected by the U0RSEL bit (bits 5 to 4) of UA0MOD0 register. The initial value "00" selects the P02 and the value "01" selects the P42.
- Even if the P42 pin is selected as RXD0 by the P42MD1, P42MD0, P42C1, P42C0, and P42DIR bits, the P02 pin will be selected as RXD0 when the U0RSEL bit of UA0MOD0 register is "00".
- P02 (Port 0) does not have the registers used to select data direction (input or output) and mode (primary or secondary function).

13.4.3 Functioning P85 (TXD1: Output) and P86 pins (RXD0: Input) as the UART (Full-duplex)

Set the P86MD1 to P85MD1 bits (bits 6 to 5 of P8MOD1 register) to "0", and set the P86MD0 to P85MD0 bits (bits 6 to 5 of P8MOD0 register) to "1", for specifying the UART as the secondary function of P86 and P85.

Register name	P8MOD1 register (Address: 0F281H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87MD1	**P86MD1**	**P85MD1**	P84MD1	P83MD1	-	-	-
Setting value	*	**0**	**0**	*	*	-	-	-

Register name	P8MOD0 register (Address: 0F280H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87MD0	**P86MD0**	**P85MD0**	P84MD0	P83MD0	-	-	-
Setting value	*	**1**	**1**	*	*	-	-	-

Set the P85C1 bit (bit 5 of P8CON1 register) to "1", the P85C0 bit (bit 5 of P8CON0 register) to "1", and the P85DIR bit (bit 5 of P8DIR register) to "0", for specifying the state mode of the P85 pin to CMOS output.
Set the P86DIR bit (bit 6 of P8DIR register) to "1" for selecting the P86 as an input pin.
The set value ($) is arbitrary for the P86C1 and P86C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P86 pin is connected.

Register name	P8CON1 register (Address: 0F27FH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87C1	**P86C1**	**P85C1**	P84C1	P83C1	-	-	-
Setting value	*	**$**	**1**	*	*	-	-	-

Register name	P8CON0 register (Address: 0F27EH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87C0	**P86C0**	**P85C0**	P84C0	P83C0	-	-	-
Setting value	*	**$**	**1**	*****	*****	-	-	-

Register name	P8DIR register (Address: 0F27DH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87DIR	**P86DIR**	**P85DIR**	P84DIR	P83DIR	-	-	-
Setting value	*	**1**	**0**	*****	*****	-	-	-

The data for the P86D to P85D bits (bits 6 to 5 of P8D register) can be "0" or "1".

Register name	P8D register (Address: 0F27CH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	P87D	**P86D**	**P85D**	P84D	P83D	-	-	-
Setting value	*	******	******	*****	*****	-	-	-

* : Bit not related to the UART function
** : Don't care $: Arbitrarily

13.4.4 Functioning P53 (TXD1: Output) and P03 pins (RXD1: Input) as the UART (Half-duplex)

Set the P53MD1 bit (bit 3 of P5MOD1 register) to "0" and set the P53MD0 bit (bit 3 of P5MOD0 register) to "1", to specify the UART as the secondary function of P53.

Register name	P5MOD1 register (address: 0F257H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57MD1	P56MD1	P55MD1	P54MD1	**P53MD1**	-	-	-
Setting value	*	*	*	*	**0**	-	-	-

Register name	P5MOD0 register (address: 0F256H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57MD0	P56MD0	P55MD0	P54MD0	**P53MD0**	-	-	-
Setting value	*	*	*	*	**1**	-	-	-

Set the P53C1 bit (bit 3 of P5CON1 register) to "1", the P53C0 bit (bit 3 of P5CON0 register) to "1", and the P53DIR bit (bit 3 of P5DIR register) to "0", for specifying the state mode of the P53 pin to CMOS output.

Register name	P5CON1 register (address: 0F255H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57C1	P56C1	P55C1	P54C1	**P53C1**	-	-	-
Setting value	*	*	*	*	**1**	-	-	-

Register name	P5CON0 register (address: 0F254H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57C0	P56C0	P55C0	P54C0	**P53C0**	-	-	-
Setting value	*	*	*	*	**1**	-	-	-

Register name	P5DIR register (address: 0F253H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57DIR	P56DIR	P55DIR	P54DIR	**P53DIR**	-	-	-
Setting value	*	*	*	*	**0**	-	-	-

The data for the P53D bit (bit 3 of P5D register) can be "0" or "1".

Register name	P5D register (address: 0F252H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P57D	P56D	P55D	P54D	**P53D**	-	-	-
Setting value	*	*	*	*	**	-	-	-

The P03 pin is an input-only pin and does not need input/output selection by the register. The set value ($) is arbitrary for the P03C1 and P03C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P03 pin is connected.

Register name	P0CON1 register (Address: 0F20FH)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	-	-	P05C1	P04C1	**P03C1**	P02C1	P01C1	P00C1
Setting value	-	-	*	*	**$**	*	*	*

Register name	P0CON0 register (Address: 0F20EH)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	-	-	P05C0	P04C0	**P03C0**	P02C0	P01C0	P00C0
Setting value	-	-	*	*	**$**	*	*	*

The data for the P03D bit (bit 2 of P0D register) can be "0" or "1".

Register name	P0D register (Address: 0F20CH)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	-	-	P05D	P04D	**P03D**	P02D	P01D	P00D
Setting value	-	-	*	*	****	*	*	*

- : Bit that does not exist
* : Bit not related to the UART function
** : Don’t care $: Arbitrarily

[Note]
- The receive pin (RXD) is selected by the U1RSEL bit (bit 4) of UA1MOD0 register. The initial value "0" selects the P03 and the value "1" selects the P84.
- Even if the P84 pin is selected as RXD1 by the P84MD1, P84MD0, P84C1, P84C0, and P84DIR bits, the P03 pin will be selected as RXD1 when the U1RSEL bit of UA1MOD0 register is "0".
- P03 (Port 0) does not have the registers used to select data direction (input or output) and mode (primary or secondary function).

13.4.5 Functioning P55 (TXD0: Output) and P42 pins (RXD0: Input) as the UART (Half-duplex)

Set the P55MD1 bit (bit 5 of P5MOD1 register) to "1" and set the P55MD0 bit (bit 5 of P5MOD0 register) to "1", to specify the UART as the secondary function of P55.

Register name	P5MOD1 register (address: 0F257H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57MD1	P56MD1	**P55MD1**	P54MD1	P53MD1	-	-	-
Setting value	*	*	**0**	*	*****	-	-	-

Register name	P5MOD0 register (address: 0F256H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57MD0	P56MD0	**P55MD0**	P54MD0	P53MD0	-	-	-
Setting value	*	*	**1**	*	*****	-	-	-

Set the P55C1 bit (bit 5 of P5CON1 register) to "1", the P55C0 bit (bit 5 of P5CON0 register) to "1", and the P55DIR bit (bit 5 of P5DIR register) to "0" for specifying the state mode of the P55 pin to CMOS output.

Register name	P5CON1 register (address: 0F255H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57C1	P56C1	**P55C1**	P54C1	P53C1	-	-	-
Setting value	*	*	**1**	*	*****	-	-	-

Register name	P5CON0 register (address: 0F254H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57C0	P56C0	**P55C0**	P54C0	P53C0	-	-	-
Setting value	*	*	**1**	*	*****	-	-	-

Register name	P5DIR register (address: 0F253H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57DIR	P56DIR	**P55DIR**	P54DIR	P53DIR	-	-	-
Setting value	*	*	**0**	*	*	-	-	-

The data for the P55D bit (bit 5 of P5D register) can be "0" or "1".

Register name	P5D register (address: 0F252H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P57D	P56D	**P55D**	P54D	P53D	-	-	-
Setting value	*	*	******	*	*****	-	-	-

Set the P42MD1 bit (bit 2 of P4MOD1 register) to "0" and set the P42MD0 bit (bit 2 of P4MOD0 register) to "1", to specify the UART as the secondary function of P42.

Register name	P4MOD1 register (Address: 0F249H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	**P42MD1**	P41MD1	P40MD1
Setting value	*	*	*	*	*	**0**	*	*

Register name	P4MOD0 register (Address: 0F248H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	**P42MD0**	P41MD0	P40MD0
Setting value	*	*	*	*	*	**1**	*	*

Set the P42DIR bit (bit 2 of P4DIR register) to "1" for selecting the P42 as an input pin.
The set value ($) is arbitrary for the P42C1 and P42C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P42 pin is connected.

Register name	P4CON1 register (Address: 0F247H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	**P42C1**	P41C1	P40C1
Setting value	*	*	*	*	*	**$**	*	*

Register name	P4CON0 register (Address: 0F246H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	**P42C0**	P41C0	P40C0
Setting value	*	*	*	*	*	**$**	*	*

Register name	P4DIR register (Address: 0F245H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	**P42DIR**	P41DIR	P40DIR
Setting value	*	*	*	*	*	**1**	*	*

The data for the P43D to D42D bits (bits 3 to 2 of P4D register) can be "0" or "1".

Register name	P4D register (Address: 0F244H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	P47D	P46D	P45D	P44D	P43D	**P42D**	P41D	P40D
Setting value	*	*	*	*	*	******	*	*

* : Bit not related to the UART function
** : Don’t care $: Arbitrarily

13.4.6 Functioning P43 (TXD0: Output) and P54 pins (RXD0: Input) as the UART (Half-duplex)

Set the P43MD1 bit (bit 3 of P4MOD1 register) to "0" and set the P43MD0 bit (bit 3 of P4MOD0 register) to "1", to specify the UART as the secondary function of P43.

Register name	P4MOD1 register (Address: 0F249H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	*	**0**	$	*	*

Register name	P4MOD0 register (Address: 0F248H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	*	**1**	$	*	*

Set the P43C1 bit (bit 3 of P4CON1 register) to "1", the P43C0 bit (bit 3 of P4CON0 register) to "1", and the P43DIR bit (bit 3 of P4DIR register) to "0" for specifying the state mode of the P43 pin to CMOS output.

Register name	P4CON1 register (Address: 0F247H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4CON0 register (Address: 0F246H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4DIR register (Address: 0F245H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	*	**0**	*	*	*

The data for the P43D bit (bit 3 of P4D register) can be "0" or "1".

Register name	P4D register (Address: 0F244H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Setting value	*	*	*	*	**	*	*	*

Set the P54MD1 bit (bit 4 of P5MOD1 register) to "0" and set the P54MD0 bit (bit 4 of P5MOD0 register) to "1", to specify the UART as the secondary function of P54.

Register name	P5MOD1 register (address: 0F257H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57MD1	P56MD1	P55MD1	**P54MD1**	P53MD1	-	-	-
Setting value	*	*	*	**0**	*	-	-	-

Register name	P5MOD0 register (address: 0F256H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57MD0	P56MD0	P55MD0	**P54MD0**	P53MD0	-	-	-
Setting value	*	*	*	**1**	*	-	-	-

Set the P54DIR bit (bit 4 of P5DIR register) to "1" for selecting the P54 as an input pin.
The set value ($) is arbitrary for the P54C1 and P54C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P54 pin is connected.

Register name	P5CON1 register (address: 0F255H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57C1	P56C1	P55C1	**P54C1**	P53C1	-	-	-
Setting value	*	*	*	**$**	*	-	-	-

Register name	P5CON0 register (address: 0F254H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57C0	P56C0	P55C0	**P54C0**	P53C0	-	-	-
Setting value	*	*	*	**$**	*	-	-	-

Register name	P5DIR register (address: 0F253H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57DIR	P56DIR	P55DIR	**P54DIR**	P53DIR	-	-	-
Setting value	*	*	*	**1**	*	-	-	-

The data for the P54D bit (bit 4 of P5D register) can be "0" or "1".

Register name	P5D register (address: 0F252H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P57D	P56D	P55D	**P54D**	P53D	-	-	-
Setting value	*	*	*	******	*	-	-	-

* : Bit not related to the UART function
** : Don’t care $: Arbitrarily

13.4.7 Functioning P85 (TXD1: Output) and P72 pins (RXD1: Input) as the UART (Half-duplex)

Set the P85MD1 bit (bit 5 of P8MOD1 register) to "0", and set the P85MD0 bit (bit 5 of P8MOD0 register) to "1", for specifying the UART as the secondary function of P85.

Register name	P8MOD1 register (Address: 0F2E3H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87MD1	P86MD1	**P85MD1**	P84MD1	P83MD1	P82MD1	P81MD1	P80MD1
Setting value	*	*	**0**	$	*	*	*	*

Register name	P8MOD0 register (Address: 0F2E2H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87MD0	P86MD0	**P85MD0**	P84MD0	P83MD0	P82MD0	P81MD0	P80MD0
Setting value	*	*	**1**	$	*	*	*	*

Set the P85C1 bit (bit 5 of P8CON1 register) to "1", the P83C0 bit (bit 5 of P8CON0 register) to "1", and the P85DIR bit (bit 5 of P8DIR register) to "0", for specifying the state mode of the P85 pin to CMOS output.

Register name	P8CON1 register (Address: 0F2E1H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87C1	P86C1	**P85C1**	P84C1	P83C1	P82C1	P81C1	P80C1
Setting value	*	*	**1**	*	*	*	*	*

Register name	P8CON0 register (Address: 0F2E0H)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87C0	P86C0	**P85C0**	P84C0	P83C0	P82C0	P81C0	P80C0
Setting value	*	*	**1**	*	*	*	*	*

Register name	P8DIR register (Address: 0F2DFH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87DIR	P86DIR	**P85DIR**	P84DIR	P83DIR	P82DIR	P81DIR	P80DIR
Setting value	*	*	**0**	*	*	*	*	*

The data for the P85D bit (bit 5 of P8D register) can be "0" or "1".

Register name	P8D register (Address: 0F2DEH)							
Bit	7	6	**5**	4	3	2	1	0
Bit name	P87D	P86D	**P85D**	P84D	P83D	P82D	P81D	P80D
Setting value	*	*	******	*	*	*	*	*

Set the P72MD1 bit (bit 2 of P7MOD1 register) to "0" and set the P72MD0 bit (bit 2 of P7MOD0 register) to "1", to specify the UART as the secondary function of P72.

Register name	P7MOD1 register (Address: 0F273H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74MD1	P73MD1	**P72MD1**	P71MD1	P70MD1
Setting value	-	-	-	*	*	**0**	*	*

Register name	P7MOD0 register (Address: 0F272H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74MD0	P73MD0	**P72MD0**	P71MD0	P70MD0
Setting value	-	-	-	*	*	**1**	*	*

Set the P72DIR bit (bit 2 of P7DIR register) to "1" for selecting the P72 as an input pin.
The set value ($) is arbitrary for the P72C1 and P72C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P72 pin is connected.

Register name	P7CON1 register (Address: 0F271H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74C1	P73C1	**P72C1**	P71C1	P70C1
Setting value	-	-	-	*	*	**$**	*	*

Register name	P7CON0 register (Address: 0F270H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74C0	P73C0	**P72C0**	P71C0	P70C0
Setting value	-	-	-	*	*	**$**	*	*

Register name	P7DIR register (Address: 0F26FH)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74DIR	P73DIR	**P72DIR**	P71DIR	P70DIR
Setting value	-	-	-	*	*	**1**	*	*

The data for the P72D bit (bit 2 of P7D register) can be "0" or "1".

Register name	P7D register (Address: 0F26EH)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	P74D	P73D	**P72D**	P71D	P70D
Setting value	-	-	-	*	*	******	*	*

* : Bit not related to the UART function
** : Don’t care $: Arbitrarily

Chapter 14 I^2C Bus Interface

14 I^{2}C Bus Interface

14.1 General Description

This LSI includes 1 channel of I2C bus interface (master).
The I^{2}C bus interface data I/O pin and the I^{2}C bus interface clock I/O pin are assigned as the secondary function of the ports 4, 5, 6, and port 8. For the ports 4, 5, 6 and port 8, see Chapter 19 “Port 4”, Chapter 20 “Port 5”, Chapter 21 “Port 6” and Chapter 23 “Port 8”.

14.1.1 Features

- Master function
- Communication speeds supported include standard mode (100kbps) and fast mode (400kbps).
- 7-bit address format (10-bit address can be supported)
- Support clock synchronization (handshake).

14.1.2 Configuration

Figure 14-1 shows the configuration of the I^{2}C bus interface.

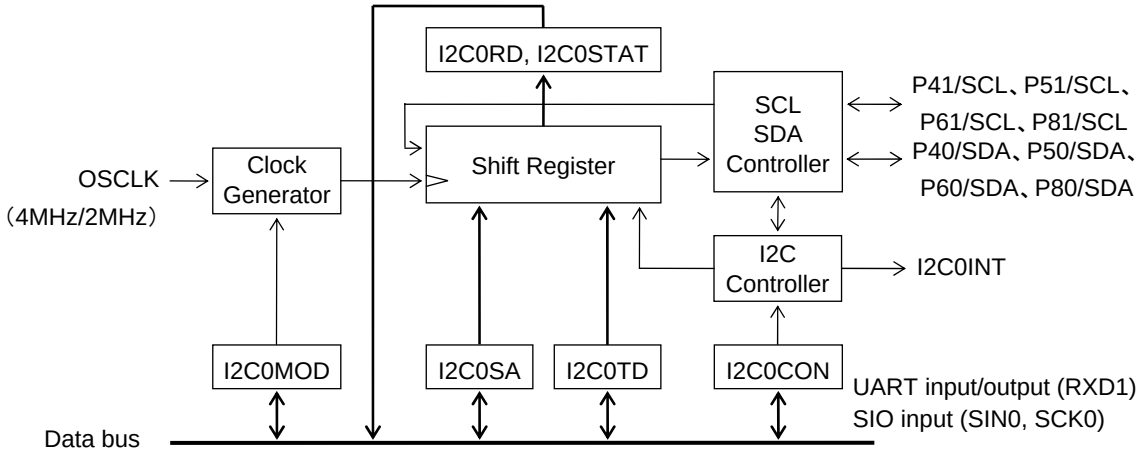


Figure 14-1 Configuration of I^{2}C Bus Interface

14.1.3 List of Pins

Pin name	I/O	Description
P40/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P40 pin.
P41/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P41 pin.
P50/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P50 pin.
P51/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P51 pin.
P60/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P60 pin.
P61/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P61 pin.
P80/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P80 pin.
P81/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P81 pin.

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Word)	Symbol (Byte)	R/W	Size	Initial value
0F740H	I^2C bus 0 receive register	–	I2C0RD	R	8	0000H
0F741H			–	–	–	
0F742H	I^2C bus 0 slave address register	–	I2C0SA	R/W	8	0000H
0F743H			–	–	–	
0F744H	I^2C bus 0 transmit data register	–	I2C0TD	R/W	8	0000H
0F745H			–	–	–	
0F746H	I^2C bus 0 control register	I2C0CON	I2C0CON0	R/W	16/8	0000H
0F747H			–	–	–	
0F748H	I^2C bus 0 mode register	I2C0MOD	I2C0MODL	R/W	16/8	0200H
0F749H			I2C0MODH	R/W	8	
0F74AH	I^2C bus 0 status register	I2C0STA	I2C0STAL	R	16/8	0000H
0F74BH			–	–	–	

14.2.2 I²C Bus 0 Receive Data Register (I2C0RD)

Address: 0F740H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0RD	I20R7	I20R6	I20R5	I20R4	I20R3	I20R2	I20R1	I20R0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0RD is a read-only special function register (SFR) to store the received data.
I2C0RD is updated after completion of each reception.

[Description of Bits]

- **I20R7 to I20R0** (bits 7-0)
  The I20R7 to I20R0 bits are used to store the received data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

14.2.3 I²C Bus 0 Slave Address Register (I2C0SA)

Address: 0F742H
Access: R/W
Access size: 8 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
I2C0SA	I20A6	I20A5	I20A4	I20A3	I20A2	I20A1	I20A0	I20RW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

- **I20A6 to I20A0** (bits 7-1)
  The I20A6 to I20A0 bits are used to set the address of the communication partner.

- **I20RW** (bit 0)
  The I20RW bit is used to select the data transmit mode (write) or data receive mode (read).

I20RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

14.2.4 I²C Bus 0 Transmit Data Register (I2C0TD)

Address: 0F744H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0TD0	I20T7	I20T6	I20T5	I20T4	I20T3	I20T2	I20T1	I20T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0TD is a special function register (SFR) used to set the transmitted data.

[Description of Bits]

- **I20T7 to 0** (bits 7-0)
  The I20T7 to 0 bits are used to set the transmit data.

14.2.5 I²C Bus 0 Control Register (I2C0CON)

Address: 0F746H
Access: R/W
Access size: 16/8 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
I2C0CON0	I20ACT	-	-	-	-	I20RS	I20SP	I20ST
R/W	R/W	R	R	R	R	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
I2C0CON1	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I20ACT** (bit 7)
  The I20ACT bit is used to set the acknowledge signal to be output at completion of reception.

I20ACT	Description
0	Acknowledgment data “0” (initial value)
1	Acknowledgment data “1”

- **I20RS** (bit 2)
  The I20RS bit is a write-only bit used to request a restart. When this bit is set to “1” during data communication, the I²C bus shifts to the restart condition and communication restarts from the slave address. I20RS can be set to “1” only while communication is active (I20ST =“1”). When the I20RS bit is read, “0” is always read.

I20RS	Description
0	No restart request (initial value)
1	Restart request

- **I20SP** (bit 1)
  The I20SP bit is a write-only bit used to request a stop condition. When the I20SP bit is set to “1”, the bus shifts to the stop condition and communication stops. When the I20SP bit is read, “0” is always read.

I20SP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I20ST** (bit 0)
  The I20ST bit is used to control the communication operation of the I²C bus interface. When the I2nST bit is set to “1”, communication starts. When “1” is overwritten to the I20ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication restarts. When the I20ST bit is set to “0”, communication is stopped forcibly.
  The I20ST bit can be set to “1” only when the I²C bus interface is in an operation enable state (I20EN = “1”). When the I2nSP bit is set to “1”, the I20ST bit is set to “0”.

I20ST	Description
0	Stops communication (initial value)
1	Start communication

14.2.6 I²C Bus 0 Mode Register (I2C0MOD)

Address: 0F748H
Access: R/W
Access size: 16/8 bits
Initial value: 0200H

	7	6	5	4	3	2	1	0
I2C0MODL	—	—	—	—	I20DW1	I20DW0	I20MD	I20EN
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
I2C0MODH	-	-	-	-	-	-	I20CD1	I20CD0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

I2C00MOD is a special function register (SFR) used to set the operation mode.

[Description of Bits]

- **I20CD1, I20CD0** (bits 9, 8)
  The I20CD1 and I20CD0 bits are used to set the operating frequency of I²C. Set a frequency division value of OSCLK. Make sure that the clock input to I²C is 4MHz or less. Proper operation cannot be guaranteed if the frequency division value exceeds 4MHz. Table 14-1 shows the relationship between the setting values of OSCLK, I20CD1, and I20CD0 and the communication speed.

I20CD1	**I20CD0**	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK (initial value)
1	1	Setting prohibited

- **I20SYN** (bit 4)
  The I20SYN bit is used to select whether or not to use the clock synchronization function (handshake function).

I20SYN	Description
0	Do not use clock synchronization (Initial value)
1	Use clock synchronization

- **I20DW1, I20DW0** (bits 3-2)
  The I20DW1 and I20DW0 bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kbps/400kbps.

I20DW1	**I20DW0**	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

- **I20MD** (bit 1)
  The I20MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected. The communication speed varies depending on the setting value of the SYSC2, SYSC1, and SYSC0 bits of the frequency control register (FCON0). For details, see “Table 14-1 Relationship between Communication Speeds and SYSC2, SYSC1, and SYSC0 Bits”.

I20MD	Description
0	Standard mode (initial value)/100 kbps
1	Fast mode/400 kbps

- **I20EN** (bit 0)
  The I20EN bit is used to enable the operation of the I^2C bus interface. Only when I20EN is "1", the I20ST bit can be set and the I2C0 bus becomes available. When I20EN is set to "0", all the SFRs related to I^2C bus n (I2C0MODH register is excluded) are initialized.

I20EN	Description
0	Stops I^2C operation (initial value)
1	Enables I^2C operation

Table 14-1 Relationship between Communication Speeds and SYSC2, SYSC1, and SYSC0 Bits

OSCLK	I20CD1	I20CD0	I2C operating frequency	Standard mode	Fast mode
4MHz(PLL oscillation)	0	0	4MHz	100kbps	400kbps
	0	1	2MHz	50kbps	200kbps
	1	0	1MHz	25kbps	100kbps
	1	1	Setting prohibited	-	-
2MHz(RC oscillation)	0	0	2MHz	50kbps	200kbps
	0	1	1MHz	25kbps	100kbps
	1	0	0.5MHz	12.5kbps	50kbps
	1	1	Setting prohibited	-	-

[Note]
- Do not change this bit during I^2C communication. Operation is not guaranteed if it is changed.
- The communication speed becomes 100 kbps/400 kbps when the operating frequency of I^2C is 4MHz. Set the operating frequency of I^2C in I20CD0 and I20CD1.

14.2.7 I²C Bus 0 Status Register (I2C0STAT)

Address: 0F74AH
Access: R
Access size: 16/8 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
I2C0STAL	-	-	-	-	-	I20ER	I20ACR	I20BB
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0STAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

[Description of Bits]

- **I20ER** (bit 2)
  The I20ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". The SDA pin output continues until the subsequent byte data communication terminates, even if the I20ER bit is set to "1".
  The I20ER bit is set to "0" when a write operation to I2C0CON is performed. The I20ER bit is set to "0" when the I20EN bit of I2C0MOD is set to "0".

I20ER	Description
0	No transmit error (initial value)
1	Transmit error

- **I20ACR** (bit 1)
  The I20ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I20ACR bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20ACR	Description
0	Receives acknowledgment "0" (initial value)
1	Receives acknowledgment "1"

- **I20BB** (bit 0)
  The I20BB bit is used to indicate the state of use of the I²C bus interface. When the start condition is generated on the I²C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". The I20BB bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20BB	Description
0	I²C bus-free state (initial value)
1	I²C bus-busy state

14.3 Description of Operation

14.3.1 Communication Operation Mode

Communication is started when communication mode is selected by using the I^2C bus 0 mode register (I2C0MOD), the I^2C function is enabled by using the I20EN bit, a slave address and a data communication direction are set in the I^2C bus 0 slave address register (I2C0SA), and "1" is written to the I20ST bit of the I^2C bus 0 control register (I2C0CON).

14.3.1.1 Start Condition

When "1" is written to the I20ST bit of the I^2C bus 0 control register (I2C0CON) while communication is stopped (the I2nST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to the slave address transmit mode.

14.3.1.2 Restart Condition

When "1" is written to the I20RS and I20ST bits of the I^2C bus 0 control register (I2C0CON) during communication (the I20ST bit is "0"), the restart condition waveform is output to the SDA and SCL pins.
After execution of the restart condition, the LSI shifts to the slave address transmit mode.

14.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I^2C bus 0 slave address register (I2C0SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I^2C bus 0 status register (I2C0STAT).
At completion of acknowledgment reception, the LSI shifts to the I^2C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0SA output from the SDA pin is stored in I2C0RD.

14.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C0TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I^2C bus 0 status register (I2C0STAT).
At completion of acknowledgment reception, the LSI shifts to the I^2C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0TD output from the SDA pin is stored in I2C0RD.

14.3.1.5 Data receive mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I20ACT bit of the I^2C bus 0 control register (I2C0CON) is output.
At completion of acknowledgment transmission, the LSI shifts to the I^2C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The data received is stored in I2C0RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I20ACR bit of the I^2C bus 0 status register (I2C0STAT).

14.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I^2C bus 0 interface interrupt (I2C0INT) is generated.
In the control register setting wait state, the transmit error flag (I20ER) of the I^2C bus 0 status register (I2C0STAT) and acknowledgment receive data (I20ACR) are confirmed and at data reception, the contents of I2C0RD are read in the CPU and the next operation mode is selected.
When "1" is written to the I20ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I20SP bit, the LSI shifts to the stop condition. When "1" is written to the I20RS bit, the operation shifts to the restart condition.

14.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I^2C bus n interface interrupt (I2C0INT) is generated.

14.3.2 Communication Operation Timing

Figures 14-2 to 14-4 show the operation timing and control method for each communication mode.

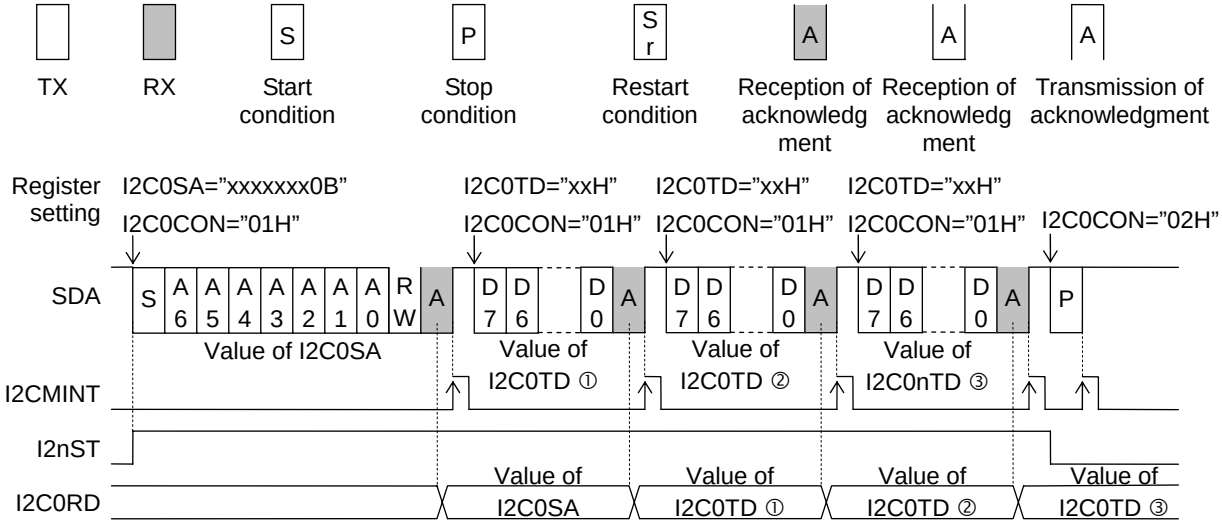


Figure 14-2 Operation Timing in Data Transmit Mode (Write)

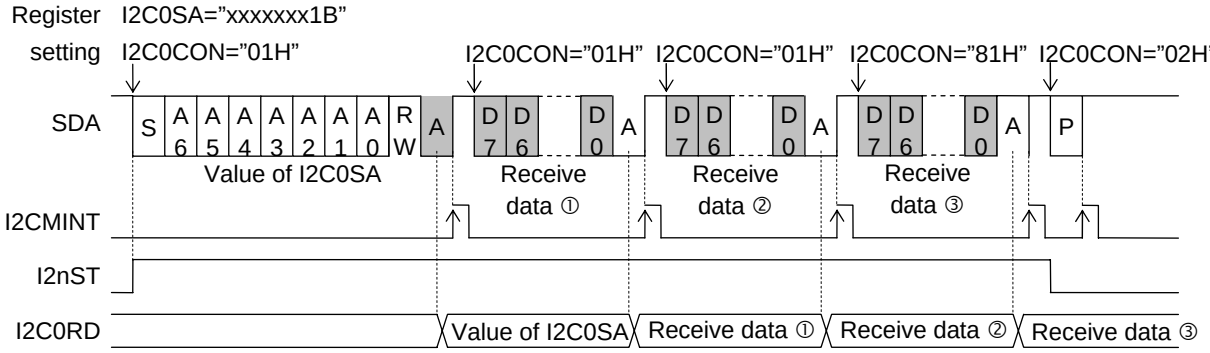


Figure 14-3 Operation Timing in Data Receive Mode (Read)

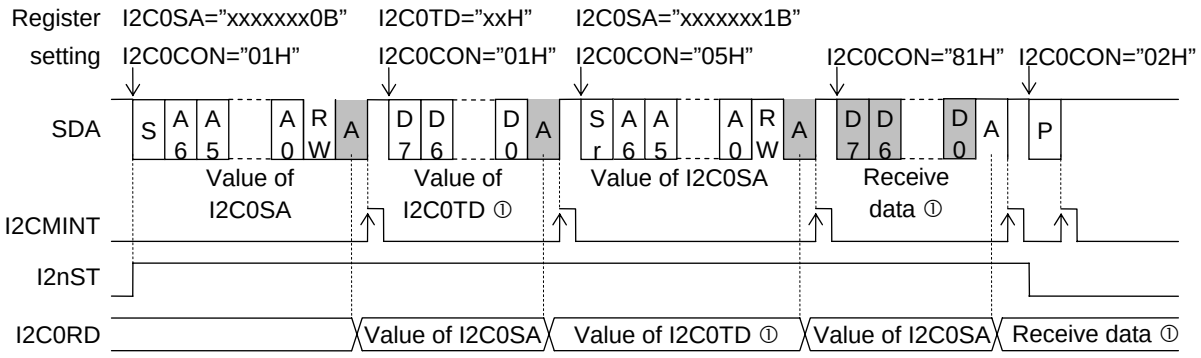


Figure 14-4 Operation Timing at Data Transmit/Receive Mode (Write/Read) Switching

Figure 14-5 shows the operation timing and control method when an acknowledgment error occurs.

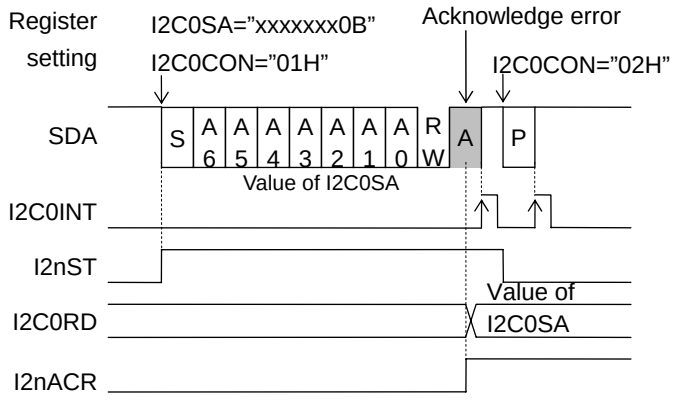


Figure 14-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide, the I2nER bit of the I^2C bus n status register (I2C0STAT) is set to “1” and the SDA pin output is disabled until termination of the subsequent byte data communication.
Figure 14-6 shows the operation timing and control method when transmission fails.

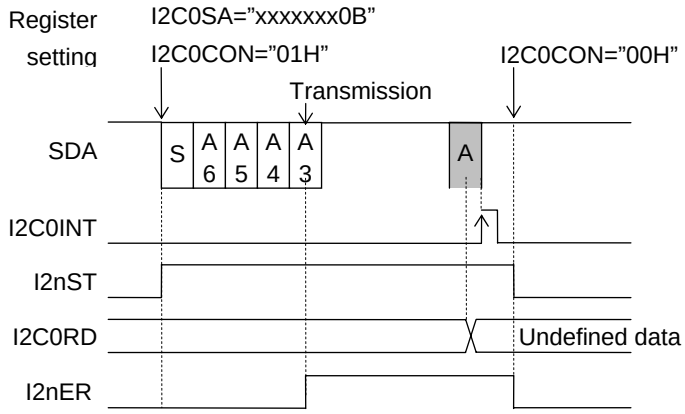


Figure 14-6 Operation Timing When Transmission Fails

14.3.3 Operation Waveforms

Figure 14-7 shows the operation waveforms of the SDA and SCL signals and the I2nBB flag. Table 15-2 shows the relationship between communication speeds and 1/m OSCLK clock counts.

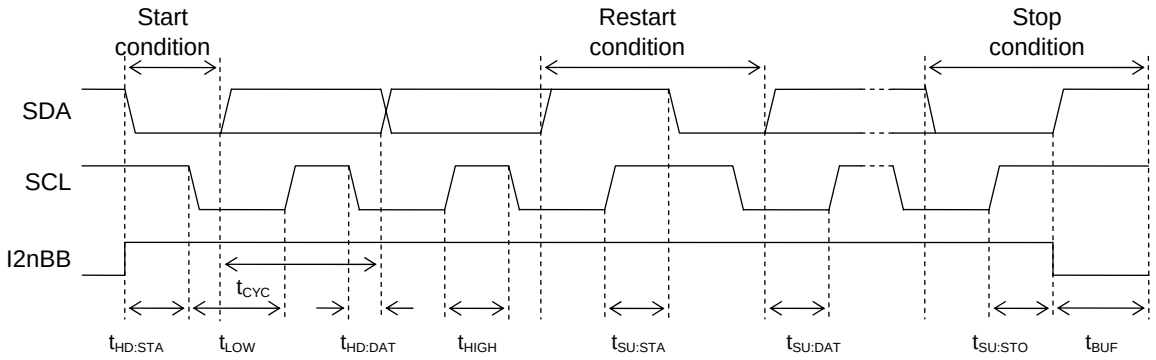


Figure 14-7 Operation Waveforms of SDA and SCL Signals and I2nBB Flag

Table 14-2 Relationship between Communication Speeds and OSCLK Clock Counts

Communication speed (I20SP)	Speed reduction (I2nDW1,0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100kbps	No reduction	40φ	18φ	22φ	4φ	18φ	22φ	18φ	18φ	22φ
	10% reduction	44φ	20φ	24φ	4φ	20φ	24φ	20φ	20φ	24φ
	20% reduction	48φ	22φ	26φ	4φ	22φ	26φ	22φ	22φ	26φ
	30% reduction	52φ	24φ	28φ	4φ	24φ	28φ	24φ	24φ	28φ
Fast mode 400kbps	No reduction	10φ	4φ	6φ	2φ	4φ	6φ	4φ	4φ	6φ
	10% reduction	11φ	4φ	7φ	2φ	4φ	7φ	5φ	4φ	7φ
	20% reduction	12φ	5φ	7φ	2φ	5φ	7φ	5φ	5φ	7φ
	30% reduction	13φ	5φ	8φ	2φ	5φ	8φ	6φ	5φ	8φ

φ: Clock cycle of 1/mOSCLK

m: Depends on the setting of the I20CD1 and I20CD0 bits of the I2C0MOD register.

[Note]

- The 1/m OSCLK clock count is set so that the communication speed may be set to 100 kbps/400 kbps when 1/m OSCLK is 4MHz.
- When using the clock cycle function (handshake function) that the slave device hold the SCL signal to “L” level, the period of “t_{CYC}” and “t_{LOW}“ get longer.

14.4 Specifying port registers

When you want to make sure the I2C bus interface function is working, please check related port registers are specified. See Chapter 19, “Port 4” , Chapter 20, “Port 5” and Chapter 21, “Port 6” for detail about the port registers.

14.4.1 Functioning P41(SCL) and P40(SDA) as the I2C

Set P41MD1-P40MD1 bits(bit1-bit0 of P4MOD1 register) to “0” and set P41MD0-P40MD0(bit1-bit0 of P4MOD0 register) to “1”, for specifying the I2C as the secondary function of P41 and P40.

Reg. name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	**1**	**0**
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	**P41MD1**	**P40MD1**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	**P41MD0**	**P40MD0**
Data	*	*	*	*	*	*	**1**	**1**

Set P41C1-P40C1 bit(bit1-0 of P4CON1 register) to “1”, set P41C0-P40C0 bit(bit1-0 of P4CON0 register) to “0”, and set P41DIR-P40DIR bit(bit1-0 of P4DIR register) to “0”, for specifying the P41 and P40 as Nch open-drain output. The open-drain/open-collector outputs are required on the I2C bus line to avoid collision between H level and L level.

Reg. name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	**P41C1**	**P40C1**
Data	*	*	*	*	*	*	**1**	**1**

Reg. name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	**P41C0**	**P40C0**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	**P41DIR**	**P40DIR**
Data	*	*	*	*	*	*	**0**	**0**

Data of P41D-P40D bits (bit1-0 of P4D register) do not affect to the I2C function, so don’t care the data for the function.

Reg. name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P47D	P46D	P45D	P44D	P43D	P42D	**P41D**	**P40D**
Data	*	*	*	*	*	*	******	******

* : Bit not related to the I2C bus interface function
** : Don’t care the data

Chapter 15 Port 0

15 Port 0

15.1 General Description

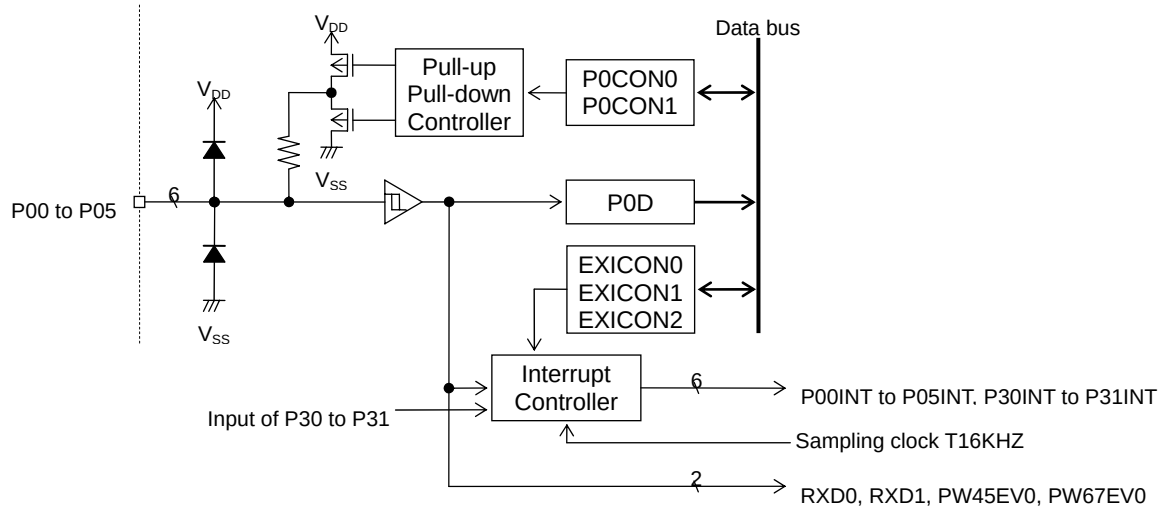
ML620Q151A/ML620Q152A/ML620Q153A includes a 5-bit input/output port, Port 0 (P00 to P04).
ML620Q154A/ML620Q155A/ML620Q156A includes a 6-bit input/output port, Port 0 (P00 to P05).
ML620Q157A/ML620Q158A/ML620Q159A includes a 6-bit input/output port, Port 0 (P00 to P05).
For details, see Section 1.3.2, "List of Pins".

15.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit. (Sampling frequency: T16KHZ)
- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- The P00 pin can be used as the PW45EV0 input pin for PWM.
- The P01 pin can be used as the PW67EV0 input pin for PWM.
- The P02 pin can be used as the RXD0 input pin for UART0.
- The P03 pin can be used as the RXD1 input pin for UART1.

15.1.2 Configuration

Figure 15-1 shows the configuration of Port 0.



P0D : Port 0 data register
P0CON0 : Port 0 control register 0
P0CON1 : Port 0 control register 1
EXICON0 : External interrupt control registers 0
EXICON1 : External interrupt control registers 1
EXICON2 : External interrupt control registers 2

Figure 15-1 Configuration of Port 0

15.1.3 List of Pins

Pin name	I/O	Function
P00/EXI0/ PW45EV0	I	Input port, External 0 interrupt, PW45EV0 input
P01/EXI1/ PW67EV0	I	Input port, External 1 interrupt, PW67EV0 input
P02/EXI2/ RXD0	I	Input port, External 2 interrupt, UART0 data input (RXD0)
P03/EXI3/ RXD1	I	Input port, External 3 interrupt, UART1 data input (RXD1)
P04/EXI4	I	Input port, External 4 interrupt
P05/EXI5	I	Input port, External 5 interrupt

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F20CH	Port 0 data register	P0D	-	R	8	Depends on pin state
0F20EH	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F20FH	Port 0 control register 1	P0CON1		R/W	8	00H
0F038H	External interrupt control registers 0	EXICON0	EXICON01	R/W	8	00H
0F039H	External interrupt control registers 1	EXICON1		R/W	8	00H
0F03AH	External interrupt control registers 2	EXICON2	-	R/W	8	00H

15.2.2 Port 0 Data Register (P0D)

Address: 0F20CH
Access: R
Access size: 8 bits
Initial value: Depends on pin state

	7	6	5	4	3	2	1	0
P0D	—	—	P05D	P04D	P03D	P02D	P01D	P00D
R	R	R	R	R	R	R	R	R
Initial value	0	0	x	x	x	x	x	x

P0D is a read-only special function register (SFR) used to read the pin level of Port 0.

Description of bits

- **P05D-P00D** (bits 5-0)
  The P05D to P00D bits are used to read the input level of the port 0 pin.

P05D	Description
0	P05 pin input: "L" level
1	P05 pin input: "H" level

P04D	Description
0	P04 pin input: "L" level
1	P04 pin input: "H" level

P03D	Description
0	P03 pin input: "L" level
1	P03 pin input: "H" level

P02D	Description
0	P02 pin input: "L" level
1	P02 pin input: "H" level

P01D	Description
0	P01 pin input: "L" level
1	P01 pin input: "H" level

P00D	Description
0	P00 pin input: "L" level
1	P00 pin input: "H" level

15.2.3 Port 0 Control Registers 0, 1 (P0CON0, P0CON1)

Address: 0F20EH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON0	—	—	P05C0	P04C0	P03C0	P02C0	P01C0	P00C0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F20FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	P05C1	P04C1	P03C1	P02C1	P01C1	P00C1
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0CON0 and P0CON1 are special function registers (SFRs) to select the input mode of Port 0.

Description of bits

- **P05C0-P00C0, P05C1-P00C1** (bits 5-0)
  The P05C0 to P00C0 bits and P05C1 to P00C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. The P0nC0 bit and the P0nC1 bit determine the input mode of P0n (Example: When P02C0 = "0" and P02C1 = "1", P02 is in input mode with a pull-up resistor).

P05C1 to P00C1	P05C0 to P00C0	Description
0	0	High-impedance input mode (initial value)
0	1	Input mode with a pull-down resistor
1	0	Input mode with a pull-up resistor
1	1	High-impedance input mode

15.2.4 External Interrupt Control Register 0, 1 (EXICON0, EXICON1)

Address: 0F038H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON0	P31E0	P30E0	P05E0	P04E0	P03E0	P02E0	P01E0	P00E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F039H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON1	P31E1	P30E1	P05E1	P04E1	P03E1	P02E1	P01E1	P00E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON0 and EXICON1 are special function registers (SFRs) to select an interrupt edge of Port 0.

Description of bits

- **P31E0-P30E0, P31E1-P30E1** (bits 5-0)
  The P31E0 to P30E0 bits and P31E1 to P30E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P3mE0 bit and the P3mE1 bit determine the interrupt mode of P3m (Example: When P30E0 = "0" and P30E1 = "1", P30 is in rising-edge interrupt mode).

P31E1 to P30E1	P31E0 to P30E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt
1	0	Rising-edge interrupt
1	1	Both-edge interrupt

- **P05E0-P00E0, P05E1-P00E1** (bits 5-0)
  The P05E0 to P00E0 bits and P05E1 to P00E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P0nE0 bit and the P0nE1 bit determine the interrupt mode of P0n (Example: When P02E0 = "0" and P02E1 = "1", P02 is in rising-edge interrupt mode).

P05E1 to P00E1	P05E0 to P00E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt
1	0	Rising-edge interrupt
1	1	Both-edge interrupt

15.2.5 External Interrupt Control Register 2 (EXICON2)

Address: 0F03AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON2	P31SM	P30SM	P05SM	P04SM	P03SM	P02SM	P01SM	P00SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON2 is a special function register (SFR) to select whether the Port 0 interrupt is with sampling or without sampling.

Description of bits

- **P31SM-P30SM** (bits 7-6)
  The P31SM to P30SM bits are used to select whether the Port 3 interrupt is with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P31SM	Description
0	Detects the input signal edge for P31 interrupt without sampling (initial value).
1	Detects with sampling

P30SM	Description
0	Detects the input signal edge for P30 interrupt without sampling (initial value).
1	Detects with sampling

- **P05SM-P00SM** (bits 5-0)
  The P05SM to P00SM bits are used to select whether the Port 0 interrupt is with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P05SM	Description
0	Detects the input signal edge for P05 interrupt without sampling (initial value).
1	Detects with sampling

P04SM	Description
0	Detects the input signal edge for P04 interrupt without sampling (initial value).
1	Detects with sampling

P03SM	Description
0	Detects the input signal edge for P03 interrupt without sampling (initial value).
1	Detects with sampling

P02SM	Description
0	Detects the input signal edge for P02 interrupt without sampling (initial value).
1	Detects with sampling

P01SM	Description
0	Detects the input signal edge for P01 interrupt without sampling (initial value).
1	Detects with sampling

P00SM	Description
0	Detects the input signal edge for P00 interrupt without sampling (initial value).
1	Detects with sampling

[Note]

- In STOP mode, no sampling is performed regardless of the value set in P31SM to P30SM and P05SM to P00SM since the sampling clock of 16 kHz stops.

15.3 Description of Operation

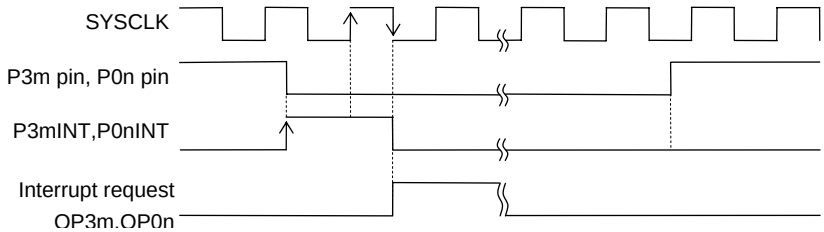
For the pins of Port 00 to 05, the setting of port 0 control registers 0, 1 (P0CON0, P0CON1) allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
High-impedance input mode is selected at system reset.
The pin level of Port 0 can be read by reading the Port 0 data register (P0D).

15.3.1 External Interrupt

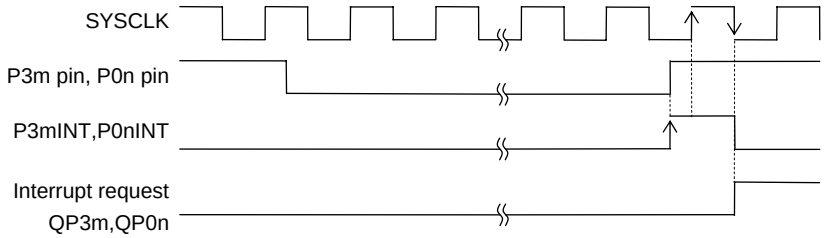
The Port 0 pins (P00, P01, P02, P03, P04, P05, P30, P31) can be used as P00 to P05 and P30 to P31 interrupts (P00INT to P05INT and P30INT to P31INT). The P00 to P05 and P30 to P31 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupt".
The P00 pin can be used as PW45EV0 input pin of PWM, the P01 pin as PW67EV0 input pin of PWM, the P02 pin as RXD0 input of UART0, and the P03 pin as RXD1 input of UART1.
See Chapter 11, "PWM" for PWM function, Chapter 13, "UART" for UART function, and Chapter 8, "8-bit Timer" for timer function.

15.3.2 Interrupt Request

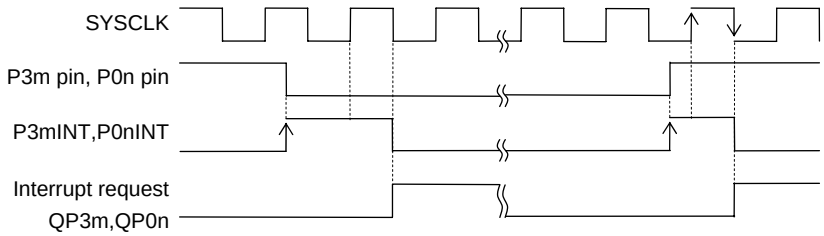
When an interrupt edge selected with the external interrupt control register 0, 1, or 2 (EXICON0, EXICON1, or EXICON2) occurs at a Port 0 or 3 pin, any of the maskable P00 to P05 and P30 to P31 interrupts (P00INT to P05INT, P30INT to P31INT) occurs.
Figure 15-2 shows the generation timing of P00 to P05 and P30 to P31 interrupts in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



(a) When Falling-Edge Interrupt Mode without Sampling is Selected

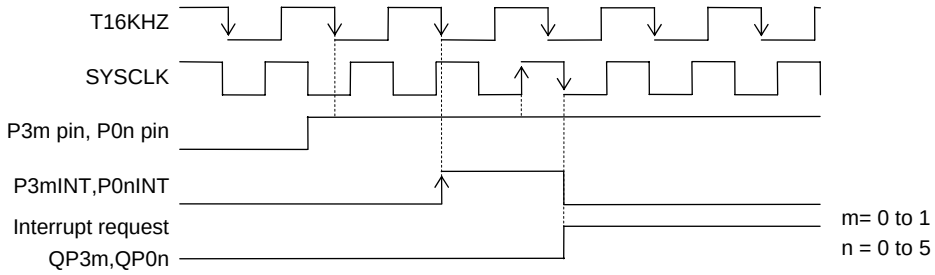


(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected

When rising-edge interrupt mode with sampling is selected, the input level of P0n and P3m pins is checked at falling edges of T16KHz. If it is "H" twice consecutively, the interrupt condition is satisfied, and an interrupt request occurs at the timing of falling edge of SYSCLK after the second falling edge of T16KHz.



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 15-2 P00 to P05 and P30 to P31 Interrupt Generation Timing

Chapter 16 Port 1

16 Port 1

16.1 General Description

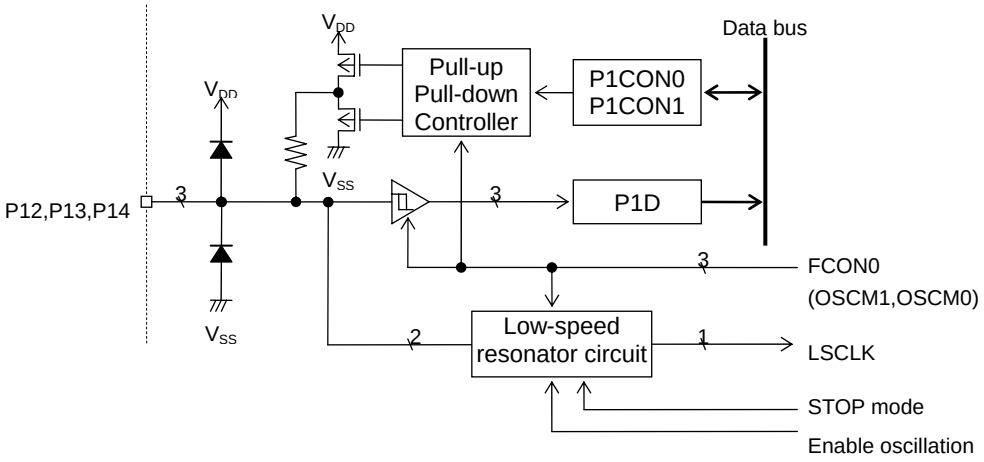
This LSI includes a 3-bit input port, Port 1 (P12, P13, P14).
Port 1 can have a low-speed crystal oscillation pin (32.768 kHz) as a secondary function. To use it as a low-speed crystal oscillation pin, it can be selected in Code-Option.
For Code-Option, see Chapter 30, "Code-Option".

16.1.1 Features

- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- Allows selection of a crystal oscillation pin as secondary function.

16.1.2 Configuration

Figure 16-1 shows the configuration of Port 1.



P1D : Port 1 data register
P1CON0 : Port 1 control register 0
P1CON1 : Port 1 control register 1

Figure 16-1 Configuration of Port 1

16.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P12/XT0	I	Input port	Pin for connecting a crystal for low-speed clock
P13/XT1	I/O	I/O port	Pin for connecting a crystal for low-speed clock
P14/TEST0	I *	Input port/ Test input pin	-

*: The output setting for P14 is prohibited.
[Note]
Do not program ML620Q150A series with an application program code that sets P14IDR bit of P1DIR register to"0". Because the program code is executed before µEASE accesses to ML620Q150A series, P14/TEST0 pin gets output mode and from then on, the LSI cannot enter the on-chip debug mode. Notice that µEASE cannot initialize the P14DIR bit.

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F21AH	Port 1 data register	P1D	-	R	8	Depends on pin state
0F21BH	Port 1 direction register	P1DIR	-	R/W	8	10H
0F21CH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	10H
0F21DH	Port 1 control register 1	P1CON1		R/W	8	00H

16.2.2 Port 1 Data Register (P1D)

Address: 0F21AH
Access: R/W
Access size: 8 bits
Initial value: Depends on pin state

	7	6	5	4	3	2	1	0
P1D	—	—	—	P14D	P13D	P12D	—	—
R/W	R	R	R	R/W	R/W	R	R	R
Initial value	0	0	0	x	x	x	0	0

P1D is a read-only special function register (SFR) used to read the input level of the port 1 pin.

Description of bits

- **P14D, P13D, P12D** (bits 4-2)
  The P14D, P13D, and P12D bits are used to read the input level of the Port 1 pin.

P14D	Description
0	Input level of the P14 pin: "L"
1	Input level of the P14 pin: "H"

P13D	Description
0	Input level of the P13 pin: "L"
1	Input level of the P13 pin: "H"

P12D	Description
0	Input level of the P12 pin: "L"
1	Input level of the P12 pin: "H"

16.2.3 Port 1 Direction Register (P1DIR)

Address: 0F21BH
Access: R/W
Access size: 8 bits
Initial value: 18H

	7	6	5	4	3	2	1	0
P1DIR	—	—	—	P14DIR	P13DIR	—	—	—
R/W	R	R	R	R/W	R/W	R	R	R
Initial value	0	0	0	1	0	0	0	0

P1DIR is a special function register (SFR) to select the input/output mode of Port 1 (P14).
The P12 pin is an input-only port, and the P13 pin is an I/O port.

Description of bits

- **P14DIR** (bit 4)
  The P14DIR bit is used to set the input/output direction of the Port 14 pins.

P14DIR	Description
0	**(Setting prohibited)** P14 pin: Output
1	P14 pin: Input (initial value)

- **P13DIR** (bit 3)
  The P13DIR bit is used to set the input/output direction of the Port 13 pins.

P13DIR	Description
0	P13 pin: Output (initial value)
1	P13 pin: Input

[Note]
Do not program ML620Q150A series with an application program code that sets P14IDR bit of P1DIR register to"0". Because the program code is executed before µEASE accesses to ML620Q150A series, P14/TEST0 pin gets output mode and from then on, the LSI cannot enter the on-chip debug mode. Notice that µEASE cannot initialize the P14DIR bit.

16.2.4 Port 1 Control Registers 0, 1 (P1CON0, P1CON1)

Address: 0F21CH
Access: R/W
Access size: 8/16 bit
Initial value: 10H

	7	6	5	4	3	2	1	0
P1CON0	—	—	—	P14C0	P13C0	P12C0	—	—
R/W	R	R	R	R/W	R/W	R/W	R	R
Initial value	0	0	0	1	0	0	0	0

Address: 0F21DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	P14C1	P13C1	P12C1	—	—
R/W	R	R	R	R/W	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

P1CON0 and P1CON1 are special function registers (SFRs) used to select the input/output mode of Port 1.

Description of bits

- **P14C0-P12C0, P14C1-P12C1** (bits 4-2)
  The P14C0 to P12C0 bits and P14C1 to P12C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.

		When output mode is selected (P14DIR bit = "0") *** The output setting is prohibited.**	When input mode is selected (P14DIR bit = "1")
P14C1	**P14C0**	Description	
0	0	P14 pin: High-impedance output	P14 pin: High-impedance input
0	1	P14 pin: P-channel open drain output	P14 pin: Input with a pull-down resistor (initial value)
1	0	P14 pin: N-channel open drain output	P14 pin: Input with a pull-up resistor
1	1	P14 pin: CMOS output	P14 pin: High-impedance input

		When output mode is selected (P13DIR bit = "0")	When input mode is selected (P13DIR bit = "1")
P13C1	**P13C0**	Description	
0	0	P13 pin: High-impedance output (initial value)	P13 pin: High-impedance input
0	1	P13 pin: P-channel open drain output	P13 pin: Input with a pull-down resistor
1	0	P13 pin: N-channel open drain output	P13 pin: Input with a pull-up resistor
1	1	P13 pin: CMOS output	P13 pin: High-impedance input

P12C1	**P12C0**	Description
0	0	P12 pin: High-impedance input (initial value)
0	1	P12 pin: Input with a pull-down resistor
1	0	P12 pin: Input with a pull-up resistor
1	1	P12 pin: High-impedance input

[Note]

• Do not program ML620Q150A series with an application program code that sets P14IDR bit of P1DIR register to”0”. Because the program code is executed before µEASE accesses to ML620Q150A series, P14/TEST0 pin gets output mode and from then on, the LSI cannot enter the on-chip debug mode. Notice that µEASE cannot initialize the P14DIR bit.

• If a crystal oscillation pin is selected in Code-Option, the P12 and P13 pins are automatically set to the high-impedance input mode.

16.3 Description of Operation

16.3.1 Input Port Function

For each pin of Port 1, one of high-impedance input mode, input mode with a pull-down resistor, and input mode with a pull-up resistor can be selected by setting the Port 1 control registers 0, 1 (P1CON0, P1CON1). At a system reset, high-impedance input mode is selected as the initial status.
The input level of the Port 1 pin can be read by reading the Port 1 data register (P1D).

Chapter 17 Port 2

17 Port 2

17.1 General Description

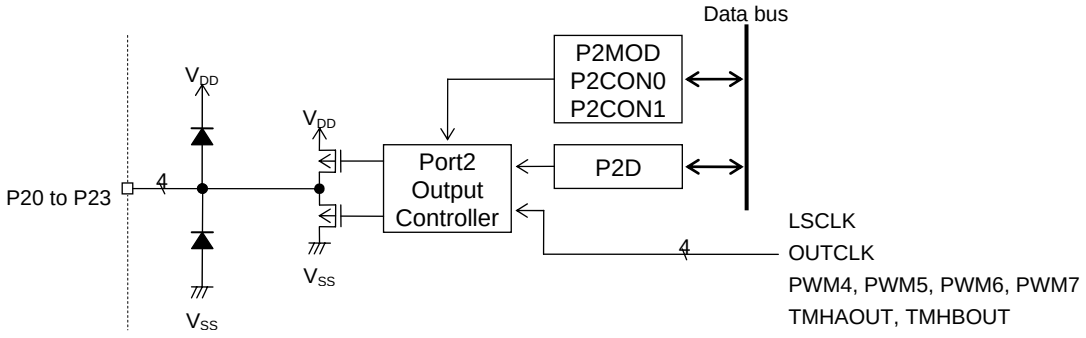
This LSI includes a 4-bit output-only port, Port 2 (P20 to P23).
Port 2 can output the low-speed clock (LSCLK) and high-speed clock (OUTCLK) as the secondary function, the PWM4 output (PWM4), PWM5 output (PWM5), timer A out (TMHAOUT), and timer B out (TMHBOUT) as the tertiary function, and the PWM6 output (PWM6) and PWM7 output (PWM7) as the quartic function. See Chapter 6, "Clock Generation Circuit" for the clock output, Chapter 11, "PWM" for the PWM output, and Chapter 9, "16-bit Timer" for the timer out.

17.1.1 Features

- Allows direct LED drive.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit.
- The low-speed clock (LSCLK) and high-speed clock (OUTCLK) can be output as the secondary function, the PWM4 output (PWM4), PWM5 output (PWM5), timer A out (TMHAOUT), and timer B out (TMHBOUT) as the tertiary function, and the PWM6 output (PWM6) and PWM7 output (PWM7) as the quartic function.
- Enters the LED drive mode when the general-purpose output port function is selected.

17.1.2 Configuration

Figure 17-1 shows the configuration of Port 2.



P2D : Port 2 data register
P2CON0 : Port 2 control register 0
P2CON1 : Port 2 control register 1
P2MOD : Port 2 mode register

Figure 17-1 Configuration of Port 2

17.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P20/LED0/ LSCLK/PWM4	O	Output port, Direct LED drive	Low-speed clock output (LSCLK)	PWM4 output (PWM4)	-
P21/LED1/ OUTCLK/PWM5	O	Output port, Direct LED drive	High-speed clock output (OUTCLK)	PWM5 output (PWM5)	-
P22/LED2/ TMHAOUT/PWM6	O	Output port, Direct LED drive	-	Timer A out (TMHAOUT)	PWM6 output (PWM6)
P23/LED3/ TMHBOUT/PWM7	O	Output port, Direct LED drive	-	Timer B out (TMHBOUT)	PWM7 output (PWM7)

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F228H	Port 2 data register	P2D	-	R/W	8	00H
0F22AH	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F22BH	Port 2 control register 1	P2CON1		R/W	8	00H
0F22CH	Port 2 mode register 0	P2MOD0	P2MOD	R/W	8/16	00H
0F22DH	Port 2 mode register 1	P2MOD1		R/W	8	00H

17.2.2 Port 2 Data Register (P2D)

Address: 0F228H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	—	—	—	—	P23D	P22D	P21D	P20D
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the output value of the Port 2. The value of this register is output to the Port 2 pin. The value written to P2D is readable.

Description of bits

- **P23D-P20D** (bits 3-0)
  The P23D to P20D bits are used to set the output value of the Port 2 pin.

P23D	Description
0	Output level of the P23 pin: "L"
1	Output level of the P23 pin: "H"

P22D	Description
0	Output level of the P22 pin: "L"
1	Output level of the P22 pin: "H"

P21D	Description
0	Output level of the P21 pin: "L"
1	Output level of the P21 pin: "H"

P20D	Description
0	Output level of the P20 pin: "L"
1	Output level of the P20 pin: "H"

17.2.3 Port 2 Control Registers 0, 1 (P2CON0, P2CON1)

Address: 0F22AH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON0	—	—	—	—	P23C0	P22C0	P21C0	P20C0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON1	—	—	—	—	P23C1	P22C1	P21C1	P20C1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select the output state of the output pin Port 2.

Description of bits

- **P23C0-P20C0, P23C1-P20C1** (bits 3-0)
  The P23C0 to P20C0 and P23C1 to P20C1 bits are used to select high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode.
  To directly drive LEDs, select N-channel open drain output mode.

P23C1	P23C0	Description
0	0	P23 pin: High-impedance output (initial value)
0	1	P23 pin: P-channel open drain output
1	0	P23 pin: N-channel open drain output
1	1	P23 pin: CMOS output

P22C1	P22C0	Description
0	0	P22 pin: High-impedance output (initial value)
0	1	P22 pin: P-channel open drain output
1	0	P22 pin: N-channel open drain output
1	1	P22 pin: In CMOS output mode

P21C1	P21C0	Description
0	0	P21 pin: High-impedance output (initial value)
0	1	P21 pin: P-channel open drain output
1	0	P21 pin: N-channel open drain output
1	1	P21 pin: In CMOS output mode

P20C1	P20C0	Description
0	0	P20 pin: High-impedance output (initial value)
0	1	P20 pin: P-channel open drain output
1	0	P20 pin: N-channel open drain output
1	1	P20 pin: In CMOS output mode

17.2.4 Port 2 Mode Register (P2MOD)

Address: 0F22CH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD0	—	—	—	—	P23MD0	P22MD0	P21MD0	P20MD0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD1	—	—	—	—	P23MD1	P22MD1	P21MD1	P20MD1
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2MOD0 and P2MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of Port 2.

Description of bits

- **P23MD0, P23MD1** (bit 3)
  The P23MD0 and P23MD1 bits are used to select the primary, secondary, tertiary, or quartic function of the P23 pin.

P23MD1	P23MD0	Description
0	0	General-purpose output port function/LED drive mode (initial value)
0	1	Do not use
1	0	Timer B out output function (TMHBOUT)
1	1	PWM7 output (PWM7)

- **P22MD0, P22MD1** (bit 2)
  The P22MD0 and P22MD1 bits are used to select the primary, secondary, tertiary, or quartic function of the P22 pin.

P22MD1	P22MD0	Description
0	0	General-purpose output port function/LED drive mode (initial value)
0	1	Do not use
1	0	Timer A out output function (TMHAOUT)
1	1	PWM output (PWM6)

- **P21MD0, P21MD1** (bit 1)
  The P21MD0 and P21MD1 bits are used to select the primary, secondary, or tertiary function of the P21 pin.

P21MD1	P21MD0	Description
0	0	General-purpose output port function/LED drive mode (initial value)
0	1	High-speed clock output function (OUTCLK)
1	0	PWM5 output (PWM5)
1	1	Do not use

- **P20MD0, P20MD1** (bit 0)
  The P20MD0 and P20MD1 bits are used to select the primary, secondary, or tertiary function of the P20 pin.

P20MD1	P20MD0	Description
0	0	General-purpose output port function/LED drive mode (initial value)
0	1	Low-speed clock (LSCLK) output function
1	0	PWM4 output (PWM4)
1	1	Do not use

[Note]
P2 (Port 2) is an output-only pin and does not have the register to select the data direction (input or output).

17.3 Description of Operation

17.3.1 Output Port Function

For each pin of Port 2, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 2 control registers 0, 1 (P2CON0, P2CON1). At a system reset, high-impedance output mode is selected as the initial status.
Depending of the value set in the Port 2 data register (P2D), a “L” level or “H” level signal is output to each pin of Port 2.

17.3.2 Secondary, Tertiary, and Quartic Functions

The low-speed clock (LSCLK), high-speed clock (OUTCLK) output, PWM4 output (PWM4), PWM5 output (PWM5), PWM6 output (PWM6), PWM7 output (PWM7), timer A out (TMHAOUT), and timer B out (TMHBOUT) are assigned to Port 2 as the secondary, tertiary, and quartic functions. The secondary, tertiary, or quartic function can be used by setting the P23MD to P20MD and P23MD1 to P20MD1 bits of the Port 2 mode register (P2MOD, P2MOD1) to "1".

Chapter 18 Port 3

18 Port 3

18.1 General Description

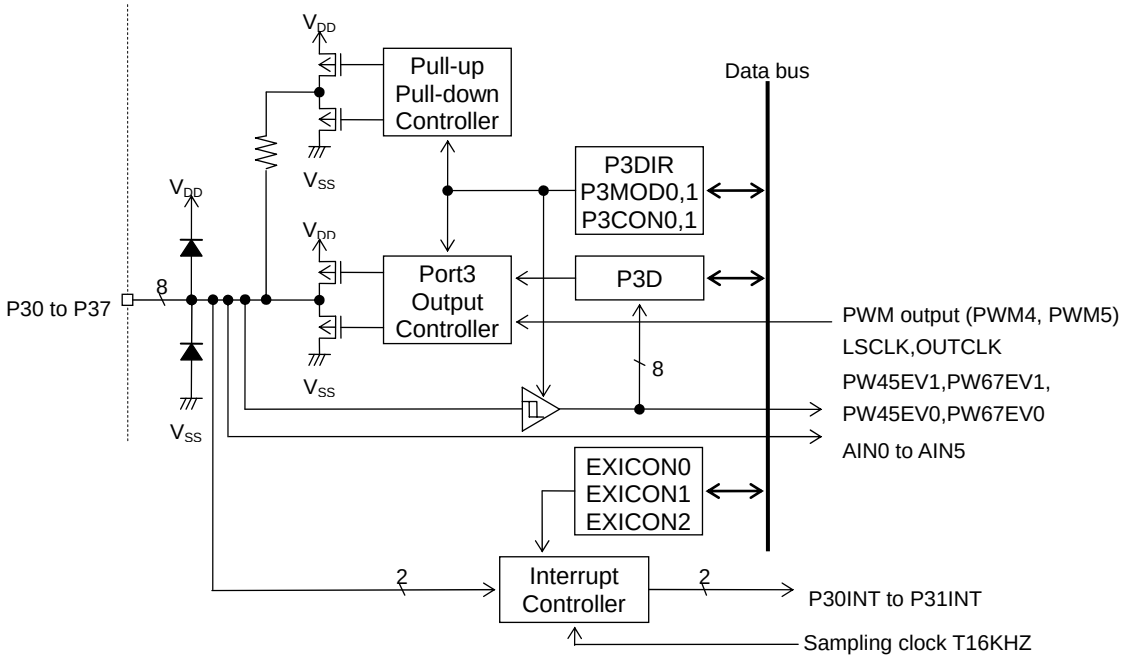
ML620Q151A/ML620Q152A/ML620Q153A includes a 6-bit input/output port, Port 3 (P30 to P35).
ML620Q154A/ML620Q155A/ML620Q156A includes a 7-bit input/output port, Port 3 (P30 to P36).
ML620Q157A/ML620Q158A/ML620Q159A includes a 8-bit input/output port, port 3 (P30 to P37).
For details, see Section 1.3.2, "List of Pins".
It also can output the PWM output (PWM4, PWM5), low-speed clock (LSCLK), and high-speed clock (OUTCLK) in the secondary and tertiary function modes. See Chapter 11, "PWM" for the PWM output and Chapter 6, "Clock Generation Circuit" for the clock output.

18.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Allows the low-speed clock (LSCLK) output and high-speed clock (OUTCLK) output as the secondary function, and the PWM output (PWM4, PWM5) as the tertiary function.
- The P30 pin can be used as the PW45EV1 input pin for PWM4 and PWM5.
- The P31 pin can be used as the PW67EV1 input pin for PWM6 and PWM7.
- The P32 pin can be used as the PW45EV0 input pin for PWM4 and PWM5.
- The P33 pin can be used as the PW67EV0 input pin for PWM6 and PWM7.
- The P30 to P35 pins can be used as an analog input pin of the successive approximation type ADC.
- Allows selection of with/without interrupt sampling for P30 to P31.(Sampling frequency: T16KHZ)

18.1.2 Configuration

Figure 18-1 shows the configuration of Port 3.



P3D : Port 3 data register
P3DIR : Port 3 direction register
P3CON0 : Port 3 control register 0
P3CON1 : Port 3 control register 1
P3MOD0 : Port 3 mode register 0
P3MOD1 : Port 3 mode register 1
EXICON0 : External interrupt control registers 0
EXICON1 : External interrupt control registers 1
EXICON2 : External interrupt control registers 2

Figure 18-1 Configuration of Port 3

[Note]
P30 to P35 are assigned to the successive approximation type ADC input. To use them as the analog input of successive approximation type ADC, set the appropriate port to the high-impedance output mode.

18.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P30/EXI6 PW45EV1/ AIN0	I/O	I/O port, External 6 interrupt PW45EV1 input, Successive approximation type ADC input	-	-
P31/EXI7 PW67EV1/ AIN1	I/O	I/O port, External 7 interrupt PW67EV1 input, Successive approximation type ADC input	-	-
P32/PW45EV0 AIN2	I/O	I/O port, PW45EV0 input Successive approximation type ADC input	-	-
P33/PW67EV0 AIN3	I/O	I/O port, PW67EV0 input Successive approximation type ADC input	-	-
P34/ AIN4/ PWM4	I/O	I/O port, Successive approximation type ADC input	-	PWM output (PWM4)
P35/ AIN5/ PWM5	I/O	I/O port, Successive approximation type ADC input	-	PWM output (PWM5)
P36/ LSCLK	I/O	I/O port	Low-speed clock output (LSCLK)	-
P37/ OUTCLK	I/O	I/O port	High-speed clock output (OUTCLK)	-

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F236H	Port 3 data register	P3D	-	R/W	8	00H
0F237H	Port 3 direction register	P3DIR	-	R/W	8	00H
0F238H	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F239H	Port 3 control register 1	P3CON1		R/W	8	00H
0F23AH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F23BH	Port 3 mode register 1	P3MOD1		R/W	8	00H

18.2.2 Port 3 Data Register (P3D)

Address: 0F236H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3D	P37D	P36D	P35D	P34D	P33D	P32D	P31D	P30D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3D is a special function register (SFR) to set the value to be output to the Port 3 pin or to read the input level of the Port 3. In output mode, the value of this register is output to the Port 3 pin. The value written to P3D is readable.
In input mode, the input level of the Port 3 pin is read when P3D is read. Output mode or input mode is selected by using the port mode register (P3DIR) described later.

Description of bits

- **P37D-P30D** (bits 7-0)
  The P37D to P30D bits are used to set the output value of the Port 3 pin in output mode and to read the pin level of the Port 3 pin in input mode.

P37D	Description
0	Output or input level of the P37 pin: "L"
1	Output or input level of the P37 pin: "H"

P36D	Description
0	Output or input level of the P36 pin: "L"
1	Output or input level of the P36 pin: "H"

P35D	Description
0	Output or input level of the P35 pin: "L"
1	Output or input level of the P35 pin: "H"

P34D	Description
0	Output or input level of the P34 pin: "L"
1	Output or input level of the P34 pin: "H"

P33D	Description
0	Output or input level of the P33 pin: "L"
1	Output or input level of the P33 pin: "H"

P32D	Description
0	Output or input level of the P32 pin: "L"
1	Output or input level of the P32 pin: "H"

P31D	Description
0	Output or input level of the P31 pin: "L"
1	Output or input level of the P31 pin: "H"

P30D	Description
0	Output or input level of the P30 pin: "L"
1	Output or input level of the P30 pin: "H"

18.2.3 Port 3 Direction Register (P3DIR)

Address: 0F237H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3DIR	P37DIR	P36DIR	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

Description of bits

- **P37DIR-P30DIR** (bits 7-0)
  The P37DIR to P30DIR bits are used to set the input/output direction of the Port 3 pins.

P37DIR	Description
0	P37 pin: Output (initial value)
1	P37 pin: Input

P36DIR	Description
0	P36 pin: Output (initial value)
1	P36 pin: Input

P35DIR	Description
0	P35 pin: Output (initial value)
1	P35 pin: Input

P34DIR	Description
0	P34 pin: Output (initial value)
1	P34 pin: Input

P33DIR	Description
0	P33 pin: Output (initial value)
1	P33 pin: Input

P32DIR	Description
0	P32 pin: Output (initial value)
1	P32 pin: Input

P31DIR	Description
0	P31 pin: Output (initial value)
1	P31 pin: Input

P30DIR	Description
0	P30 pin: Output (initial value)
1	P30 pin: Input

18.2.4 Port 3 Control Registers 0, 1 (P3CON0, P3CON1)

Address: 0F238H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON0	P37C0	P36C0	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F239H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON1	P37C1	P36C1	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3CON0 and P3CON1 are special function registers (SFRs) used to select the input/output state of the Port 3 pin. The output state is different between input mode and output mode. Input or output is selected by using the P3DIR register.

Description of bits

- **P37C1-P30C1, P37C0-P30C0** (bits 7-0)
  The P37C1 to P30C1 and P37C0 to P30C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

		When output mode is selected (P37DIR bit = "0")	When input mode is selected (P37DIR bit = "1")
P37C1	**P37C0**	Description	
0	0	P37 pin: High-impedance output (initial value)	P37 pin: High-impedance input
0	1	P37 pin: P-channel open drain output	P37 pin: Input with a pull-down resistor
1	0	P37 pin: N-channel open drain output	P37 pin: Input with a pull-up resistor
1	1	P37 pin: CMOS output	P37 pin: High-impedance input

		When output mode is selected (P36DIR bit = "0")	When input mode is selected (P36DIR bit = "1")
P36C1	**P36C0**	Description	
0	0	P36 pin: High-impedance output (initial value)	P36 pin: High-impedance input
0	1	P36 pin: P-channel open drain output	P36 pin: Input with a pull-down resistor
1	0	P36 pin: N-channel open drain output	P36 pin: Input with a pull-up resistor
1	1	P36 pin: CMOS output	P36 pin: High-impedance input

		When output mode is selected (P35DIR bit = "0")	When input mode is selected (P35DIR bit = "1")
P35C1	**P35C0**	Description	
0	0	P35 pin: High-impedance output (initial value)	P35 pin: High-impedance input
0	1	P35 pin: P-channel open drain output	P35 pin: Input with a pull-down resistor
1	0	P35 pin: N-channel open drain output	P35 pin: Input with a pull-up resistor
1	1	P35 pin: CMOS output	P35 pin: High-impedance input

		When output mode is selected (P34DIR bit = "0")	When input mode is selected (P34DIR bit = "1")
P34C1	**P34C0**	Description	
0	0	P34 pin: High-impedance output (initial value)	P34 pin: High-impedance input
0	1	P34 pin: P-channel open drain output	P34 pin: Input with a pull-down resistor
1	0	P34 pin: N-channel open drain output	P34 pin: Input with a pull-up resistor
1	1	P34 pin: CMOS output	P34 pin: High-impedance input

		When output mode is selected (P33DIR bit = "0")	When input mode is selected (P33DIR bit = "1")
P33C1	**P33C0**	Description	
0	0	P33 pin: High-impedance output (initial value)	P33 pin: High-impedance input
0	1	P33 pin: P-channel open drain output	P33 pin: Input with a pull-down resistor
1	0	P33 pin: N-channel open drain output	P33 pin: Input with a pull-up resistor
1	1	P33 pin: CMOS output	P33 pin: High-impedance input

		When output mode is selected (P32DIR bit = "0")	When input mode is selected (P32DIR bit = "1")
P32C1	**P32C0**	Description	
0	0	P32 pin: High-impedance output (initial value)	P32 pin: High-impedance input
0	1	P32 pin: P-channel open drain output	P32 pin: Input with a pull-down resistor
1	0	P32 pin: N-channel open drain output	P32 pin: Input with a pull-up resistor
1	1	P32 pin: CMOS output	P32 pin: High-impedance input

		When output mode is selected (P31DIR bit = "0")	When input mode is selected (P31DIR bit = "1")
P31C1	**P31C0**	Description	
0	0	P31 pin: High-impedance output (initial value)	P31 pin: High-impedance input
0	1	P31 pin: P-channel open drain output	P31 pin: Input with a pull-down resistor
1	0	P31 pin: N-channel open drain output	P31 pin: Input with a pull-up resistor
1	1	P31 pin: CMOS output	P31 pin: High-impedance input

		When output mode is selected (P30DIR bit = "0")	When input mode is selected (P30DIR bit = "1")
P30C1	**P30C0**	Description	
0	0	P30 pin: High-impedance output (initial value)	P30 pin: High-impedance input
0	1	P30 pin: P-channel open drain output	P30 pin: Input with a pull-down resistor
1	0	P30 pin: N-channel open drain output	P30 pin: Input with a pull-up resistor
1	1	P30 pin: CMOS output	P30 pin: High-impedance input

18.2.5 Port 3 Mode Registers 0, 1 (P3MOD0, P3MOD1)

Address: 0F23AH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD0	P37MD0	P36MD0	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F23BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD1	P37MD1	P36MD1	P35MD1	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3MOD0 and P3MOD1 are special function registers (SFRs) used to select the primary, secondary, or tertiary function of the Port 3.

Description of bits

- **P37MD1, P37MD0** (bit 7)
  The P37MD1 and P37MD0 bits are used to select the primary or secondary function of the P37 pin.

P37MD1	P37MD0	Description
0	0	General-purpose output port function (initial value)
0	1	High-speed clock (OUTCLK) output function
1	0	Do not use
1	1	Do not use

- **P36MD1, P36MD0** (bit 6)
  The P36MD1 and P36MD0 bits are used to select the primary or secondary function of the P36 pin.

P36MD1	P36MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Low-speed clock (LSCLK) output function
1	0	Do not use
1	1	Do not use

- **P35MD1, P35MD0** (bit 5)
  The P35MD1 and P35MD0 bits are used to select the primary or tertiary function of the P35 pin.

P35MD1	P35MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	PWM5 output pin (PWM5)
1	1	Do not use

- **P34MD1, P34MD0** (bits 4)
  The P34MD1 and P34MD0 bits are used to select the primary or tertiary function of the P34 pin.

P34MD1	P34MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	PWM4 output pin (PWM4)
1	1	Do not use

- **P33MD1, P33MD0** (bit 3)
  The P33MD1 and P33MD0 bits are used to select the primary, secondary, or tertiary function of the P33 pin.

P33MD1	P33MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	Do not use
1	1	Do not use

- **P32MD1, P32MD0** (bit 2)
  The P32MD1 and P32MD0 bits are used to select the primary function of the P32 pin.

P32MD1	P32MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	Do not use
1	1	Do not use

- **P31MD1, P31MD0** (bit 1)
  The P31MD1 and P31MD0 bits are used to select the primary function of the P31 pin.

P31MD1	P31MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	Do not use
1	1	Do not use

- **P30MD1, P30MD0** (bit 0)
  The P30MD1 and P30MD0 bits are used to select the primary function of the P30 pin.

P30MD1	P30MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	Do not use
1	1	Do not use

[Note]
When the pin is set to "Do not use" and the output mode is selected (by the Port 3 control register), the Port 3 output pin state is fixed as follows regardless of the data of the port data register P3D:
When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

18.3 Description of Operation

18.3.1 Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers 0, 1 (P3CON0, P3CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 3 control registers 0, 1 (P3CON0, P3CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

18.3.2 Secondary and Tertiary Functions

The PWM output (PWM4, PWM5), low-speed clock (LSCLK) output, and high-speed clock (OUTCLK) output are assigned to Port 3 as the secondary and tertiary functions. These pins can be used in the secondary or tertiary function mode by setting the P37MD0 to P30MD0 and P37MD1 to P30MD1 bits of the Port 3 mode registers (P3MOD0, P3MOD1).

[Note]
P30 to P35 are assigned to the successive approximation type ADC input. To use them as the analog input of successive approximation type ADC, set the appropriate port to the high-impedance output mode.

18.3.3 External Interrupt

The Port 3 pins (P30, P31) can be used as P30 to P31 interrupts (P30INT to P31INT). The P30 to P31 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupt".

18.3.4 Interrupt Request

When an interrupt edge selected with the external interrupt control register 0, 1, or 2 (EXICON0, EXICON1, or EXICON2) occurs at a Port 3 pin (P30, P31), any of the maskable P30 to P31 interrupts (P30INT to P31INT) occurs. For the external interrupt control registers 0, 1, and 2 (EXICON0, EXICON1, EXICON2) and the interrupt generation timing, see Chapter 15, "Port 0".

Chapter 19 Port 4

19 Port 4

19.1 General Description

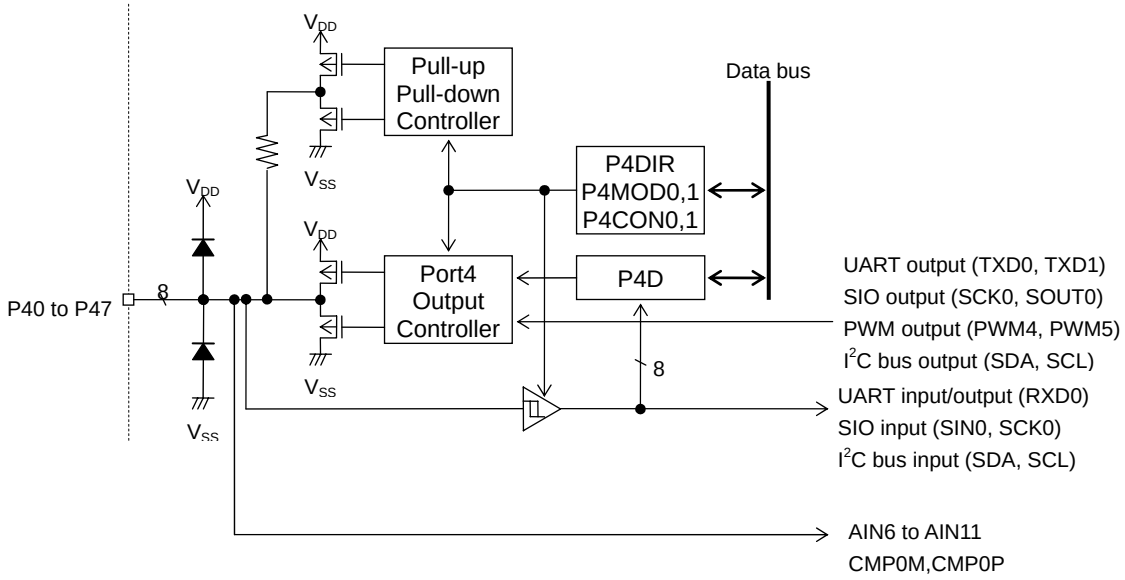
This LSI includes a 8-bit input/output port, Port 4 (P40 to P47).
Port 4 can have the PWM output, UART, synchronous serial port, and I^2C bus functions as the secondary, tertiary, or quartic function.
See Chapter 11, "PWM" for the PWM output, Chapter 12, "Synchronous Serial Port" for the synchronous serial port, Chapter 13, "UART" for UART, and Chapter 14, "I^2C Bus Interface" for the I^2C bus.

19.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The PWM output pins (PWM4, PWM5), UART pins (RXD0, TXD0,TXD1), synchronous serial port pins (SIN0, SCK0, SOUT0), and I^2C0 bus pins (SDA,SCL) can be used as the secondary, tertiary, or quartic function.
- The P40 to P41 pins can be used as the input pin of analogue comparator.
- The P42 to P47 pins can be used as an analog input pin of the successive approximation type ADC.

19.1.2 Configuration

Figure 19-1 shows the configuration of Port 4.



P4D : Port 4 data register
P4DIR : Port 4 direction register
P4CON0 : Port 4 control register 0
P4CON1 : Port 4 control register 1
P4MOD0 : Port 4 mode register 0
P4MOD1 : Port 4 mode register 1

Figure 19-1 Configuration of Port 4

[Note]
P42 to P47 are assigned to the successive approximation type ADC input. To use them as the analog input of successive approximation type ADC, set the appropriate port to the high-impedance output mode.

19.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P40/CMP0M/ SDA/SIN0	I/O	I/O port, Analogue comparator 0 non-inverting input	I^2C bus 0 data I/O pin	SSIO0 data input pin	-
P41/CMP0P/ SCL/SCK0	I/O	I/O port, Analogue comparator 0 inverting input	I^2C bus 0 clock I/O pin	SSIO0 clock I/O pin	-
P42/AIN6/ RXD0/SOUT0	I/O	I/O port, Successive approximation type ADC input	UART0 data input pin	SSIO0 data output pin	-
P43/AIN7/ TXD0/PWM4/ TXD1	I/O	I/O port, Successive approximation type ADC input	UART0 data output pin	PWM4 output pin	UART1 data output pin
P44/T0P4CK/ AIN8/SIN0	I/O	I/O port, PMW4 external clock input, Successive approximation type ADC input	-	SSIO0 data input pin	-
P45/T1P5CK/ AIN9/SCK0	I/O	I/O port, PMW5 external clock input, Successive approximation type ADC input	-	SSIO0 clock I/O pin	-
P46/T16CK0/ AIN10/SOUT0	I/O	I/O port, Timer 8, A external clock input, PWM6 external clock input, Successive approximation type ADC input	-	SSIO0 data output pin	-
P47/T16CK1/ AIN11/PWM5	I/O	I/O port, Timer 9, B external clock input, PWM7 external clock input, Successive approximation type ADC input	-	PWM5 output pin	-

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F244H	Port 4 data register	P4D	-	R/W	8	00H
0F245H	Port 4 direction register	P4DIR	-	R/W	8	00H
0F246H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F247H	Port 4 control register 1	P4CON1		R/W	8	00H
0F248H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F249H	Port 4 mode register 1	P4MOD1		R/W	8	00H

19.2.2 Port 4 Data Register (P4D)

Address: 0F244H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable.
In input mode, the input level of the Port 4 pin is read when P4D is read. Output mode or input mode is selected by using the port mode register (P4DIR) described later.

Description of bits

- **P47D-P40D** (bits 7-0)
  The P47D to P40D bits are used to set the output value of Port 4 pin in output mode and to read the pin level of Port 4 pin in input mode.

P47D	Description
0	Output or input level of the P47 pin: "L"
1	Output or input level of the P47 pin: "H"

P46D	Description
0	Output or input level of the P46 pin: "L"
1	Output or input level of the P46 pin: "H"

P45D	Description
0	Output or input level of the P45 pin: "L"
1	Output or input level of the P45 pin: "H"

P44D	Description
0	Output or input level of the P44 pin: "L"
1	Output or input level of the P44 pin: "H"

P43D	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

P42D	Description
0	Output or input level of the P42 pin: "L"
1	Output or input level of the P42 pin: "H"

P41D	Description
0	Output or input level of the P41 pin: "L"
1	Output or input level of the P41 pin: "H"

P40D	Description
0	Output or input level of the P40 pin: "L"
1	Output or input level of the P40 pin: "H"

19.2.3 Port 4 Direction Register (P4DIR)

Address: 0F245H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

Description of bits

- **P47DIR-P40DIR** (bits 7-0)
  The P47DIR to P40DIR bits are used to set the input/output mode of the port 4 pin.

P47DIR	Description
0	P47 pin: Output (initial value)
1	P47 pin: Input

P46DIR	Description
0	P46 pin: Output (initial value)
1	P46 pin: Input

P45DIR	Description
0	P45 pin: Output (initial value)
1	P45 pin: Input

P44DIR	Description
0	P44 pin: Output (initial value)
1	P44 pin: Input

P43DIR	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

19.2.4 Port 4 Control Registers 0, 1 (P4CON0, P4CON1)

Address: 0F246H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON0	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F247H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON1	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) used to select the output state of the Port 4 pin. The output state is different between input mode and output mode. Input or output is selected by using the P4DIR register.

Description of bits

- **P47C1-P40C1, P47C0-P40C0** (bits 7-0)
  The P47C1 to P40C1 and P47C0 to P40C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P47 pin		When output mode is selected (P47DIR bit = "0")	When input mode is selected (P47DIR bit = "1")
P47C1	**P47C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P46 pin		When output mode is selected (P46DIR bit = "0")	When input mode is selected (P46DIR bit = "1")
P46C1	**P46C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P45 pin		When output mode is selected (P45DIR bit = "0")	When input mode is selected (P45DIR bit = "1")
P45C1	**P45C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P44 pin		When output mode is selected (P44DIR bit = "0")	When input mode is selected (P44DIR bit = "1")
P44C1	**P44C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = "0")	When input mode is selected (P43DIR bit = "1")
P43C1	**P43C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = "0")	When input mode is selected (P42DIR bit = "1")
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

19.2.5 Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)

Address: 0F248H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD0	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F249H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD1	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of Port 4.

Description of bits

- **P47MD1, P47MD0** (bit 7)
  The P47MD1 and P47MD0 bits are used to select the primary or tertiary function of the P47 pin.

P47MD1	P47MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	PWM5 output pin (PWM5)
1	1	Do not use

- **P46MD1, P46MD0** (bit 6)
  The P46MD1 and P46MD0 bits are used to select the primary or tertiary function of the P46 pin.

P46MD1	P46MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	SIO0 data output pin (SOUT0)
1	1	Do not use

- **P45MD1, P45MD0** (bit 5)
  The P45MD1 and P45MD0 bits are used to select the primary or tertiary function of the P45 pin.

P45MD1	P45MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	SIO0 clock I/O pin (SCK0)
1	1	Do not use

- **P44MD1, P44MD0** (bit 4)
  The P44MD1 and P44MD0 bits are used to select the primary or tertiary function of the P44 pin.

P44MD1	P44MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	SIO0 data input pin (SIN0)
1	1	Do not use

- **P43MD1, P43MD0** (bit 3)
  The P43MD1 and P43MD0 bits are used to select the primary, secondary, tertiary, or quartic function of the P43 pin.

P43MD1	P43MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data output pin (TXD0)
1	0	PWM4 output pin (PWM4)
1	1	UART1 data output pin (TXD1)

- **P42MD1, P42MD0** (bit 2)
  The P42MD1 and P42MD0 bits are used to select the primary, secondary, or tertiary function of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data input pin (RXD0)
1	0	SIO0 data output pin (SOUT0)
1	1	Do not use

- **P41MD1, P41MD0** (bit 1)
  The P41MD1 and P41MD0 bits are used to select the primary, secondary, or tertiary function of the P41 pin.

P41MD1	P41MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C bus 0 clock I/O pin (SCL)
1	0	SIO0 clock I/O pin (SCK0)
1	1	Do not use

- **P40MD1, P40MD0** (bit 0)
  The P40MD1 and P40MD0 bits are used to select the primary, secondary, or tertiary function of the P40 pin.

P40MD1	P40MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C bus 0 data I/O pin (SDA)
1	0	SIO0 data input pin (SIN0)
1	1	Do not use

[Note]
When the pin is set to "Do not use" and the output mode is selected (by the Port 4 control register), the Port 4 output pin state is fixed as follows regardless of the data of the port data register P4D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

19.3 Description of Operation

19.3.1 Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0, 1 (P4CON0, P4CON1).
In the input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 4 control registers 0, 1 (P4CON0, P4CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

19.3.2 Secondary, Tertiary, and Quartic Functions

The PWM pins (PWM4, PWM5), UART pins (RXD0, TXD0, TXD1), synchronous serial port 0 pins (SIN0, SCK0, SOUT0), and I2C bus 0 pins (SDA, SCL) are assigned to Port 4 as the secondary, tertiary, and quartic functions. These pins can be used in the secondary, tertiary, or quartic function mode by setting the P47MD0 to P40MD0 and P47MD1 to P40MD1 bits of the Port 4 mode register (P4MOD0, P4MOD1).

[Note]
The P42 to P47 pins are assigned to the successive approximation type ADC input, and the P40 to P41 pins to the analogue comparator input. To use them as the analog input of successive approximation type ADC or analogue comparator input, set the appropriate port to the high-impedance output mode.

Chapter 20 Port 5

20 Port 5

20.1 General Description

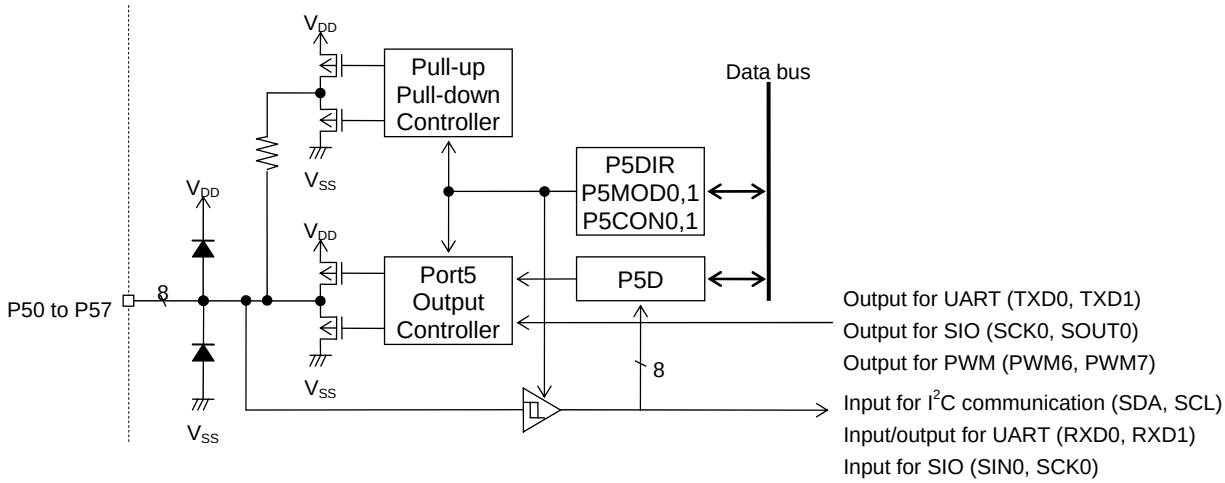
ML620Q151A/ML620Q152A/ML620Q153A includes a 4-bit input/output port, Port 5 (P54 to P57).
ML620Q154A/ML620Q155A/ML620Q156A includes a 5-bit input/output port, Port 5 (P53 to P57).
ML620Q157A/ML620Q158A/ML620Q159A includes a 8-bit input/output port, port 5 (P50 to P57).
For details, see Section 1.3.2, "List of Pins".

20.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The I^2C communication pins (SCL, SDA), PWM output pins (PWM6, PWM7), UART pins (RXD0, TXD0, RXD1, TXD1), and synchronous serial port pins (SIN0, SCK0, SOUT0) can be used as the secondary, tertiary, or quartic function.

20.1.2 Configuration

Figure 20-1 shows the configuration of Port 5.



P5D : Port 5 data register
P5DIR : Port 5 direction register
P5CON0 : Port 5 control register 0
P5CON1 : Port 5 control register 1
P5MOD0 : Port 5 mode register 0
P5MOD1 : Port 5 mode register 1

Figure 20-1 Configuration of Port 5

20.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P50/SDA/SIN0	I/O	I/O port	I^2C data I/O (SDA)	SSIO0 data input pin	-
P51/SCL/SCK0	I/O	I/O port	I^2C clock I/O (SCL)	SSIO0 clock I/O pin	-
P52/RXD1/SOUT0	I/O	I/O port	UART1 data input pin	SSIO0 data output pin	-
P53/TXD1/ PWM6	I/O	I/O port	UART1 data output pin	PWM6 output pin	-
P54/RXD0	I/O	I/O port	UART0 data input pin	-	-
P55/TXD0/ SIN0/TXD1	I/O	I/O port	UART0 data output pin	SSIO0 data input pin	UART1 data output pin
P56/SCK0	I/O	I/O port	-	SSIO0 clock I/O pin	-
P57/SOUT0/ PWM7	I/O	I/O port	-	SSIO0 data output pin	PWM7 output pin

20.2 Description of Registers

20.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F252H	Port 5 data register	P5D	-	R/W	8	00H
0F253H	Port 5 direction register	P5DIR	-	R/W	8	00H
0F254H	Port 5 control register 0	P5CON0	P5CON	R/W	8/16	00H
0F255H	Port 5 control register 1	P5CON1		R/W	8	00H
0F256H	Port 5 mode register 0	P5MOD0	P5MOD	R/W	8/16	00H
0F257H	Port 5 mode register 1	P5MOD1		R/W	8	00H

20.2.2 Port 5 Data Register (P5D)

Address: 0F252H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5D	P57D	P56D	P55D	P54D	P53D	P52D	P51D	P50D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5D is a special function register (SFR) to set the value to be output to the Port 5 pin or to read the input level of the Port 5. In output mode, the value of this register is output to the Port 5 pin. The value written to P5D is readable.
In input mode, the input level of the Port 5 pin is read when P5D is read. Output mode or input mode is selected by using the port mode register (P5DIR) described later.

Description of bits

- **P57D-P50D** (bits 7-0)
  The P57D to P50D bits are used to set the output value of the Port 5 pin in output mode and to read the pin level of the Port 5 pin in input mode.

P57D	Description
0	Output or input level of the P57 pin: "L"
1	Output or input level of the P57 pin: "H"

P56D	Description
0	Output or input level of the P56 pin: "L"
1	Output or input level of the P56 pin: "H"

P55D	Description
0	Output or input level of the P55 pin: "L"
1	Output or input level of the P55 pin: "H"

P54D	Description
0	Output or input level of the P54 pin: "L"
1	Output or input level of the P54 pin: "H"

P53D	Description
0	Output or input level of the P53 pin: "L"
1	Output or input level of the P53 pin: "H"

P52D	Description
0	Output or input level of the P52 pin: "L"
1	Output or input level of the P52 pin: "H"

P51D	Description
0	Output or input level of the P51 pin: "L"
1	Output or input level of the P51 pin: "H"

P50D	Description
0	Output or input level of the P50 pin: "L"
1	Output or input level of the P50 pin: "H"

20.2.3 Port 5 Direction Register (P5DIR)

Address: 0F253H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5DIR	P57DIR	P56DIR	P55DIR	P54DIR	P53DIR	P52DIR	P51DIR	P50DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5DIR is a special function register (SFR) to select the input/output mode of Port 5.

Description of bits

- **P57DIR-P50DIR** (bits 7-0)
  The P57DIR to P50DIR bits are used to set the input/output mode of the Port 5 pin.

P57DIR	Description
0	P57 pin: Output (initial value)
1	P57 pin: Input

P56DIR	Description
0	P56 pin: Output (initial value)
1	P56 pin: Input

P55DIR	Description
0	P55 pin: Output (initial value)
1	P55 pin: Input

P54DIR	Description
0	P54 pin: Output (initial value)
1	P54 pin: Input

P53DIR	Description
0	P53 pin: Output (initial value)
1	P53 pin: Input

P52DIR	Description
0	P52 pin: Output (initial value)
1	P52 pin: Input

P51DIR	Description
0	P51 pin: Output (initial value)
1	P51 pin: Input

P50DIR	Description
0	P50 pin: Output (initial value)
1	P50 pin: Input

20.2.4 Port 5 Control Registers 0, 1 (P5CON0, P5CON1)

Address: 0F254H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON0	P57C0	P56C0	P55C0	P54C0	P53C0	P52C0	P51C0	P50C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F255H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON1	P57C1	P56C1	P55C1	P54C1	P53C1	P52C1	P51C1	P50C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5CON0 and P5CON1 are special function registers (SFRs) used to select the output state of the Port 5 pin. The output state is different between input mode and output mode. Input or output is selected by using the P5DIR register.

Description of bits

- **P57C1-P50C1, P57C0-P50C0** (bits 7-0)
  The P57C1 to P50C1 and P57C0 to P50C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P57 pin		When output mode is selected (P57DIR bit = "0")	When input mode is selected (P57DIR bit = "1")
P57C1	**P57C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P56 pin		When output mode is selected (P56DIR bit = "0")	When input mode is selected (P56DIR bit = "1")
P56C1	**P56C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P55 pin		When output mode is selected (P55DIR bit = "0")	When input mode is selected (P55DIR bit = "1")
P55C1	**P55C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P54 pin		When output mode is selected (P54DIR bit = "0")	When input mode is selected (P54DIR bit = "1")
P54C1	**P54C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P53 pin		When output mode is selected (P53DIR bit = "0")	When input mode is selected (P53DIR bit = "1")
P53C1	**P53C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P52 pin		When output mode is selected (P52DIR bit = "0")	When input mode is selected (P52DIR bit = "1")
P52C1	**P52C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P51 pin		When output mode is selected (P51DIR bit = "0")	When input mode is selected (P51DIR bit = "1")
P51C1	**P51C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P50 pin		When output mode is selected (P50DIR bit = "0")	When input mode is selected (P50DIR bit = "1")
P50C1	**P50C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

20.2.5 Port 5 Mode Registers 0, 1 (P5MOD0, P5MOD1)

Address: 0F256H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD0	P57MD0	P56MD0	P55MD0	P54MD0	P53MD0	P52MD0	P51MD0	P50MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F257H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD1	P57MD1	P56MD1	P55MD1	P54MD1	P53MD1	P52MD1	P51MD1	P50MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5MOD0 and P5MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of Port 5.

Description of bits

- **P57MD1, P57MD0** (bit 7)
  The P57MD1 and P57MD0 bits are used to select the primary, tertiary, or quartic function of the P57 pin.

P57MD1	P57MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	SIO0 data output pin (SOUT0)
1	1	PWM7 output pin (PWM7)

- **P56MD1, P56MD0** (bit 6)
  The P56MD1 and P56MD0 bits are used to select the primary or tertiary function of the P56 pin.

P56MD1	P56MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	SIO0 clock I/O pin (SCK0)
1	1	Do not use

- **P55MD1, P55MD0** (bit 5)
  The P55MD1 and P55MD0 bits are used to select the primary, secondary, tertiary, or quartic function of the P55 pin.

P55MD1	P55MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data output pin (TXD0)
1	0	SIO0 data input pin (SIN0)
1	1	UART1 data output pin (TXD1)

- **P54MD1, P54MD0** (bit 4)
  The P54MD1 and P54MD0 bits are used to select the primary or secondary function of the P54 pin.

P54MD1	P54MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data input pin (RXD0)
1	0	Do not use
1	1	Do not use

- **P53MD1, P53MD0** (bit 3)
  The P53MD1 and P53MD0 bits are used to select the primary, secondary, or tertiary function of the P53 pin.

P53MD1	P53MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART1 data output pin (TXD1)
1	0	PWM6 output pin (PWM6)
1	1	Do not use

- **P52MD1, P52MD0** (bit 2)
  The P52MD1 and P52MD0 bits are used to select the primary, secondary, or tertiary function of the P52 pin.

P52MD1	P52MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART1 data input pin (RXD1)
1	0	SIO0 data output pin (SOUT0)
1	1	Do not use

- **P51MD1, P51MD0** (bit 1)
  The P51MD1 and P51MD0 bits are used to select the primary, secondary, or tertiary function of the P51 pin.

P51MD1	P51MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C communication clock I/O pin (SCL)
1	0	SIO0 clock I/O pin (SCK0)
1	1	Do not use

- **P50MD1, P50MD0** (bit 0)
  The P50MD1 and P50MD0 bits are used to select the primary, secondary, or tertiary function of the P50 pin.

P55MD1	P55MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C communication data I/O pin (SDA)
1	0	SIO0 data input pin (SIN0)
1	1	Do not use

[Note]

When the pin is set to "Do not use" and the output mode is selected (by the Port 5 control register), the Port 5 output pin state is fixed as follows regardless of the data of the port data register P5D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

20.3 Description of Operation

20.3.1 Input/Output Port Functions

For each pin of Port 5, either output or input is selected by setting the Port 5 direction register (P5DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 5 control registers 0, 1 (P5CON0, P5CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 5 control registers 0, 1 (P5CON0, P5CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 5 depending on the value set by the Port 5 data register (P5D).
In input mode, the input level of each pin of Port 5 can be read from the Port 5 data register (P5D).

20.3.2 Secondary, Tertiary, and Quartic Functions

The I^2C communication pins (SDA, SCL), PWM output pins (PWM6, PWM7), UART pins (RXD0, TXD0, RXD1,TXD1), and synchronous serial port 0 pins (SIN0, SCK0, SOUT0) are assigned to Port 5 as the secondary, tertiary, and quartic functions. These pins can be used in the secondary, tertiary, or quartic function mode by setting the P57MD0 to P50MD0 and P57MD1 to P50MD1 bits of the Port 5 mode register (P5MOD0, P5MOD1).

Chapter 21 Port 6

21 Port 6

21.1 General Description

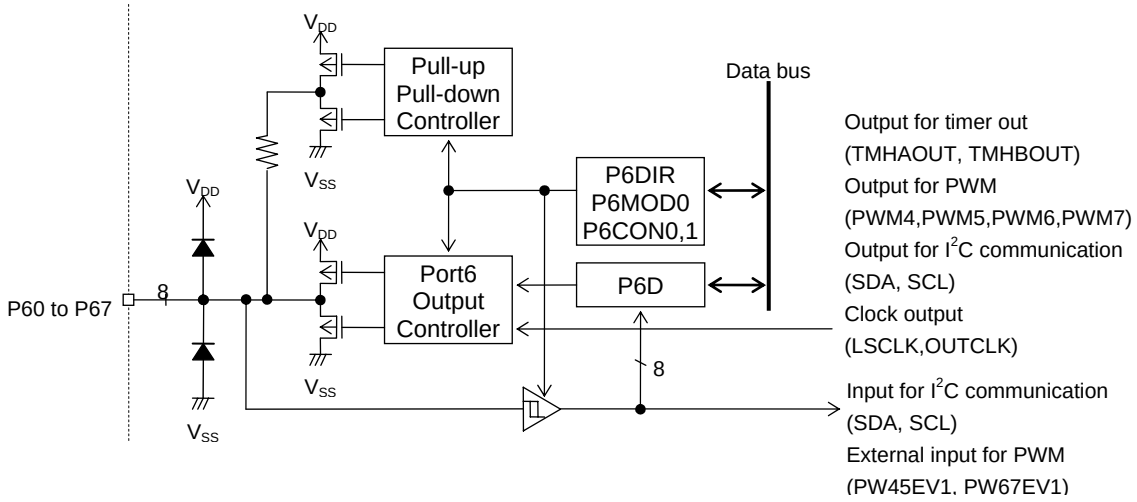
ML620Q151A/ML620Q152A/ML620Q153A includes a 4-bit input/output port, Port 6 (P60 to P63).
ML620Q154A/ML620Q155A/ML620Q156A includes a 5-bit input/output port, Port 6 (P60 to P64).
ML620Q157A/ML620Q158A/ML620Q159A includes a 8-bit input/output port, port 6 (P60 to P67).
For details, see Section 1.3.2, "List of Pins".

21.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The low-speed clock (LSCLK) output, high-speed clock (OUTCLK) output, I^2C communication pins (SCL, SDA), PWM output pins (PWM4, PWM5, PWM6, PWM7), and timer out functions (TMHAOUT, TMHBOUT) can be used as the secondary, tertiary, and quartic functions.
- The P62 pin can be used as the PW45EV1 input pin for PWM4 and PWM5.
- The P63 pin can be used as the PW67EV1 input pin for PWM6 and PWM7.

21.1.2 Configuration

Figure 21-1 shows the configuration of Port 6.



P6D : Port 6 data register
P6DIR : Port 6 direction register
P6CON0 : Port 6 control register 0
P6CON1 : Port 6 control register 1
P6MOD0 : Port 6 mode register 0

Figure 21-1 Configuration of Port 6

21.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P60/SDA/ TMHAOUT/PWM6	I/O	I/O port	I^2C data I/O (SDA)	Timer A out (TMHAOUT)	PWM6 output
P61/SCL/ TMHBOUT/PWM7	I/O	I/O port	I^2C clock I/O (SCL)	Timer B out (TMHBOUT)	PWM7 output
P62/PW45EV1	I/O	I/O port, PW45EV1 input	-	-	-
P63/PW67EV1	I/O	I/O port, PW67EV1 input	-	-	-
P64/PWM4	I/O	I/O port	-	PWM4 output	-
P65/LSCLK/PWM5	I/O	I/O port	LSCLK	PWM5 output	-
P66/OUTCLK/ PWM6	I/O	I/O port	OUTCLK	PWM6 output	-
P67	I/O	I/O port	-	-	-

21.2 Description of Registers

21.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F260H	Port 6 data register	P6D	-	R/W	8	00H
0F261H	Port 6 direction register	P6DIR	-	R/W	8	00H
0F262H	Port 6 control register 0	P6CON0	P6CON	R/W	8/16	00H
0F263H	Port 6 control register 1	P6CON1		R/W	8	00H
0F264H	Port 6 mode register 0	P6MOD0	P6MOD	R/W	8/16	00H
0F265H	Port 6 mode register 1	P6MOD1		R/W	8	00H

21.2.2 Port 6 Data Register (P6D)

Address: 0F260H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6D	P67D	P66D	P65D	P64D	P63D	P62D	P61D	P60D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6D is a special function register (SFR) to set the value to be output to the Port 6 pin or to read the input level of the Port 6. In output mode, the value of this register is output to the Port 6 pin. The value written to P6D is readable.
In input mode, the input level of the Port 6 pin is read when P6D is read. Output mode or input mode is selected by using the port mode register (P6DIR) described later.

Description of bits

- **P67D-P60D** (bits 7-0)
  The P67D to P60D bits are used to set the output value of the Port 6 pin in output mode and to read the pin level of the Port 6 pin in input mode.

P67D	Description
0	Output or input level of the P67 pin: "L"
1	Output or input level of the P67 pin: "H"

P66D	Description
0	Output or input level of the P66 pin: "L"
1	Output or input level of the P66 pin: "H"

P65D	Description
0	Output or input level of the P65 pin: "L"
1	Output or input level of the P65 pin: "H"

P64D	Description
0	Output or input level of the P64 pin: "L"
1	Output or input level of the P64 pin: "H"

P63D	Description
0	Output or input level of the P63 pin: "L"
1	Output or input level of the P63 pin: "H"

P62D	Description
0	Output or input level of the P62 pin: "L"
1	Output or input level of the P62 pin: "H"

P61D	Description
0	Output or input level of the P61 pin: "L"
1	Output or input level of the P61 pin: "H"

P60D	Description
0	Output or input level of the P60 pin: "L"
1	Output or input level of the P60 pin: "H"

21.2.3 Port 6 Direction Register (P6DIR)

Address: 0F261H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6DIR	P67DIR	P66DIR	P65DIR	P64DIR	P63DIR	P62DIR	P61DIR	P60DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6DIR is a special function register (SFR) to select the input/output mode of Port 6.

Description of bits

- **P67DIR-P60DIR** (bits 7-0)
  The P67DIR to P60DIR bits are used to set the input/output mode of the port 6 pin.

P67DIR	Description
0	P67 pin: Output (initial value)
1	P67 pin: Input

P66DIR	Description
0	P66 pin: Output (initial value)
1	P66 pin: Input

P65DIR	Description
0	P65 pin: Output (initial value)
1	P65 pin: Input

P64DIR	Description
0	P64 pin: Output (initial value)
1	P64 pin: Input

P63DIR	Description
0	P63 pin: Output (initial value)
1	P63 pin: Input

P62DIR	Description
0	P62 pin: Output (initial value)
1	P62 pin: Input

P61DIR	Description
0	P61 pin: Output (initial value)
1	P61 pin: Input

P60DIR	Description
0	P60 pin: Output (initial value)
1	P60 pin: Input

21.2.4 Port 6 Control Registers 0, 1 (P6CON0, P6CON1)

Address: 0F262H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P6CON0	P67C0	P66C0	P65C0	P64C0	P63C0	P62C0	P61C0	P60C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F263H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P6CON1	P67C1	P66C1	P65C1	P64C1	P63C1	P62C1	P61C1	P60C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6CON0 and P6CON1 are special function registers (SFRs) used to select the input/output state of the Port 6 pin. The output state is different between input mode and output mode. Input or output is selected by using the P6DIR register.

Description of bits

- **P67C1-P60C1, P67C0-P60C0** (bits 7-0)
  The P67C1 to P60C1 and P67C0 to P60C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P67 pin		When output mode is selected (P67DIR bit = "0")	When input mode is selected (P67DIR bit = "1")
P67C1	**P67C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P66 pin		When output mode is selected (P66DIR bit = "0")	When input mode is selected (P66DIR bit = "1")
P66C1	**P66C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P65 pin		When output mode is selected (P65DIR bit = "0")	When input mode is selected (P65DIR bit = "1")
P65C1	**P65C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P64 pin		When output mode is selected (P64DIR bit = "0")	When input mode is selected (P64DIR bit = "1")
P64C1	**P64C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P63 pin		When output mode is selected (P63DIR bit = "0")	When input mode is selected (P63DIR bit = "1")
P63C1	**P63C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P62 pin		When output mode is selected (P62DIR bit = "0")	When input mode is selected (P62DIR bit = "1")
P62C1	**P62C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P61 pin		When output mode is selected (P61DIR bit = "0")	When input mode is selected (P61DIR bit = "1")
P61C1	**P61C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P60 pin		When output mode is selected (P60DIR bit = "0")	When input mode is selected (P60DIR bit = "1")
P60C1	**P60C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

21.2.5 Port 6 Mode Registers 0, 1 (P6MOD0, P6MOD1)

Address: 0F264H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P6MOD0	-	P66MD0	P65MD0	P64MD0	-	-	P61MD0	P60MD0
R/W	R	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F265H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P6MOD1	-	P66MD1	P65MD1	P64MD1	-	-	P61MD1	P60MD1
R/W	R	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6MOD0 and P6MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of Port 6.

Description of bits

- **P66MD1, P66MD0** (bit 6)
  The P66MD1 and P66MD0 bits are used to select the primary or tertiary function of the P66 pin.

P66MD1	P66MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	High-speed clock (OUTCLK) output function
1	0	PWM6 output pin (PWM6)
1	1	Do not use

- **P65MD1, P65MD0** (bit 5)
  The P65MD1 and P65MD0 bits are used to select the primary, secondary, or tertiary function of the P65 pin.

P65MD1	P65MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Low-speed clock (LSCLK) output function
1	0	PWM5 output pin (PWM5)
1	1	Do not use

- **P64MD1, P64MD0** (bit 4)
  The P64MD1 and P64MD0 bits are used to select the primary or tertiary function of the P64 pin.

P64MD1	P64MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Do not use
1	0	PWM4 output pin (PWM4)
1	1	Do not use

- **P61MD1, P61MD0** (bit 1)
  The P61MD1 and P61MD0 bits are used to select the primary, secondary, tertiary, or quartic function of the P61 pin.

P61MD1	P61MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C communication clock I/O pin (SCL)
1	0	Timer B out output function (TMHBOUT)
1	1	PWM7 output pin (PWM7)

- **P60MD1, P60MD0** (bit 0)
  The P60MD1 and P60MD0 bits are used to select the primary, secondary, tertiary, or quartic function of the P60 pin.

P60MD1	P60MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C communication data I/O pin (SDA)
1	0	Timer A out output function (TMHAOUT)
1	1	PWM6 output pin (PWM6)

[Note]
When the pin is set to "Do not use" and the output mode is selected (by the Port 6 control register), the Port 6 output pin state is fixed as follows regardless of the data of the port data register P6D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

21.3 Description of Operation

21.3.1 Input/Output Port Functions

For each pin of Port 6, either output or input is selected by setting the Port 6 direction register (P6DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 6 control registers 0, 1 (P6CON0, P6CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 6 control registers 0, 1 (P6CON0, P6CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 6 depending on the value set by the Port 6 data register (P6D).
In input mode, the input level of each Port 6 pin can be read from the Port 6 data register (P6D).

21.3.2 Secondary, Tertiary, and Quartic Functions

The I^2C communication pins (SDA, SCL), timer out functions (TMHAOUT, TMHBOUT), PWM output functions (PWM4, PWM5, PWM6, PWM7), low-speed clock (LSCLK) output, and high-speed clock (OUTCLK) are assigned to Port 6 as the secondary, tertiary, and quartic functions. These pins can be used in the secondary, tertiary, and quartic function modes by setting the P66MD0, P66MD1, P65MD0, P65MD1, P64MD0, P64MD1, P61MD0, P61MD1, P60MD0, and P60MD1 bits of the Port 6 mode register (P6MOD0, P6MOD1).

Chapter 22 Port 7

22 Port 7

22.1 General Description

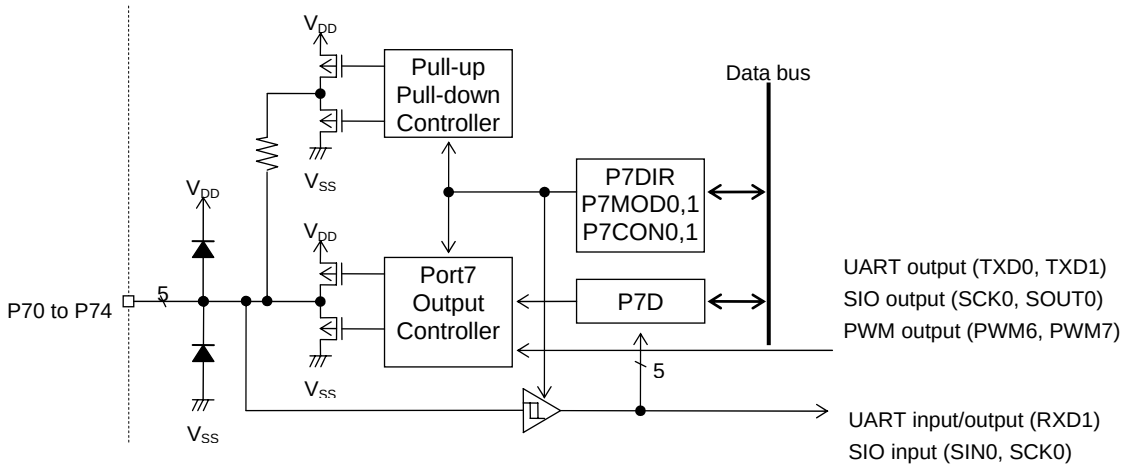
ML620Q157A/ML620Q158A/ML620Q159A includes a 5-bit input/output port, port 7 (P70 to P74).
ML620Q151A/ML620Q152A/ML620Q153A/ML620Q154A/ML620Q155A/ML620Q156A do not include the port 7.
For details, see Section 1.3.2, "List of Pins".

22.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Allows selection of PWM output (PWM6, PWM7), UART0/1 communication pins (TXD0, RXD1, TXD1), and SSIO0 communication pins (SCK0, SIN0, SOUT0) as the secondary, tertiary functions or quartic function.

22.1.2 Configuration

Figure 22-1 shows the configuration of Port 7.



P7D : Port 7 data register
P7DIR : Port 7 direction register
P7CON0 : Port 7 control register 0
P7CON1 : Port 7 control register 1
P7MOD0 : Port 7 mode register 0
P7MOD1 : Port 7 mode register 1

Figure 22-1 Configuration of Port 7

22.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P70/PWM6	I/O	I/O port	-	PWM6 output	-
P71/PWM7	I/O	I/O port	-	PWM7 output	-
P72/RXD1/SIN0	I/O	I/O port	UART1 data input	SSIO0 data input	-
P73/TXD1/SCK0/TXD0	I/O	I/O port	UART1 data output	SSIO0 clock I/O	UART0 data output
P74/SOUT0	I/O	I/O port	-	SSIO0 data output	-

22.2 Description of Registers

22.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F26EH	Port 7 data register	P7D	-	R/W	8	00H
0F26FH	Port 7 direction register	P7DIR	-	R/W	8	00H
0F270H	Port 7 control register 0	P7CON0	P7CON	R/W	8/16	00H
0F271H	Port 7 control register 1	P7CON1		R/W	8	00H
0F272H	Port 7 mode register 0	P7MOD0	P7MOD	R/W	8/16	00H
0F273H	Port 7 mode register 1	P7MOD1		R/W	8	00H

22.2.2 Port 7 Data Register (P7D)

Address: 0F26EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P7D	-	-	-	P74D	P73D	P72D	P71D	P70D
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P7D is a special function register (SFR) to set the value to be output to the Port 7 pin or to read the input level of the Port 7. In output mode, the value of this register is output to the Port 7 pin. The value written to P7D is readable.
In input mode, the input level of the Port 7 pin is read when P7D is read. Output mode or input mode is selected by using the port mode register (P7DIR) described later.

Description of bits

- **P74D-P70D** (bits 4-0)
  The P74D to P70D bits are used to set the output value of the Port 7 pin in output mode and to read the pin level of the Port 7 pin in input mode.

P74D	Description
0	Output or input level of the P74 pin: "L"
1	Output or input level of the P74 pin: "H"

P73D	Description
0	Output or input level of the P73 pin: "L"
1	Output or input level of the P73 pin: "H"

P72D	Description
0	Output or input level of the P72 pin: "L"
1	Output or input level of the P72 pin: "H"

P71D	Description
0	Output or input level of the P71 pin: "L"
1	Output or input level of the P71 pin: "H"

P70D	Description
0	Output or input level of the P70 pin: "L"
1	Output or input level of the P70 pin: "H"

22.2.3 Port 7 Direction Register (P7DIR)

Address: 0F26FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P7DIR	-	-	-	P74DIR	P73DIR	P72DIR	P71DIR	P70DIR
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P7DIR is a special function register (SFR) to select the input/output mode of Port 7.

Description of bits

- **P74DIR-P70DIR** (bits 4-0)
  The P74DIR to P70DIR bits are used to set the input/output mode of the Port 7 pin.

P74DIR	Description
0	P74 pin: Output (initial value)
1	P74 pin: Input

P73DIR	Description
0	P73 pin: Output (initial value)
1	P73 pin: Input

P72DIR	Description
0	P72 pin: Output (initial value)
1	P72 pin: Input

P71DIR	Description
0	P71 pin: Output (initial value)
1	P71 pin: Input

P70DIR	Description
0	P70 pin: Output (initial value)
1	P70 pin: Input

22.2.4 Port 7 Control Registers 0, 1 (P7CON0, P7CON1)

Address: 0F270H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P7CON0	-	-	-	P74C0	P73C0	P72C0	P71C0	P70C0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F271H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P7CON1	-	-	-	P74C1	P73C1	P72C1	P71C1	P70C1
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P7CON0 and P7CON1 are special function registers (SFRs) used to select the input/output state of the Port 7 pin. The output state is different between input mode and output mode. Input or output is selected by using the P7DIR register.

Description of bits

- **P74C1-P70C1, P74C0-P70C0** (bits 4-0)
  The P74C1 to P70C1 and P74C0 to P70C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P74 pin		When output mode is selected (P74DIR bit = "0")	When input mode is selected (P74DIR bit = "1")
P74C1	**P74C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P73 pin		When output mode is selected (P73DIR bit = "0")	When input mode is selected (P73DIR bit = "1")
P73C1	**P73C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P72 pin		When output mode is selected (P72DIR bit = "0")	When input mode is selected (P72DIR bit = "1")
P72C1	**P72C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P71 pin		When output mode is selected (P71DIR bit = "0")	When input mode is selected (P71DIR bit = "1")
P71C1	**P71C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P70 pin		When output mode is selected (P70DIR bit = "0")	When input mode is selected (P70DIR bit = "1")
P70C1	**P70C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

22.2.5 Port 7 Mode Registers 0, 1 (P7MOD0, P7MOD1)

Address: 0F272H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P7MOD0	-	-	-	P74MD0	P73MD0	P72MD0	P71MD0	P70MD0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F273H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P7MOD1	-	-	-	P74MD1	P73MD1	P72MD1	P71MD1	P70MD1
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P7MOD0 and P7MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary or quartic function of the Port 7.

Description of bits

- **P74MD1, P74MD0** (bit 4)
  The P74MD1 and P74MD0 bits are used to select the primary, secondary, or tertiary function of the P74 pin.

P74MD1	P74MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	SSIO0 data output pin (SOUT0)
1	1	Do not use

- **P73MD1, P73MD0** (bit 3)
  The P73MD1 and P73MD0 bits are used to select the primary, secondary, tertiary, or quartic function of the P73 pin.

P73MD1	P73MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART1 data output pin (TXD1)
1	0	SSIO0 clock I/O pin (SCK0)
1	1	UART0 data output pin (TXD0)

- **P72MD1, P72MD0** (bit 2)
  The P72MD1 and P72MD0 bits are used to select the primary, secondary or tertiary function of the P72 pin.

P72MD1	P72MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART1 data input pin (RXD1)
1	0	SSIO0 data input pin (SIN0)
1	1	Do not use

- **P71MD1, P71MD0** (bit 1)
  The P71MD1 and P71MD0 bits are used to select the primary, secondary, or tertiary function of the P71 pin.

P71MD1	P71MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	PWM7 output (PWM7)
1	1	Do not use

- **P70MD1, P70MD0** (bit 0)
  The P70MD1 and P70MD0 bits are used to select the primary, secondary, or tertiary function of the P70 pin.

P70MD1	P70MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	PWM6 output (PWM6)
1	1	Do not use

[Note]
When the pin is set to "Do not use" and the output mode is selected (by the Port 7 control register), the Port 7 output pin state is fixed as follows regardless of the data of the port data register P7D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

22.3 Description of Operation

22.3.1 Input/Output Port Functions

For each pin of Port 7, either output or input is selected by setting the Port 7 direction register (P7DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 7 control registers 0, 1 (P7CON0, P7CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 7 control registers 0, 1 (P7CON0, P7CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 7 depending on the value set by the Port 7 data register (P7D).
In input mode, the input level of each Port 7 pin can be read from the Port 7 data register (P7D).

22.3.2 Secondary and Tertiary Functions

The PWM output (PWM6, PWM7), UART0/1 communication pins (RXD0, TXD1, RXD1), and SSIO0 communication pins (SCK0, SIN0, SOUT0) are assigned to Port 7 as the secondary, tertiary and quartic functions. These pins can be used in the secondary or tertiary function mode by setting the P74MD0 to P70MD0 and P74MD1 to P70MD1 bits of the Port 7 mode registers (P7MOD0, P7MOD1).

Chapter 23 Port 8

23 Port 8

23.1 General Description

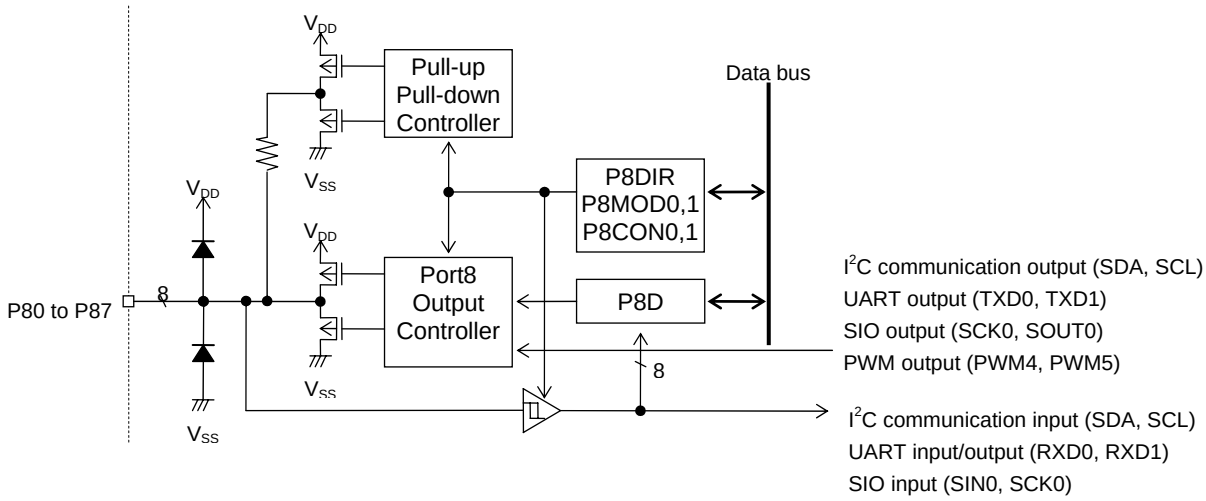
This LSI includes a 8-bit input/output port, Port 8 (P80 to P87).

23.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Allows selection of I^2C communication pins (SDA, SCL), PWM output (PWM4, PWM5), UART0/1 communication pins (TXD0, RXD0, TXD1, RXD1), and SSIO0 communication pins (SCK0, SIN0, SOUT0) as the secondary or tertiary functions.

23.1.2 Configuration

Figure 23-1 shows the configuration of Port 8.



P8D : Port 8 data register
P8DIR : Port 8 direction register
P8CON0 : Port 8 control register 0
P8CON1 : Port 8 control register 1
P8MOD0 : Port 8 mode register 0
P8MOD1 : Port 8 mode register 1

Figure 23-1 Configuration of Port 8

23.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P80/SDA/SIN0	I/O	I/O port	I^2C data I/O (SDA)	SSIO0 data input
P81/SCL/SCK0	I/O	I/O port	I^2C clock I/O (SCL)	SSIO0 clock I/O
P82/SOUT0	I/O	I/O port	-	SSIO0 data output
P83/PWM5	I/O	I/O port	-	PWM5 output
P84/RXD1/SIN0	I/O	I/O port	UART1 data input	SSIO0 data input
P85/TXD1/SCK0	I/O	I/O port	UART1 data output	SSIO0 clock I/O
P86/RXD0/SOUT0	I/O	I/O port	UART0 data input	SSIO0 data output
P87/TXD0/PWM4	I/O	I/O port	UART0 data output	PWM4 output

23.2 Description of Registers

23.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2DEH	Port 8 data register	P8D	-	R/W	8	00H
0F2DFH	Port 8 direction register	P8DIR	-	R/W	8	00H
0F2E0H	Port 8 control register 0	P8CON0	P8CON	R/W	8/16	00H
0F2E1H	Port 8 control register 1	P8CON1		R/W	8	00H
0F2E2H	Port 8 mode register 0	P8MOD0	P8MOD	R/W	8/16	00H
0F2E3H	Port 8 mode register 1	P8MOD1		R/W	8	00H

23.2.2 Port 8 Data Register (P8D)

Address: 0F2DEH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8D	P87D	P86D	P85D	P84D	P83D	P82D	P81D	P80D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8D is a special function register (SFR) to set the value to be output to the Port 8 pin or to read the input level of the Port 8. In output mode, the value of this register is output to the Port 8 pin. The value written to P8D is readable.
In input mode, the input level of the Port 8 pin is read when P8D is read. Output mode or input mode is selected by using the port mode register (P8DIR) described later.

Description of bits

- **P87D-P80D** (bits 7-0)
  The P87D to P80D bits are used to set the output value of the Port 8 pin in output mode and to read the pin level of the Port 8 pin in input mode.

P87D	Description
0	Output or input level of the P87 pin: "L"
1	Output or input level of the P87 pin: "H"

P86D	Description
0	Output or input level of the P86 pin: "L"
1	Output or input level of the P86 pin: "H"

P85D	Description
0	Output or input level of the P85 pin: "L"
1	Output or input level of the P85 pin: "H"

P84D	Description
0	Output or input level of the P84 pin: "L"
1	Output or input level of the P84 pin: "H"

P83D	Description
0	Output or input level of the P83 pin: "L"
1	Output or input level of the P83 pin: "H"

P82D	Description
0	Output or input level of the P82 pin: "L"
1	Output or input level of the P82 pin: "H"

P81D	Description
0	Output or input level of the P81 pin: "L"
1	Output or input level of the P81 pin: "H"

P80D	Description
0	Output or input level of the P80 pin: "L"
1	Output or input level of the P80 pin: "H"

23.2.3 Port 8 Direction Register (P8DIR)

Address: 0F2DFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8DIR	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	P82DIR	P81DIR	P80DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8DIR is a special function register (SFR) to select the input/output mode of Port 8.

Description of bits

- **P87DIR-P80DIR** (bits 7-0)
  The P87DIR to P80DIR bits are used to set the input/output mode of the Port 8 pin.

P87DIR	Description
0	P87 pin: Output (initial value)
1	P87 pin: Input

P86DIR	Description
0	P86 pin: Output (initial value)
1	P86 pin: Input

P85DIR	Description
0	P85 pin: Output (initial value)
1	P85 pin: Input

P84DIR	Description
0	P84 pin: Output (initial value)
1	P84 pin: Input

P83DIR	Description
0	P83 pin: Output (initial value)
1	P83 pin: Input

P82DIR	Description
0	P82 pin: Output (initial value)
1	P82 pin: Input

P81DIR	Description
0	P81 pin: Output (initial value)
1	P81 pin: Input

P80DIR	Description
0	P80 pin: Output (initial value)
1	P80 pin: Input

23.2.4 Port 8 Control Registers 0, 1 (P8CON0, P8CON1)

Address: 0F2E0H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P8CON0	P87C0	P86C0	P85C0	P84C0	P83C0	P82C0	P81C0	P80C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F2E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8CON1	P87C1	P86C1	P85C1	P84C1	P83C1	P82C1	P81C1	P80C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8CON0 and P8CON1 are special function registers (SFRs) used to select the input/output state of the Port 8 pin. The output state is different between input mode and output mode. Input or output is selected by using the P8DIR register.

Description of bits

- **P87C1-P80C1, P87C0-P80C0** (bits 7-0)
  The P87C1 to P80C1 and P87C0 to P80C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P87 pin		When output mode is selected (P87DIR bit = "0")	When input mode is selected (P87DIR bit = "1")
P87C1	**P87C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P86 pin		When output mode is selected (P86DIR bit = "0")	When input mode is selected (P86DIR bit = "1")
P86C1	**P86C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P85 pin		When output mode is selected (P85DIR bit = "0")	When input mode is selected (P85DIR bit = "1")
P85C1	**P85C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P84 pin		When output mode is selected (P84DIR bit = "0")	When input mode is selected (P84DIR bit = "1")
P84C1	**P84C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P83 pin		When output mode is selected (P83DIR bit = "0")	When input mode is selected (P83DIR bit = "1")
P83C1	**P83C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P82 pin		When output mode is selected (P82DIR bit = "0")	When input mode is selected (P82DIR bit = "1")
P82C1	**P82C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P81 pin		When output mode is selected (P81DIR bit = "0")	When input mode is selected (P81DIR bit = "1")
P81C1	**P81C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P80 pin		When output mode is selected (P80DIR bit = "0")	When input mode is selected (P80DIR bit = "1")
P80C1	**P80C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

23.2.5 Port 8 Mode Registers 0, 1 (P8MOD0, P8MOD1)

Address: 0F2E2H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P8MOD0	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	P82MD0	P81MD0	P80MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F2E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8MOD1	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	P82MD1	P81MD1	P80MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8MOD0 and P8MOD1 are special function registers (SFRs) used to select the primary, secondary, or tertiary function of the Port 3.

Description of bits

- **P87MD1, P87MD0** (bit 7)
  The P87MD1 and P87MD0 bits are used to select the primary, secondary, or tertiary function of the P87 pin.

P87MD1	P87MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART0 data output (TXD0)
1	0	PWM4 output pin (PWM4)
1	1	Do not use

- **P86MD1, P86MD0** (bit 6)
  The P86MD1 and P86MD0 bits are used to select the primary, secondary, or tertiary function of the P86 pin.

P86MD1	P86MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART0 data input pin (RXD0)
1	0	SSIO0 data output pin (SOUT0)
1	1	Do not use

- **P85MD1, P85MD0** (bit 5)
  The P85MD1 and P85MD0 bits are used to select the primary, secondary, or tertiary function of the P85 pin.

P85MD1	P85MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART1 data output (TXD1)
1	0	SSIO0 synchronous clock I/O pin (SCK0)
1	1	Do not use

- **P84MD1, P84MD0** (bit 4)
  The P84MD1 and P84MD0 bits are used to select the primary, secondary, or tertiary function of the P84 pin.

P84MD1	P84MD0	Description
0	0	General-purpose output port function (initial value)
0	1	UART1 data input pin (RXD1)
1	0	SSIO0 data input pin (SIN0)
1	1	Do not use

- **P83MD1, P83MD0** (bit 3)
  The P83MD1 and P83MD0 bits are used to select the primary or tertiary function of the P83 pin.

P83MD1	P83MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	PWM5 output pin (PWM5)
1	1	Do not use

- **P82MD1, P82MD0** (bit 2)
  The P82MD1 and P82MD0 bits are used to select the primary or tertiary function of the P82 pin.

P82MD1	P82MD0	Description
0	0	General-purpose output port function (initial value)
0	1	Do not use
1	0	SSIO0 data output pin (SOUT0)
1	1	Do not use

- **P81MD1, P81MD0** (bit 1)
  The P81MD1 and P81MD0 bits are used to select the primary, secondary, or tertiary function of the P81 pin.

P81MD1	P81MD0	Description
0	0	General-purpose output port function (initial value)
0	1	I^2C clock I/O (SCL)
1	0	SSIO0 synchronous clock I/O pin (SCK0)
1	1	Do not use

- **P80MD1, P80MD0** (bit 0)
  The P80MD1 and P80MD0 bits are used to select the primary, secondary, or tertiary function of the P80 pin.

P80MD1	P80MD0	Description
0	0	General-purpose output port function (initial value)
0	1	I^2C data I/O (SDA)
1	0	SSIO0 data input pin (SIN0)
1	1	Do not use

[Note]
When the pin is set to "Do not use" and the output mode is selected (by the Port 8 control register), the Port 8 output pin state is fixed as follows regardless of the data of the port data register P8D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

23.3 Description of Operation

23.3.1 Input/Output Port Functions

For each pin of Port 8, either output or input is selected by setting the Port 8 direction register (P8DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 8 control registers 0, 1 (P8CON0, P8CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 8 control registers 0, 1 (P8CON0, P8CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 8 depending on the value set by the Port 8 data register (P8D).
In input mode, the input level of each Port 8 pin can be read from the Port 8 data register (P8D).

23.3.2 Secondary and Tertiary Functions

The I^2C communication pins (SDA, SCL), PWM output (PWM4, PWM5), UART0/1 communication pins (TXD0, RXD0, TXD1, RXD1), and SSIO0 communication pins (SCK0, SIN0, SOUT0) are assigned to Port 8 as the secondary and tertiary functions. These pins can be used in the secondary or tertiary function mode by setting the P87MD0 to P80MD0 and P87MD1 to P80MD1 bits of the Port 8 mode registers (P8MOD0, P8MOD1).

Chapter 24 Successive Approximation Type A/D Converter

24 Successive Approximation Type A/D Converter (SA-ADC)

24.1 General Description

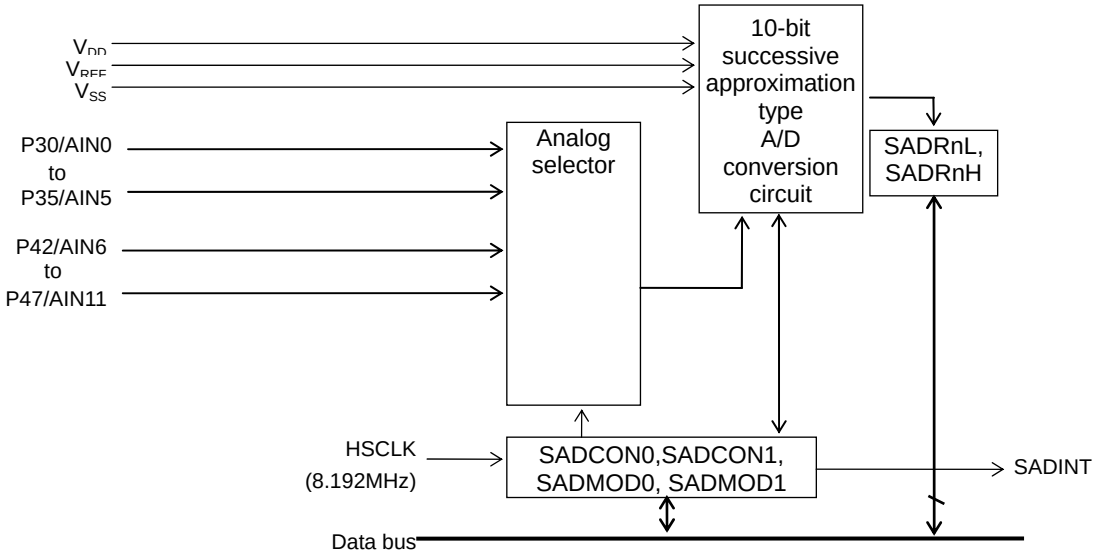
This LSI has an internal 12-channel successive approximation type A/D converter (SA-ADC).
The successive approximation type A/D converter works only when the DSAD bit of the block control register 4 (BLKCON4) is set to "0". When the DSAD bit is set to "1", every function of the successive approximation type A/D converter is reset. For block control registers, see Chapter 4, "MCU Control Function".

24.1.1 Features

- Internal sample/hold 10-bit successive approximation type A/D converter, which enables channel selection from 12 channels.

24.1.2 Configuration

Figure 24-1 shows the configuration of SA-ADC.



SADRnL : SA-ADC result register nL
SADRnH : SA-ADC result register nH
SADCON0 : SA-ADC control register 0
SADCON1 : SA-ADC control register 1
SADMOD0 : SA-ADC mode register 0
SADMOD1 : SA-ADC mode register 1

n: 0 to 11

Figure 24-1 Configuration of SA-ADC

24.1.3 List of Pins

Pin name	I/O	Function
V_{DD}	-	Positive power supply pin for the successive approximation type A/D converter
V_{REF}	-	Reference power supply pin for the successive approximation type A/D converter
V_{SS}	-	Negative power supply pin for the successive approximation type A/D converter
P30/EXI6/AIN0/PW45EV1	O	I/O port, External interrupt, PW45EV1 input, Successive approximation type A/D converter input pin 0
P31/EXI7/AIN1/PW67EV1	O	I/O port, External interrupt, PW67EV1 input, Successive approximation type A/D converter input pin 1
P32/AIN2/PW45EV0	O	I/O port, PW45EV0 input, Successive approximation type A/D converter input pin 2
P33/AIN3/PW67EV0	O	I/O port, PW67EV0 input, Successive approximation type A/D converter input pin 3
P34/AIN4/PWM4	O	I/O port, PWM4 output, Successive approximation type A/D converter input pin 4
P35/AIN5/PWM5	O	I/O port, PWM5 output, Successive approximation type A/D converter input pin 5
P42/AIN6/RXD0/SOUT0	O	I/O port, UART0 data input, SSIO0 data output, Successive approximation type A/D converter input pin 6
P43/AIN7/TXD0/PWM4/TXD1	O	I/O port, UART0 data output, PWM4 output, UART1 data output, Successive approximation type A/D converter input pin 7
P44/AIN8/T0P4CK/SIN0	O	I/O port, PWM4 external clock input, SSIO0 data input, Successive approximation type A/D converter input pin 8
P45/AIN9/T1P5CK/SCK0	O	I/O port, PWM5 external clock input, SSIO0 synchronous clock I/O, Successive approximation type A/D converter input pin 9
P46/AIN10/T16CK0/SOUT0	O	I/O port, Timer 8,A external clock input, PWM6 external clock input, SSIO0 data output, Successive approximation type A/D converter input pin 10
P47/AIN11/T16CK1/PWM5	O	I/O port, Timer 9,B external clock input, PWM7 external clock input, PWM5 output, Successive approximation type A/D converter input pin 11

24.2 Description of Registers

24.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F8D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F8D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F8D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F8D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F8D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F8D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F8D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F8D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F8D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F8D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F8DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F8DBH	SA-ADC result register 5H	SADR5H		R	8	00H
0F8DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F8DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F8DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F8DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F8E0H	SA-ADC result register 8L	SADR8L	SADR8	R	8/16	00H
0F8E1H	SA-ADC result register 8H	SADR8H		R	8	00H
0F8E2H	SA-ADC result register 9L	SADR9L	SADR9	R	8/16	00H
0F8E3H	SA-ADC result register 9H	SADR9H		R	8	00H
0F8E4H	SA-ADC result register AL	SADRAL	SADRA	R	8/16	00H
0F8E5H	SA-ADC result register AH	SADRAH		R	8	00H
0F8E6H	SA-ADC result register BL	SADRBL	SADRB	R	8/16	00H
0F8E7H	SA-ADC result register BH	SADRBH		R	8	00H
0F8F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F8F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F8F2H	SA-ADC mode register 0	SADMOD0	SADMOD	R/W	8	00H
0F8F3H	SA-ADC mode register 1	SADMOD1		R/W	8	00H

24.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F8D0H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR01	SAR00	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0L is updated after A/D conversion.

Description of bits

- **SAR01-SAR00** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 0.

24.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F8D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04	SAR03	SAR02
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0H is updated after A/D conversion.

Description of bits

- **SAR09-SAR02** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 0.

24.2.4 SA-ADC Result Register 1L (SADR1L)

Address: 0F8D2H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1L	SAR11	SAR10	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR1L is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1L is updated after A/D conversion.

Description of bits

- **SAR11-SAR10** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 1.

24.2.5 SA-ADC Result Register 1H (SADR1H)

Address: 0F8D3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1H	SAR19	SAR18	SAR17	SAR16	SAR15	SAR14	SAR13	SAR12
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1H is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1H is updated after A/D conversion.

Description of bits

- **SAR19-SAR12** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 1.

24.2.6 SA-ADC Result Register 2L (SADR2L)

Address: 0F8D4H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2L	SAR21	SAR20	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR2L is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2L is updated after A/D conversion.

Description of bits

- **SAR21-SAR20** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 2.

24.2.7 SA-ADC Result Register 2H (SADR2H)

Address: 0F8D5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2H	SAR29	SAR28	SAR27	SAR26	SAR25	SAR24	SAR23	SAR22
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2H is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2H is updated after A/D conversion.

Description of bits

- **SAR29-SAR22** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 2.

24.2.8 SA-ADC Result Register 3L (SADR3L)

Address: 0F8D6H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3L	SAR31	SAR30	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR3L is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3L is updated after A/D conversion.

Description of bits

- **SAR31-SAR30** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 3.

24.2.9 SA-ADC Result Register 3H (SADR3H)

Address: 0F8D7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3H	SAR39	SAR38	SAR37	SAR36	SAR35	SAR34	SAR33	SAR32
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3H is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3H is updated after A/D conversion.

Description of bits

- **SAR39-SAR32** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 3.

24.2.10 SA-ADC Result Register 4L (SADR4L)

Address: 0F8D8H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4L	SAR41	SAR40	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR4L is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4L is updated after A/D conversion.

Description of bits

- **SAR41-SAR40** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 4.

24.2.11 SA-ADC Result Register 4H (SADR4H)

Address: 0F8D9H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4H	SAR49	SAR48	SAR47	SAR46	SAR45	SAR44	SAR43	SAR42
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR4H is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4H is updated after A/D conversion.

Description of bits

- **SAR49-SAR42** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 4.

24.2.12 SA-ADC Result Register 5L (SADR5L)

Address: 0F8DAH
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5L	SAR51	SAR50	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR5L is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5L is updated after A/D conversion.

Description of bits

- **SAR51-SAR50** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 5.

24.2.13 SA-ADC Result Register 5H (SADR5H)

Address: 0F8DBH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5H	SAR59	SAR58	SAR57	SAR56	SAR55	SAR54	SAR53	SAR52
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR5H is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5H is updated after A/D conversion.

Description of bits

- **SAR59-SAR52** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 5.

24.2.14 SA-ADC Result Register 6L (SADR6L)

Address: 0F8DCH
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6L	SAR61	SAR60	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR6L is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6L is updated after A/D conversion.

Description of bits

- **SAR61-SAR60** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 6.

24.2.15 SA-ADC Result Register 6H (SADR6H)

Address: 0F8DDH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6H	SAR69	SAR68	SAR67	SAR66	SAR65	SAR64	SAR63	SAR62
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR6H is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6H is updated after A/D conversion.

Description of bits

- **SAR69-SAR62** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 6.

24.2.16 SA-ADC Result Register 7L (SADR7L)

Address: 0F8DEH
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7L	SAR71	SAR70	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR7L is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7L is updated after A/D conversion.

Description of bits

- **SAR71-SAR70** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 7.

24.2.17 SA-ADC Result Register 7H (SADR7H)

Address: 0F8DFH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7H	SAR79	SAR78	SAR77	SAR76	SAR75	SAR74	SAR73	SAR72
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR7H is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7H is updated after A/D conversion.

Description of bits

- **SAR79-SAR72** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 7.

24.2.18 SA-ADC Result Register 8L (SADR8L)

Address: 0F8E0H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR8L	SAR81	SAR80	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR8L is a special function register (SFR) used to store SA-ADC conversion results on channel 8.
SADR8L is updated after A/D conversion.

Description of bits

- **SAR81-SAR80** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 8.

24.2.19 SA-ADC Result Register 8H (SADR8H)

Address: 0F8E1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR8H	SAR89	SAR88	SAR87	SAR86	SAR85	SAR84	SAR83	SAR82
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR8H is a special function register (SFR) used to store SA-ADC conversion results on channel 8.
SADR8H is updated after A/D conversion.

Description of bits

- **SAR89-SAR82** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 8.

24.2.20 SA-ADC Result Register 9L (SADR9L)

Address: 0F8E2H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR9L	SAR91	SAR90	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADR9L is a special function register (SFR) used to store SA-ADC conversion results on channel 9.
SADR9L is updated after A/D conversion.

Description of bits

- **SAR91-SAR90** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 9.

24.2.21 SA-ADC Result Register 9H (SADR9H)

Address: 0F8E3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR9H	SAR99	SAR98	SAR97	SAR96	SAR95	SAR94	SAR93	SAR92
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR9H is a special function register (SFR) used to store SA-ADC conversion results on channel 9.
SADR9H is updated after A/D conversion.

Description of bits

- **SAR99-SAR92** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 9.

24.2.22 SA-ADC Result Register AL (SADRAL)

Address: 0F8E4H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRAL	SARA1	SARA0	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADRAL is a special function register (SFR) used to store SA-ADC conversion results on channel A.
SADRAL is updated after A/D conversion.

Description of bits

- **SARA1-SARA0** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel A.

24.2.23 SA-ADC Result Register AH (SADRAH)

Address: 0F8E5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRAH	SARA9	SARA8	SARA7	SARA6	SARA5	SARA4	SARA3	SARA2
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRAH is a special function register (SFR) used to store SA-ADC conversion results on channel A.
SADRAH is updated after A/D conversion.

Description of bits

- **SARA9-SARA2** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel A.

24.2.24 SA-ADC Result Register BL (SADRBL)

Address: 0F8E6H
Access: R
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRBL	SARB1	SARB0	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	X	X	0	0	0	0

SADRBL is a special function register (SFR) used to store SA-ADC conversion results on channel B.
SADRBL is updated after A/D conversion.

Description of bits

- **SARB1-SARB0** (bits 7-6)
  These bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel B.

24.2.25 SA-ADC Result Register BH (SADRBH)

Address: 0F8E7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADRBH	SARB9	SARB8	SARB7	SARB6	SARB5	SARB4	SARB3	SARB2
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADRBH is a special function register (SFR) used to store SA-ADC conversion results on channel B.
SADRBH is updated after A/D conversion.

Description of bits

- **SARB9-SARB2** (bits 7-0)
  These bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel B.

24.2.26 SA-ADC Control Register 0 (SADCON0)

Address: 0F8F0H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON0	-	-	-	-	-	-	SACK	SALP
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

Description of bits

- **SALP** (bit 0)
  This bit is used to select whether A/D conversion is performed once only for each channel or consecutively. When this bit is set to "0", A/D conversion is performed once only for each channel and when it is set to "1", A/D conversion is performed consecutively according to the settings of the SA-ADC mode register 0 (SADMOD0).

SALP	Description
0	Single A/D conversion only (initial value)
1	Consecutive A/D conversion

- **SACK** (bit 1)
  This bit is used to select the conversion time per channel. When this bit is set to "0", the conversion time per channel is set to about 13.5 μs. This is effective only in PLL oscillation mode. When this bit is set to "1", the conversion time per channel is set to about 43 μs.

SACK	Description
0	Conversion time: about 13.5 μs/1ch (only in PLL oscillation mode)(initial value)
1	Conversion time: about 43 μs/1ch

[Note]
Set the SA-ADC mode register 0 before starting the conversion.

24.2.27 SA-ADC Control Register 1 (SADCON1)

Address: 0F8F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	-	-	-	-	-	-	-	SARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

Description of bits

- **SARUN** (bit 0)
  This bit is used to start or stop SA-ADC conversion. Set this bit to "1" to start A/D conversion, and "0" to stop it.
  When SALP of SADCON0 is "0" and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to "0".

SARUN	Description
0	Stops conversion (initial value)
1	Starts conversion

[Note]
Use the SA-ADC with high-speed clock oscillation (OSCLK) enabled in the frequency control register (FCON0).
Do not start A/D conversion in the state in which all of the SACHB to SACH0 bits of SA-ADC mode register 0, 1 (SADMOD0,1) are "0". When A/D conversion is started in this state, the SARUN bit remains "0", and A/D conversion is not started. Set SACHB to SACH0 of the SA-ADC mode register (SADMOD) before starting the conversion.

24.2.28 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F8F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	SACH7	SACH6	SACH5	SACH4	SACH3	SACH2	SACH1	SACH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

Description of bits

- **SACH7** (bit 7)

SACH7	Description
0	Stops conversion on channel 7 (initial value)
1	Performs conversion on channel 7.

- **SACH6** (bit 6)

SACH6	Description
0	Stops conversion on channel 6 (initial value)
1	Performs conversion on channel 6.

- **SACH5** (bit 5)

SACH5	Description
0	Stops conversion on channel 5 (initial value)
1	Performs conversion on channel 5.

- **SACH4** (bit 4)

SACH4	Description
0	Stops conversion on channel 4 (initial value)
1	Performs conversion on channel 4.

- **SACH3** (bit 3)

SACH3	Description
0	Stops conversion on channel 3 (initial value)
1	Performs conversion on channel 3.

- **SACH2** (bit 2)

SACH2	Description
0	Stops conversion on channel 2 (initial value)
1	Performs conversion on channel 2.

- **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1 (initial value)
1	Performs conversion on channel 1.

- **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0 (initial value)
1	Performs conversion on channel 0.

The SACH7 to SACH0 bits are used to select channel(s) on which A/D conversion is performed.
If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

[Note]
Do not start A/D conversion in the state in which all of the SACHB to SACH0 bits of SA-ADC mode register 0, 1 (SADMOD0,1) are "0". When A/D conversion is started in this state, the SARUN bit remains "0", and A/D conversion is not started. Set SACHB to SACH0 of the SA-ADC mode register (SADMOD) before starting the conversion.

24.2.29 SA-ADC Mode Register 1 (SADMOD1)

Address: 0F8F3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD1	-	-	-	-	SACHB	SACHA	SACH9	SACH8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

Description of bits

- **SACHB** (bit 3)

SACHB	Description
0	Stops conversion on channel B (initial value)
1	Performs conversion on channel B.

- **SACHA** (bit 2)

SACHA	Description
0	Stops conversion on channel A (initial value)
1	Performs conversion on channel A.

- **SACH9** (bit 1)

SACH9	Description
0	Stops conversion on channel 9 (initial value)
1	Performs conversion on channel 9.

- **SACH8** (bit 0)

SACH8	Description
0	Stops conversion on channel 8 (initial value)
1	Performs conversion on channel 8.

The SACH8 to SACHB bits are used to select channel(s) on which A/D conversion is performed.

[Note]
Do not start A/D conversion in the state in which all of the SACHB to SACH0 bits of SA-ADC mode register 0, 1 (SADMOD0,1) are "0". When A/D conversion is started in this state, the SARUN bit remains "0", and A/D conversion is not started. Set SACHB to SACH0 of the SA-ADC mode register (SADMOD) before starting the conversion.

24.3 Description of Operation

24.3.1 Setting of A/D Conversion Channels

According to the setting of SA-ADC mode register (SADMOD), A/D conversion is performed as shown below and A/D conversion results are stored in the SA-ADC result register.

SA-ADC mode registers 0/1					SA-ADC result register					Remarks
SACHB	•••	SACH2	SACH1	SACH0	SADRB	•••	SADR2	SADR1	SADR0	
0	0	0	0	0						Do not use
0	0	0	0	1					AIN0	
0	0	0	1	0				AIN1		
0	0	0	1	1				AIN1	AIN0	
0	0	1	0	0			AIN2			
0	0	1	0	1			AIN2		AIN0	
0	0	1	1	0			AIN2	AIN1		
0	0	1	1	1			AIN2	AIN1	AIN0	
1	0	0	0	0	AIN11					
1	0	0	0	1	AIN11				AIN0	
1	0	0	1	0	AIN11			AIN1		
1	0	0	1	1	AIN11			AIN1	AIN0	
1	0	1	0	0	AIN11		AIN2			
1	0	1	0	1	AIN11		AIN2		AIN0	
1	0	1	1	0	AIN11		AIN2	AIN1		
1	0	1	1	1	AIN11		AIN2	AIN1	AIN0	

The values of the result register for the sections with a slash mark remain unchanged.
Do not start A/D conversion when all of bit 7 (SACH7) to bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) and bit 3 (SACHB) to bit 0 (SACH8) of the SA-ADC mode register 1 (SADMOD1) are "0". When A/D conversion is started in this state, the SARUN bit remains "0", and A/D conversion is not started. Set SACHB to SACH0 of the SA-ADC mode register 0, 1 (SADMOD0, 1) before starting the conversion.

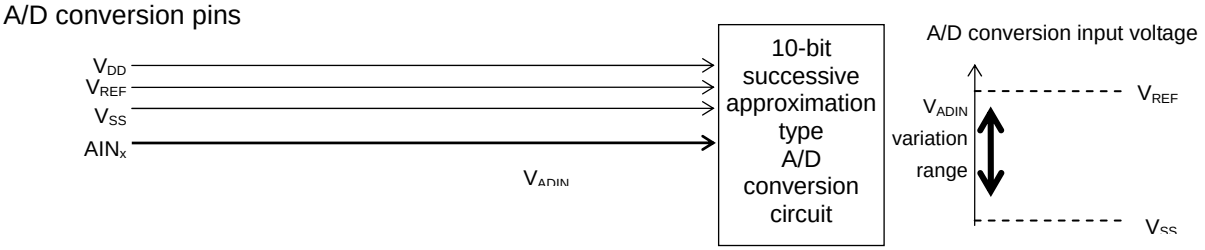


Figure 24-2 A/D Conversion Pins and Conversion Range

24.3.2 Operation of the Successive Approximation Type A/D Converter

For direct input, operate SA-ADC in the following procedure.

1. Before starting SA-ADC, start oscillation of the high-speed clock (OSCLK) and wait until the oscillator settles.
2. Set the SA-ADC mode register 0 (SADMOD0) and SA-ADC mode register 1 (SADMOD1).
3. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the lower channel number that is selected in the SA-ADC mode registers (SADMOD0, SADMOD1).
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRnL, SADRnH), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.
5. Finally, using bit 0 (SALP) of the SADCON0 register, it is possible to select whether A/D conversion is terminated (SARUN bit is "0") or A/D conversion is automatically restarted at termination of A/D conversion of the last channel.

Even if the channel is switched during A/D conversion, it is held as selected at the start of A/D conversion until an A/D conversion termination interrupt occurs.
Figure 24-3 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

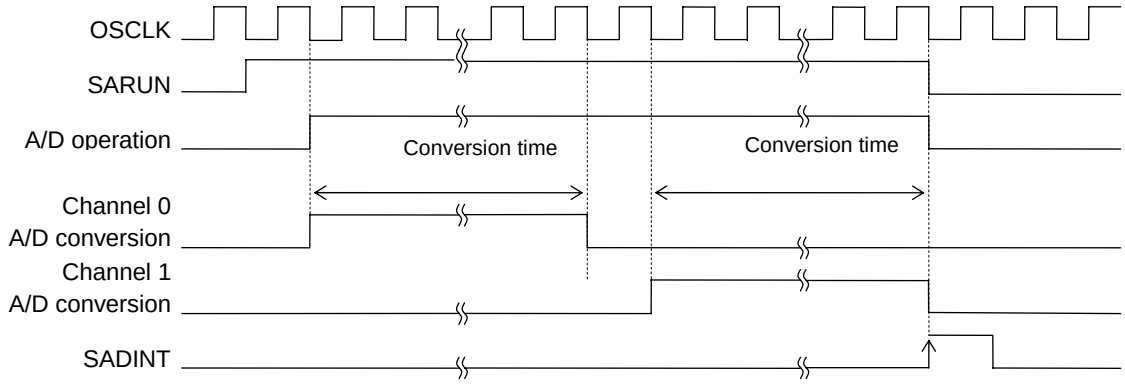


Figure 24-3 SA-ADC Operation Timing at Direct Input

Chapter 25 Analogue Comparator

25 Analogue Comparator

25.1 General Description

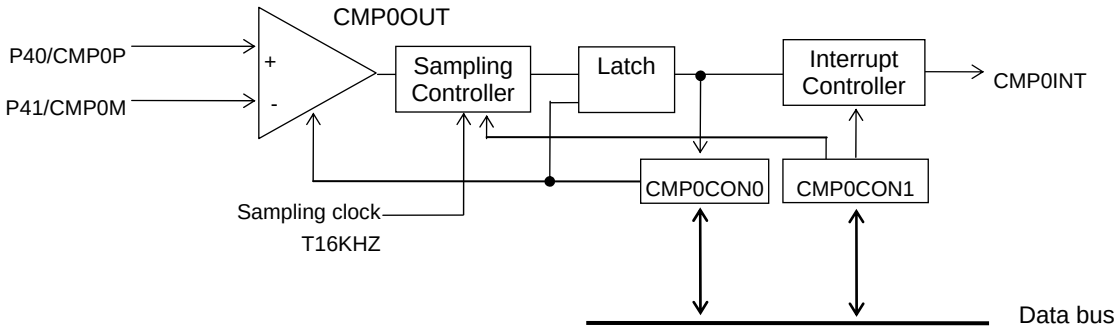
This LSI includes 1 channels of analogue comparator.
Voltage comparison between two pins (CMP0P, CMP0M) that are input to the comparator is available.

25.1.1 Features

- The comparator output can generate an interrupt.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for interrupt.
- Allows selection of with/without sampling. (Sampling frequency: T16KHZ)
- The last status of comparator output (CMP0D) remains after the comparator is deactivated.

25.1.2 Configuration

Figure 25-1 shows the configuration of the comparator.



CMP0CON0: Comparator control register 0
CMP0CON1: Comparator control register 1

Figure 25-1 Configuration of Comparator

25.1.3 List of Pins

Pin name	I/O	Function
P40/CMP0M	I	I/O port, Analogue comparator 0 non-inverting input
P41/CMP0P	I	I/O port, Analogue comparator 0 inverting input

[Note]

- To use the analogue comparator, set the port as high-impedance output in advance. For the setting method, see Chapter 19, "Port 4".

25.2 Description of Registers

25.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F950H	Comparator 0 control register 0	CMP0CON0	CMP0CON	R/W	8/16	00H
0F951H	Comparator 0 control register 1	CMP0CON1		R/W	8	00H

25.2.2 Comparator 0 Control Register 0 (CMP0CON0)

Address: 0F950H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON0	—	—	—	—	—	—	CMP0D	CMP0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON0 is a special function register (SFR) to control the comparator.

Description of bits

- **CMP0D** (bit 1)
  CMP0D indicates the status of the comparator output (CMP0OUT in Figure 25-1).
  It is set to "1" when the CMP0P pin voltage is higher than the CMP0M pin voltage (CMP0P>CMP0M). It is set to "0" when the CMP0P pin voltage is lower than the CMP0M pin voltage (CMP0P<CMP0M).
  It holds the last status even after the comparator is turned off (CMP0EN is set to "0").

CMP0D	Description
0	CMP0P < CMP0M (initial value)
1	CMP0P > CMP0M

- **CMP0EN** (bit 0)
  The CMP0EN bit is used to control ON/OFF of the comparator.
  When CMP0EN is set to "1", the comparator is turned on. When it is set to "0", the comparator is turned off.

CMP0EN	Description
0	Comparator OFF (initial value)
1	Comparator ON

25.2.3 Comparator 0 Control Register 1 (CMP0CON1)

Address: 0F951H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON1	—	—	—	—	—	CMP0SM0	CMP0E1	CMP0E0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON1 is a special function register (SFR) to control the comparator interrupt.

Description of bits

- **CMP0SM0** (bit 2)
  The CMP0SM0 bit is used to select with/without sampling for the comparator comparison. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

CMP0SM0	Description
0	Detects without sampling (initial value)
1	Detects with sampling

- **CMP0E0, CMP0E1** (bit 0, bit 1)
  The CMP0E0 and CMP0E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.

CMP0E1	CMP0E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt
1	0	Rising-edge interrupt
1	1	Both-edge interrupt

[Note]

- In STOP mode, no sampling is performed regardless of the value set in CMP0SM0 since the sampling clock T16KHZ stops.

25.3 Description of Operation

25.3.1 Comparator Functions

The comparator compares the input voltages of the CMP0P and CMP0M pins to output the result to the CMP0D bit of the comparator n control register 0 (CMP0CON0).
To use the comparator, set the port as high-impedance output in advance. For the setting method, see Chapter 19, "Port 4".
CMP0EN of CMP0CON0 is controlled by the comparator enable. When CMP0EN is set to "1", the comparator is activated (ON). When CMP0EN is set to "0", the comparator is deactivated (OFF) and has no current consumption.
The comparison result is read from the CMP0D bit. When CMP0D is "1", it indicates that the input voltage of the CMP0P pin is higher than that of the CMP0M pin. When CMP0D is "0", it indicates that the input voltage of the CMP0P pin is lower than that of the CMP0M pin.
The comparator requires a settling time. Read the CMP0D bit 100 μs or longer after the CMP0EN bit is set to "1".
Figure 25-2 shows an example of the operation timing diagram.

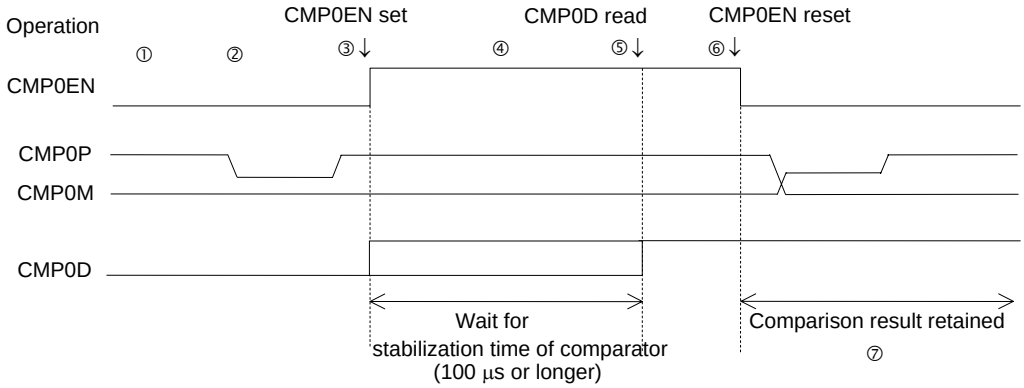


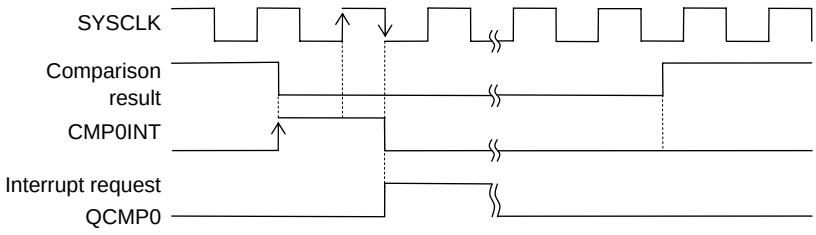
Figure 25-2 Example of Operation Timing Diagram

The operations in Figure 25-2 are described below.

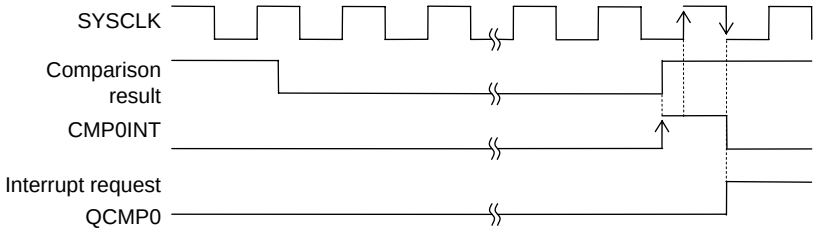
① Set the port as high-impedance output.
② Select the interrupt mode by CMP0CON1.
③ Set CMP0EN to "1" to turn on the comparator.
④ Wait the settling time (100 μs or longer) of the comparator.
⑤ Read the comparison result (CMP0D).
⑥ Set CMP0EN to "0" to turn off the comparator. At the same time, the result is retained.
⑦ CMP0D can be read after CMP0EN is set to "0" because CMP0D holds the comparison result at the time when CMP0EN is set to "0".

25.3.2 Interrupt Request

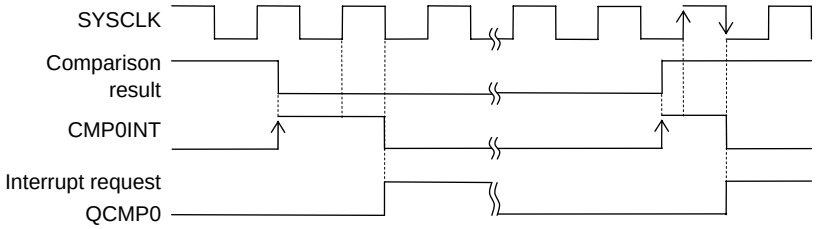
When an interrupt edge selected by the comparator control register 1 (CMP0CON1) occurs on the comparison result of the comparator, a comparator interrupt (CMP0INT) is generated. For the comparator interrupt, the edge can be selected. Figure 25-3 shows the interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



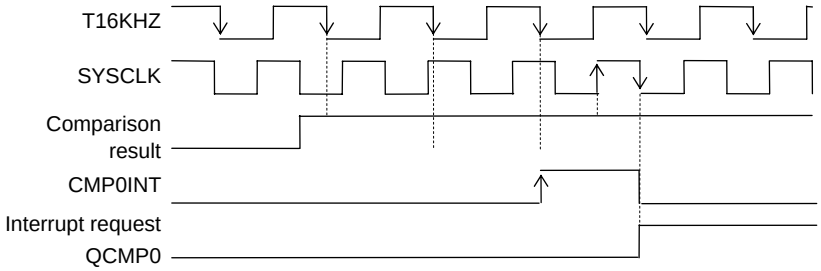
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 25-3 Comparator Interrupt Generation Timing

Chapter 26 LLD (Low Level Detector)

26 LLD (Low Level Detector)

26.1 General Description

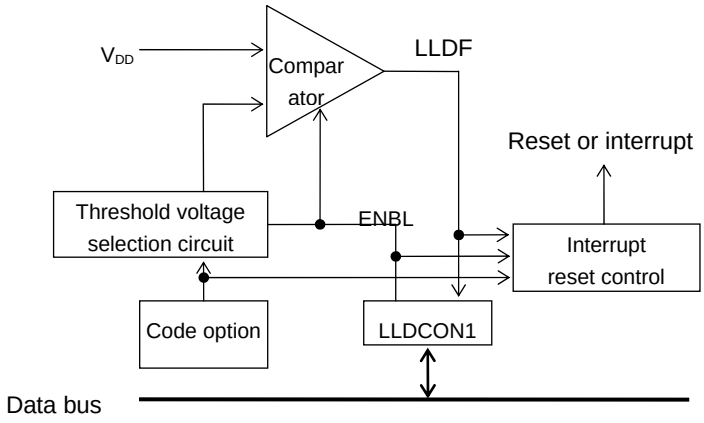
This LSI includes a Low Level Detector (LLD).
Four levels of threshold voltage can be selected by setting Code-Option.
The operation (reset or interrupt) to be performed when the voltage drops below the threshold can be selected by setting Code-Option.
For Code-Option, see Chapter 30, "Code-Option".

26.1.1 Features

- Threshold voltage: One of the four levels can be selected
- Reset or interrupt can be selected
- Hysteresis width: 80 mV (Typ.)

26.1.2 Configuration

LLD consists of the comparator and the threshold voltage select circuit.
Figure 26-1 shows the configuration of the LLD circuit.



LLDCON1 : LLD circuit control register 1

Figure 26-1 Configuration of LLD Circuit

26.2 Description of Registers

26.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F8C1H	LLD circuit control register 1	LLDCON1	-	R/W	8	00H

26.2.2 LLD Circuit Control Register 1 (LLDCON1)

Address: 0F8C1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LLDCON1	—	—	—	—	—	—	LLDF	ENBL
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

LLDCON1 is a special function register (SFR) used to control the LLD circuit.

Description of bits

- **LLDF** (bit 1)
  LLDF is the judgment result flag of the LLD circuit.
  It is set to "1" when the power supply voltage (V_{DD}) is lower than the threshold voltage (V_{CMP}) selected by LD1 to LD0 bits, or "0" otherwise.

LLDF	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

- **ENBL** (bit 0)
  The ENBL bit is used to control ON/OFF of the LLD circuit.
  The LLD circuit is turned on when ENBL is set to "1", and off when "0".

ENBL	Description
0	LLD circuit OFF (initial value)
1	LLD circuit ON

26.3 Description of Operation

26.3.1 Threshold Voltage

The value of the threshold voltage (V_{CMP}) can be selected by Code-Option.
Table 26-1 shows the threshold voltages and hysteresis width, and Table 26-2 shows the LLD operation selection.

Table 26-1 Threshold Voltages and Accuracy

Code option (FLASH address: *)		Threshold voltage V_{CMP}	Hysteresis width Ta=25°C
Bit 1	Bit 0		
LLD1	LLD0		
0	0	1.90V	80mV (Typ.)
0	1	2.55V	
1	0	3.70V	
1	1	4.20V	

Table 26-2 LLD Operation Selection

Code option (FLASH address: *)	LLD operation
Bit 2	
LLDSEL	
0	Interrupt output
1	Reset

* : The FLASH address of the code option varies depending on the product.
See the Code-Option data format described in Section 30.3.1.

26.3.2 Operation of LLD Circuit

Activation (ON) and deactivation (OFF) of LLD circuit are controlled by setting the ENBL bit of the LLD circuit control register 1 (LLDCON1), and the result of comparison of the power supply voltage (V_{DD}) to the threshold voltage is output to the LLDF bit of LLDCON1.
ENBL is the enable control bit of the LLD circuit. When it is set to "1", the circuit is activated (ON). When ENBL is set to "0", the LLD circuit is deactivated (OFF) and has no current consumption.
LLDF is the judgment result flag. When LLDF is "1", it indicates the power supply voltage (V_{DD}) is lower than the threshold voltage. When LLDF is "0", it indicates the power supply voltage (V_{DD}) is higher than the threshold voltage.
The judgment circuit of the LLD circuit requires a settling time. Read the LLDF bit 100 µs or longer after the ENBL bit is set to "1".
Figure 26-2 shows an example of the operation timing diagram.

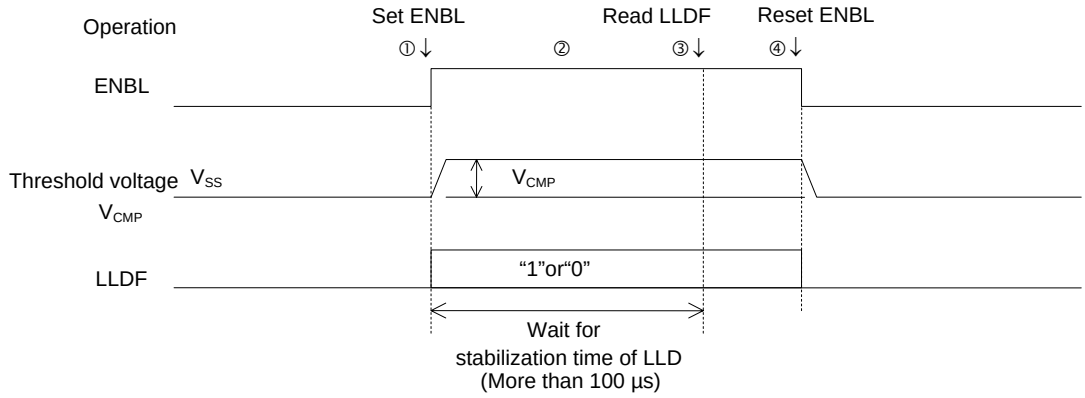


Figure 26-2 Example of Operation Timing Diagram

The operations in Figure 26-2 are described below.

① Set ENBL to "1" to turn on the LLD circuit.
② Wait the settling time (100 µs or longer) of the LLD detection circuit.
③ Read the judgment result flag (LLDF).
④ Set ENBL bit to "0".

[Note]
Select the threshold voltage (VCMP) when the ENBL bit is "0".

Chapter 27 Power Supply Circuit

27 Power Supply Circuit

27.1 General Description

This LSI includes a voltage regulator circuit for internal logic (VRL).
The VRL outputs the operating voltage, V_{DDL}, of the internal logic circuit, program memory, RAM, etc.

27.1.1 Features

- The VRL outputs the operating voltage, V_{DDL}, of the internal logic circuit, program memory, RAM, etc.

27.1.2 Configuration

Figure 27-1 shows the configuration of the power supply circuit.

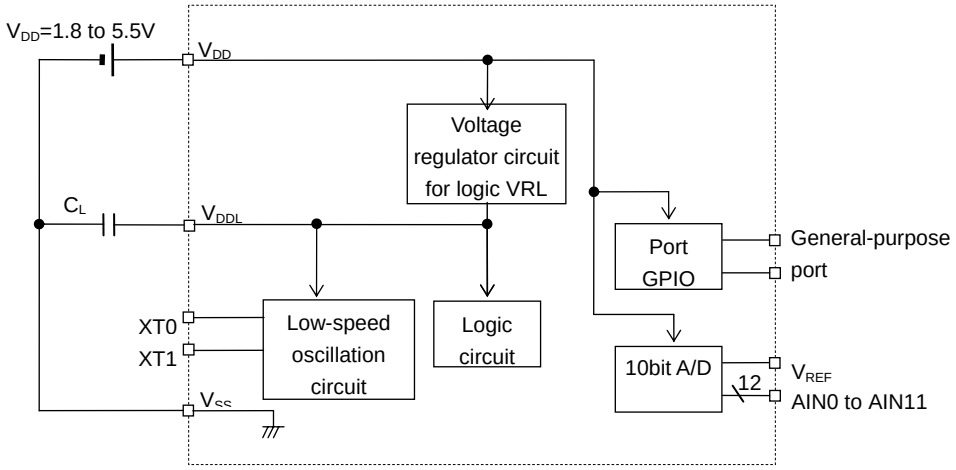


Figure 27-1 Configuration of Power Supply Circuit

27.1.3 List of Pins

Pin name	I/O	Function
V_{DDL}	-	Positive power supply pin for the internal logic circuits

27.2 Description of Operation

After power-on, the V_{DDL} voltage becomes approximately 1.5 V in any operation mode.

Figure 27-2 shows the operation waveforms of the power supply circuit.

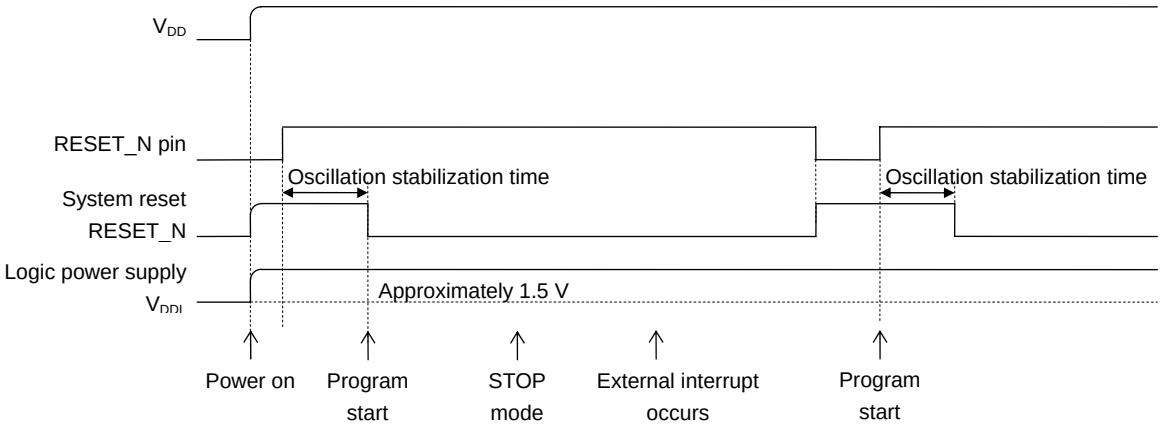


Figure 27-2 Operation Waveform of Power Supply Circuit

Chapter 28 On-chip Debug Function

28 On-chip Debug Function

28.1 General Description

This LSI has an on-chip debug function allowing Flash memory rewriting.
The on-chip debug emulator (µEASE) is connected to this LSI to perform the on-chip debug function.

28.2 How to connect the On-Chip Debug Emulator

Figure 28-1 shows connection to the on-chip debug emulator (µEASE).
For on-chip debug emulator, see "µEASE Connection Manual" and "µEASE User's Manual".

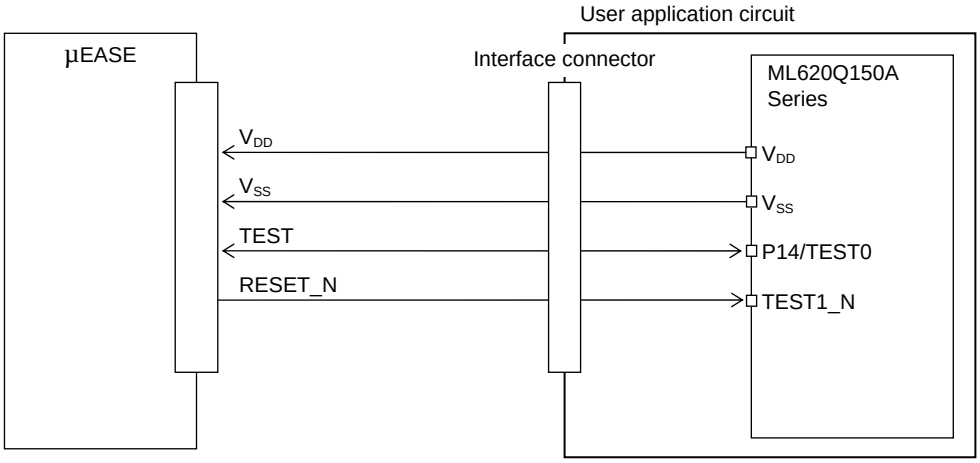


Figure 28-1 Connection to On-chip Debug Emulator (µEASE)

[Note]

• Do not program ML620Q150A series with an application program code that sets P14IDR bit of P1DIR register to"0". Because the program code is executed before µEASE accesses to ML620Q150A series, P14/TEST0 pin gets output mode and from then on, the LSI cannot enter the on-chip debug mode. Notice that µEASE cannot initialize the P14DIR bit.

• Please do not apply LSIs being used for debugging to mass production.

• When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 4 pins (V_{DD}, V_{SS}, P14/TEST0, and TEST1_N) required for connection to the on-chip debug emulator can be connected.

• "3.0V to 5.5V" has to be supplied to V_{DD} while debugging and writing flash.

For details, see "µEASE User's Manual" and "µEASE Target Connection Manual".

Chapter 29 Flash Memory Rewrite Function

29 FLASH Memory Rewrite Function

29.1 General Description

This LSI includes the ISP (In System Programming) function and boot area remap function that rewrite the content of the flash memory (program memory space) using a special function register (SFR) programmatically.

29.1.1 Features

- Supports 1-word write function
- Two erase types
  1. Block erase (erase unit: 8 Kbytes)
     ML620Q151A/ML620Q154A/ML620Q157A: Erasable range (0:0000h to 0:7FFFh, 7:0000h to 7:07FFh)
     ML620Q152A/ML620Q155A/ML620Q158A: Erasable range (0:0000h to 0:0BFFFh, 7:0000h to 7:07FFh)
     ML620Q153A/ML620Q156A/ML620Q159A: Erasable range (0:0000h to 0:0FFFFh, 7:0000h to 7:07FFh)
  2. Sector erase (erase unit: 1 Kbytes)
     ML620Q151A/ML620Q154A/ML620Q157A: Erasable range (0:0000h to 0:7FFFh, 7:0000h to 7:07FFh)
     ML620Q152A/ML620Q155A/ML620Q158A: Erasable range (0:0000h to 0:0BFFFh, 7:0000h to 7:07FFh)
     ML620Q153A/ML620Q156A/ML620Q159A: Erasable range (0:0000h to 0:0FFFFh, 7:0000h to 7:07FFh)

- Rewrite count of flash memory.
  This depends on the following rewrite addresses.

ML620Q151A/ML620Q154A/ML620Q157A :

Rewrite address	Rewrite count
0:0000h to 0:7FFFh*1	100
7:0000h to 7:07FFh	10000

ML620Q152A/ML620Q155A/ML620Q158A :

Rewrite address	Rewrite count
0:0000h to 0:0BFFFh*1	100
7:0000h to 7:07FFh	10000

ML620Q153A/ML620Q156A/ML620Q159A :

Rewrite address	Rewrite count
0:0000h to 0:0FFFFh*1	100
7:0000h to 7:07FFh	10000

[Note]

*1 ML620Q151A/ML620Q154A/ML620Q157A: The test data area (0:7C00h to 0FFFFh) is excluded.
ML620Q152A/ML620Q155A/ML620Q158A: The test data area (0:0BC00h to 0FFFFh) is excluded.
ML620Q153A/ML620Q156A/ML620Q159A: The test data area (0:0FC00h to 0FFFFh) is excluded.

- Software remap function.
  The boot area (0:0000h to 0:0FFFh) of 4 Kbytes can be remapped by the REMAPADD register.

29.2 Description of Registers

29.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	—	W	8	00H
0F0E6H	Flash acceptor	FLASHACP	—	W	8	00H
0F0E8H	Flash segment register	FLASHSEG	—	R/W	8	00H
0F0EAH	Flash self register	FLASHSLF	—	R/W	8	00H
0F0ECH	Remap address register	REMAPADD	—	R/W	8	00H

29.2.2 Flash Address Register (FLASHAL, FLASHAH)

Address: 0F0E0H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAL	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAH	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHAL and FLASHAH are special function registers (SFRs) used to set the flash memory rewrite addresses.

Description of bits

- **FA7-FA0** (bits 7-0)
  The FA7 to FA0 bits are used to set the lower address for 1-word write.
  Note that the bit 0 is fixed to 0 and cannot be written.

- **FA15-FA8** (bits 7-0)
  The FA15 to FA8 bits are used to set the upper address for block erase, sector erase, or 1-word write.
  At block erase, the block specified by FA15 to FA14 is erased.
  At sector erase, the sector specified in FA15 to FA9 is erased.

Table 29-1 and Table 29-2 show the address setting values at block erase and sector erase for ML620Q151A/ML620Q154A/ML620Q157A, respectively.
Table 29-3 and Table 29-4 show the address setting values at block erase and sector erase for ML620Q152A/ML620Q155A/ML620Q158A, respectively.
Table 29-5 and Table 29-6 show the address setting values at block erase and sector erase for ML620Q153A/ML620Q156A/ML620Q159A, respectively.

[Note]
Specify the addresses before remapping in this register even for software remap. For the remap function, see Section 29.3.4, "Boot Area Remap Function by Software".

Table 29-1 Address Setting Values for Block Erase (ML620Q151A/ML620Q154A/ML620Q157A)

Area for block erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:1FFFH	0	0	0	0	0	0	0	0	0	0	0
	0:2000H	to	0:3FFFH	0	0	0	0	0	1	0	0	0	0	0
	0:4000H	to	0:5FFFH	0	0	0	0	1	0	0	0	0	0	0
	0:6000H	to	0:7FFFH	0	0	0	0	1	1	0	0	0	0	0
Segment 7	7:0000H	to	7:07FFH	1	1	1	0	0	0	0	0	0	0	0

The unit of block is 8 KB for the segment 0 and 2 KB for the segment 7.
Therefore, the total number of blocks is 5, including 4 blocks in the segment 0 and 1 block in the segment 7.

Table 29-2 Address Setting Values for Sector Erase (ML620Q151A/ML620Q154A/ML620Q157A)

Area for sector erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:03FFH	0	0	0	0	0	0	0	0	0	0	0
	0:0400H	to	0:07FFH	0	0	0	0	0	0	0	0	1	0	0
	0:0800H	to	0:0BFFH	0	0	0	0	0	0	0	1	0	0	0
	0:0C00H	to	0:0FFFH	0	0	0	0	0	0	0	1	1	0	0
	0:1000H	to	0:13FFH	0	0	0	0	0	0	1	0	0	0	0
	0:1400H	to	0:17FFH	0	0	0	0	0	0	1	0	1	0	0
	0:1800H	to	0:1BFFH	0	0	0	0	0	0	1	1	0	0	0
	0:1C00H	to	0:1FFFH	0	0	0	0	0	0	1	1	1	0	0
		⋮												
	0:6000H	to	0:63FFH	0	0	0	0	1	1	0	0	0	0	0
	0:6400H	to	0:67FFH	0	0	0	0	1	1	0	0	1	0	0
	0:6800H	to	0:6BFFH	0	0	0	0	1	1	0	1	0	0	0
	0:6C00H	to	0:6FFFH	0	0	0	0	1	1	0	1	1	0	0
	0:7000H	to	0:73FFH	0	0	0	0	1	1	1	0	0	0	0
	0:7400H	to	0:77FFH	0	0	0	0	1	1	1	0	1	0	0
	0:7800H	to	0:7BFFH	0	0	0	0	1	1	1	1	0	0	0
	0:7C00H	to	0:7FFFH	0	0	0	0	1	1	1	1	1	0	0
Segment 7	7:0000H	to	7:03FFH	1	1	1	0	0	0	0	0	0	0	0
	7:0400H	to	7:07FFH	1	1	1	0	0	0	0	0	1	0	0

The unit of sector is 1 KB.
Therefore, the total number of sectors is 34, including 32 sectors in the segment 0 and 2 sectors in the segment 7.

Table 29-3 Address Setting Values for Block Erase (ML620Q152A/ML620Q155A/ML620Q158A)

Area for block erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:1FFFH	0	0	0	0	0	0	0	0	0	0	0
	0:2000H	to	0:3FFFH	0	0	0	0	0	1	0	0	0	0	0
	0:4000H	to	0:5FFFH	0	0	0	0	1	0	0	0	0	0	0
	0:6000H	to	0:7FFFH	0	0	0	0	1	1	0	0	0	0	0
	0:8000H	to	0:9FFFH	0	0	0	1	0	0	0	0	0	0	0
	0:0A000H	to	0:0BFFFH	0	0	0	1	0	1	0	0	0	0	0
Segment 7	7:0000H	to	7:07FFH	1	1	1	0	0	0	0	0	0	0	0

The unit of block is 8 KB for the segment 0 and 2 KB for the segment 7.
Therefore, the total number of blocks is 7, including 6 blocks in the segment 0 and 1 block in the segment 7.

Table 29-4 Address Setting Values for Sector Erase (ML620Q152A/ML620Q155A/ML620Q158A)

Area for sector erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:03FFH	0	0	0	0	0	0	0	0	0	0	0
	0:0400H	to	0:07FFH	0	0	0	0	0	0	0	0	1	0	0
	0:0800H	to	0:0BFFH	0	0	0	0	0	0	0	1	0	0	0
	0:0C00H	to	0:0FFFH	0	0	0	0	0	0	0	1	1	0	0
	0:1000H	to	0:13FFH	0	0	0	0	0	0	1	0	0	0	0
	0:1400H	to	0:17FFH	0	0	0	0	0	0	1	0	1	0	0
	0:1800H	to	0:1BFFH	0	0	0	0	0	0	1	1	0	0	0
	0:1C00H	to	0:1FFFH	0	0	0	0	0	0	1	1	1	0	0
		:												
		:												
	0:0A000H	to	0:0A3FFH	0	0	0	1	0	1	0	0	0	0	0
	0:0A400H	to	0:0A7FFH	0	0	0	1	0	1	0	0	1	0	0
	0:0A800H	to	0:0ABFFH	0	0	0	1	0	1	0	1	0	0	0
	0:0AC00H	to	0:0AFFFH	0	0	0	1	0	1	0	1	1	0	0
	0:0B000H	to	0:0B3FFH	0	0	0	1	0	1	1	0	0	0	0
	0:0B400H	to	0:0B7FFH	0	0	0	1	0	1	1	0	1	0	0
	0:0B800H	to	0:0BBFFH	0	0	0	1	0	1	1	1	0	0	0
	0:0BC00H	to	0:0BFFFH	0	0	0	1	0	1	1	1	1	0	0
Segment 7	7:0000H	to	7:03FFH	1	1	1	0	0	0	0	0	0	0	0
	7:0400H	to	7:07FFH	1	1	1	0	0	0	0	0	1	0	0

The unit of sector is 1 KB.
Therefore, the total number of sectors is 50, including 48 sectors in the segment 0 and 2 sectors in the segment 7.

Table 29-5 Address Setting Values for Block Erase (ML620Q153A/ML620Q156A/ML620Q159A)

Area for block erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:1FFFH	0	0	0	0	0	0	0	0	0	0	0
	0:2000H	to	0:3FFFH	0	0	0	0	0	1	0	0	0	0	0
	0:4000H	to	0:5FFFH	0	0	0	0	1	0	0	0	0	0	0
	0:6000H	to	0:7FFFH	0	0	0	0	1	1	0	0	0	0	0
	0:8000H	to	0:9FFFH	0	0	0	1	0	0	0	0	0	0	0
	0:A000H	to	0:BFFFH	0	0	0	1	0	1	0	0	0	0	0
	0:C000H	to	0:DFFFH	0	0	0	1	1	0	0	0	0	0	0
	0:E000H	to	0:FFFFH	0	0	0	1	1	1	0	0	0	0	0
Segment 7	7:0000H	to	7:07FFH	1	1	1	0	0	0	0	0	0	0	0

The unit of block is 8 KB for the segment 0 and 2 KB for the segment 7.
Therefore, the total number of blocks is 9, including 8 blocks in the segment 0 and 1 block in the segment 7.

Table 29-6 Address Setting Values for Sector Erase (ML620Q153A/ML620Q156A/ML620Q159A)

Area for sector erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:03FFH	0	0	0	0	0	0	0	0	0	0	0
	0:0400H	to	0:07FFH	0	0	0	0	0	0	0	0	1	0	0
	0:0800H	to	0:0BFFH	0	0	0	0	0	0	0	1	0	0	0
	0:0C00H	to	0:0FFFH	0	0	0	0	0	0	0	1	1	0	0
	0:1000H	to	0:13FFH	0	0	0	0	0	0	1	0	0	0	0
	0:1400H	to	0:17FFH	0	0	0	0	0	0	1	0	1	0	0
	0:1800H	to	0:1BFFH	0	0	0	0	0	0	1	1	0	0	0
	0:1C00H	to	0:1FFFH	0	0	0	0	0	0	1	1	1	0	0
		⋮												
	0:0E000H	to	0:0E3FFH	0	0	0	1	1	1	0	0	0	0	0
	0:0E400H	to	0:0E7FFH	0	0	0	1	1	1	0	0	1	0	0
	0:0E800H	to	0:0EBFFH	0	0	0	1	1	1	0	1	0	0	0
	0:0EC00H	to	0:0EFFFH	0	0	0	1	1	1	0	1	1	0	0
	0:0F000H	to	0:0F3FFH	0	0	0	1	1	1	1	0	0	0	0
	0:0F400H	to	0:0F7FFH	0	0	0	1	1	1	1	0	1	0	0
	0:0F800H	to	0:0FBFFH	0	0	0	1	1	1	1	1	0	0	0
	0:0FC00H	to	0:0FFFFH	0	0	0	1	1	1	1	1	1	0	0
Segment 7	7:0000H	to	7:03FFH	1	1	1	0	0	0	0	0	0	0	0
	7:0400H	to	7:07FFH	1	1	1	0	0	0	0	0	1	0	0

The unit of sector is 1 KB.
Therefore, the total number of sectors is 66, including 64 sectors in the segment 0 and 2 sectors in the segment 7.

29.2.3 Flash Data Register (FLASHDL, FLASHDH)

Address: 0F0E2H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDL	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDH	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHDL and FLASHDH are special function registers (SFRs) used to set the flash memory rewrite data.

Description of bits

- **FD7-FD0** (bits 7-0)
  The FD7 to FD0 bits are used to set the lower data for 1-word write.

- **FD15 to FD8** (bits 7-0)
  The FD15 to FD8 bits are used to set the upper data for 1-word write.
  Writing to the FD15 to FD8 bits starts the 1-word write.
  The CPU stops instructions during a flash memory write operation. After the completion of writing, the CPU restarts from the next instruction.

[Note]
Clear the contents of the target addresses in advance. The content of an overwritten address is not guaranteed.
Writing to FLASHDH starts the 1-word write. Write data to FLASHDL and FLASHDH in this order.

29.2.4 Flash Control Register (FLASHCON)

Address: 0F0E4H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHCON	—	—	—	—	—	—	FSERA	FERS
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHCON is a write-only special function register (SFR) to control the block erase and sector erase for the flash memory rewrite.

Description of bits

- **FSERS** (bit 1)
  FSERS is a bit to specify the start of the sector erase.
  Setting the FSERS bit to "1" erases the sector specified by the FLASHSEG and FLASHAH registers. This bit is automatically set to "0" after all data has been erased.
  The CPU stops executing instructions during a flash memory erase operation. After the completion of writing, the CPU restarts executing from the next instruction.

FSERS	FERS	Description
0	0	Stop block/sector erase (initial value)
0	1	Start block erase
1	0	Start sector erase
1	1	Start block erase

- **FERS** (bit 0)
  The FERS bit is used to start the block erase.
  Setting the FERS bit to "1" erases the block specified by the FLASHSEG and FLASHAH registers. This bit is automatically set to "0" after all data has been erased.
  The CPU stops executing instructions during a flash memory erase operation. After the completion of writing, the CPU restarts executing from the next instruction.

29.2.5 Flash Acceptor (FLASHACP)

Address: 0F0E6H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHACP	fac7	fac6	fac5	fac4	fac3	fac2	fac1	fac0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHACP is a write-only special function register (SFR) to control the block erase for the flash memory rewrite or enable/disable the 1-word write operation.

Description of bits

- **fac7-fac0** (bit 7-0)
  The fac7 to fac0 registers are used to restrict the block erase or 1-word write operation in order to prevent an unintended operation.
  Writing "0FAH" and "0F5H" to FLASHACP in this order enables a one-time block erase or 1-word write. For subsequent block erases or 1-word writes, "0FAH" and "0F5H" must be written to FLASHACP each time.
  Even if another instruction is inserted between "0FAH" and "0F5H" written to FLASHACP, the block erase or 1-word write is enabled. Note that, if data other than "0F5H" is written to FLASHACP after "0FAH" is written, the "0FAH" write processing becomes invalid. So, it must be rewritten "0FAH" at first.

29.2.6 Flash Segment Register (FLASHSEG)

Address: 0F0E8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSEG	—	—	—	—	—	FSEG2	FSEG1	FSEG0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSEG is a special function register (SFR) used to set the flash memory rewrite segment address.

Description of bits

- **FSEG2-0** (bits 2-0)
  The FSEG2 to FSEG0 bits are used to specify the flash memory segment address.
  For details, see the description of the flash address registers (FLASHAL, FLASHAH).

29.2.7 Flash Self Register (FLASHSLF)

Address: 0F0EAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSLF	—	—	—	—	—	—	—	FSELF
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSLF is a special function register (SFR) used to control the flash memory self-rewrite function.

Description of bits

- **FSELF** (bit 0)
  To use the flash memory self-rewrite function, the FSELF bit needs to be set to “1”.

FSELF	Description
0	Flash memory rewrite disabled (initial value)
1	Flash memory rewrite enabled

29.2.8 Flash Remap Register (REMAPADD)

Address: 0F0ECH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
REMAPADD	RBTA	RES2	RES1	RES0	REA15	REA14	REA13	REA12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

REMAPADD is a special function register (SFR) used to specify the remap area.
In REMAPADD, the following two types of remapping can be specified.

1. Remap the addresses from 0000H to 0FFFH (4 KB) to an area of the same size (4 KB or less) starting from the address specified by the RES2 to RES0 bits and REA15 to REA12 bits.

2.
ML620Q151A/ML620Q154A/ML620Q157A :
Remap the addresses from 0000H to 02FFH (512 B) to the ISP boot area (addresses from 7C00H to 7DFFH) by setting the RBTA bit.
ML620Q152A/ML620Q155A/ML620Q158A :
Remap the addresses from 0000H to 02FFH (512 B) to the ISP boot area (addresses from 0BC00H to 0BDFFH) by setting the RBTA bit.
ML620Q153A/ML620Q156A/ML620Q159A :
Remap the addresses from 0000H to 02FFH (512 B) to the ISP boot area (addresses from 0FC00H to 0FDFFH) by setting the RBTA bit.

When the software reset is executed by the BRK instruction (* only the CPU is reset), the CPU executes instructions from the beginning address of the remap area specified in REMAPADD. Note that the remap function remaps all of the vector table areas (reset vector area, hardware interrupt vector area, and software interrupt vector area). * For the BRK instruction, refer to “nX-U16/100 Core Instruction Manual”.

Description of bits

- **RBTA** (bit 7)
  By setting RBTA to "1", the boot area can be remapped to the ISP boot area (addresses from xC00H to xDFFH). As REA15 to REA12 can specify only "x", the higher 4 bits of the address (xC00H), use this bit to remap the boot area to the ISP boot area.

- **RES2-RES0** (bits 6-4)
  The RES2 to RES0 bits are used to set the segment of the area to remap.
  Since only the segment 0 is used in this LSI, set these bits to 0.

- **REA15-REA12** (bits 3-0)
  The REA15 to REA12 bits are used to set the higher 4 bits (bits 15 to 12) of the beginning address of the area to remap.
  Example) When “0BH” is set in REA15 to 12 and the BRK instruction is executed, the area from 0F000H to 0FFFFH is mapped to 0000H to 0FFFH.

29.3 Description of Operation

When using the self-rewrite function, prepare the program for self-rewrite in advance on a program code area with addresses that are not used for block/sector erase or 1-word write.
The self-rewrite function includes the block erase function that erases by 8 K words (16 Kbytes), the sector erase function that erases by 512 words (1 Kbyte), and the 1-word write function that writes by 1 word (2 bytes).

The rewrite count of the flash memory depends on the address as shown in the table below.

For ML620Q151A/ML620Q154A/ML620Q157A

Rewrite address	Rewrite count
Area from 0:0000H to 0:07FFFH	100
7:0000H to 7:07FFH	10000

For ML620Q152A/ML620Q155A/ML620Q158A

Rewrite address	Rewrite count
Area from 0:0000H to 0:0BFFFH	100
7:0000H to 7:07FFH	10000

For ML620Q153A/ML620Q156A/ML620Q159A

Rewrite address	Rewrite count
Area from 0:0000H to 0:0FFFFH	100
7:0000H to 7:07FFH	10000

It also includes the flash self register and flash rewrite acceptor function that restrict the self-rewrite operation, to prevent an improper rewriting of the flash memory. When "0FAH" is written to the flash acceptor (FLASHACP) after the self-rewrite function is enabled in the flash self register, the block/sector erase or 1-word write is enabled only once.

The flash memory self-write operation is not supported when the system clock (CPU operation clock) speed is low. Notes on each clock mode are described below.

Table 29-7 System Clock and Cautions When Performing Flash Memory Self-Rewrite

Clock mode and register setting		Cautions
Low-speed crystal oscillation mode Internal low-speed RC oscillation mode	When the SYSCLK bit of FCON1 register is set to "0" (initial value).	The flash memory self-write operation is not guaranteed.
Internal high-speed RC oscillation clock mode	When the OSCM1 and OSCM0 bits of FCON0 register are set to "0" and "0" (initial value) respectively, and the SYSCLK bit of FCON1 register is set to "1". The dividing ratio of the clock can be set by the SYSC1-0 bits of the FCON0 register. (One of 2.097 MHz, 1.048 MHz, 524 KHz and 262 KHz is used as the system clock.)	The operating frequency is not restricted.
Internal PLL oscillation clock mode	When the OSCM1 and OSCM0 bits of FCON0 register are set to "1" and "0" (initial value) respectively, and the SYSCLK bit of FCON1 register is set to "1". The dividing ratio of the clock can be set by the SYSC1-0 bits of the FCON0 register. (One of	The operating frequency is not restricted.

	8.192 MHz, 4.096 MHz, 2.048 MHz, and 1.024 MHz is used as the system clock.)	

For details of clock modes and settings, see Chapter 6, "Clock Generation Circuit".

Note on debugging flash self-write code using the U16 development environment are described below.

Table 29-8 Cautions When Debugging Flash Self-Write Code

State of use	Cautions
When debugging flash self-write code using the DTU8 debugger	• Do not perform real time execution (GO execution) while break points are set in the flash self-write sequence (from writing to the flash acceptor to writing to the flash data register). If real time execution is performed with break points set in the sequence, flash self-write may not be executed. • Do not perform STEP execution in the flash self-write sequence (from writing to the flash acceptor to writing to the flash data register). If STEP execution is performed in the sequence, flash self-write may not be executed. • The data flash area (07:00000H-07:007FFH) can be referred through the "Memory of One Physical Segment or more" window on the DTU8 debugger. However, the data cannot be changed directly in this window (the change will not be accepted by the DTU8 debugger).
DTU8, FWμEASE, When writing to the flash memory with MWμEASE	Erase/write to the data flash area using the on-chip debug emulator (μEASE) is not supported.

29.3.1 Block Erase Function

This function erases the flash memory data by block (8 Kbytes).
Writing "01H" to the flash self register starts voltage multiplying in the LSI, and rewrite operation becomes enabled.
Write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the block address in the flash address register H (FLASHAH). Then, write "1" to the FERS bit of the flash control register (FLASHCON) to erase the data in the block (8 Kbytes) specified by FLASHAH.
During the block erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that sets the FERS bit of FLASHCON to "1".
Figure 29-1 shows a sample program of block erase.

```
        LEA     offset FLASHAH              ; EA ← FLASHAH address
        MOV     R0,     #0FAH               ; Flash acceptor enable data
        MOV     R1,     #0F5H               ; Flash acceptor enable data
        MOV     R2,     #01H                ; Block erase setting data
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8   ; ER4 ← FLASHACP address
        MOV     R6,     #(offset FLASHCON)&0FFH
        MOV     R7,     #(offset FLASHCON)>>8   ; ER6 ← FLASHCON address
        :
        (Set the erase start block address to R9)
MARK:
        SB      FSELF               ; Enable flash self-write
                                    (Start voltage multiplying in the LSI)

        ST      R0,     [ER4]               ; Enable flash acceptor
        ST      R1,     [ER4]               ; Enable flash acceptor
        ST      R9,     [EA]                ; Set block address
        ST      R2,     [ER6]               ; Start block erase
        NOP                                 ; ※ Always set
        NOP                                 ; ※ Always set

        RB      FSELF               ; Disable flash self-write
                                    (The voltage returns to the normal operation level)
```

Figure 29-1 Sample Program of Block Erase

[Note]

- Be sure to set the NOP instruction twice or more, following the block erase start instruction.
- Do not erase the running program itself.

29.3.2 Sector Erase Function

This function erases the flash memory data by sector (1 Kbytes).
Writing "01H" to the flash self register starts voltage multiplying in the LSI, and rewrite operation becomes enabled. After checking the completion of voltage multiplying with the flash status register, write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the sector address in the flash address register H (FLASHAH). Then, write "1" to the FSERS bit of the flash control register (FLASHCON) to erase the data in the sector (1 Kbyte) specified by FLASHAH.
During the sector erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that sets the FSERS bit of FLASHCON to "1".
Figure 29-2 shows a sample program of sector erase.

```
        LEA     offset FLASHAH                  ; EA ← FLASHAH address
        MOV     R0,     #0FAH                   ; Flash acceptor enable data
        MOV     R1,     #0F5H                   ; Flash acceptor enable data
        MOV     R2,     #02H                    ; Sector erase setting data
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8   ; ER4 ← FLASHACP address
        MOV     R6,     #(offset FLASHCON)&0FFH
        MOV     R7,     #(offset FLASHCON)>>8   ; ER6 ← FLASHCON address
        :
        (Set the erase start block address to R9)
MARK:
        SB      FSELF               ; Enable flash self-write
                                    (Start voltage multiplying in the LSI)

        ST      R0,     [ER4]               ; Enable flash acceptor
        ST      R1,     [ER4]               ; Enable flash acceptor
        ST      R9,     [EA]                ; Set sector address
        ST      R2,     [ER6]               ; Start sector erase
        NOP                                 ; ※ Always set
        NOP                                 ; ※ Always set

        RB      FSELF               ; Disable flash self-write
                                    (The voltage returns to the normal operation level)
```

Figure 29-2 Sample Program of Sector Erase

[Note]

- Be sure to set the NOP instruction twice or more, following the sector erase start instruction.
- Do not erase the running program itself.

29.3.3 1-word Write Function

This function writes data to the flash memory by 1 word (2 bytes).
Writing "01H" to the flash self register starts voltage multiplying in the LSI, and rewrite operation becomes enabled. After checking the completion of voltage multiplication with the flash status register, write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the address in the flash address register L, H (FLASHAL,H). Then, write data to the flash data register L, H (FLASHDL,H) to write the data in the address specified by FLASHAL, H.
During the 1-word write, the CPU is stopped. When the write is completed, the program is restarted from the instruction following the write to FLASHDH instruction.
Figure 29-3 shows a sample program of 1-word write (assuming that the flash segment register is already set).

```
        LEA     offset FLASHAH                  ; EA ← FLASHAH address
        MOV     R0,     #0FAH                   ; Flash acceptor enable data
        MOV     R1,     #0F5H                   ; Flash acceptor enable data
        MOV     R2,     #02H                    ; Address increment data
        MOV     R3,     #00H
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8   ; ER4 ← FLASHACP address
        :
        (Set the write start address in ER8)
        (Set the write end address in ER12)
MARK:
        SB      FSELF                   ; Enable flash self-write
                                        (Start voltage multiplying in the LSI)

        ST      R0,     [ER4]           ; Enable flash acceptor
        ST      R1,     [ER4]           ; Enable flash acceptor
        ST      XR8,    [EA]            ; Set address and data, start 1-word write
        NOP                             ; ※ Always set
        NOP                             ; ※ Always set

    L       ER14,   [ER8]               ; Load data
    CMP     ER14,   ER10                ; Check data
    BNE     ERROR                       ; Go to error routine on error

    ADD     ER8,    ER2                 ; Address increment
    CMP     ER8,    ER12
    BLE     MARK                        ; Compare addresses

        RB      FSELF                   ; Disable flash self-write
                                        (The voltage returns to the normal operation level)
```

Figure 29-3 Sample Program of 1-word Write

[Note]

- Be sure to set the NOP instruction twice or more, following the write to FLASHDH instruction.
- Do not erase the running program itself.

29.3.4 Boot Area Remap Function by Software

This function can remap the area from 0000H to 0FFFH (4 KB) to the area of the same size (4 KB or less) starting from the address set in the REMAPADD register.
The program can start from the remapped area by setting the beginning address of the area to remap in the REMAPADD register and performing the software reset (* only CPU is reset) by execution of the BRK instruction. For the BRK instruction, refer to “nX-U16/100 Core Instruction Manual”.
The remap function also remaps the vector table areas (reset vector area, hardware interrupt vector area, and software interrupt vector area). This allows for the managing of interrupts independently by the program in the remap area. If the program size is 4 KB or less, the program can be developed independently of the main program. This is useful when controlling some interrupts generated by the self-rewrite program, etc. separately from normal interrupts.
Figure 29-4 shows a sample program for remap (when the beginning address of the remap area is 0F000H). Figure 29-5 shows the memory map before and after remapping.

```
MOV     R0,    #00FH      ;
ST      R0,    0F0ECH     ; Set the higher 4 bits of the beginning address of the area
                          ; to remap to the REMAPADD register (0F0ECH).
MOV     PSW, #02H         ; Set the interrupt level (ELEVEL) to 2.
BRK                       ; Execute the BRK instruction.
                          ; Execution starts with the code at the remapped 0F000H.
```

Figure 29-4 Sample Program for Remap

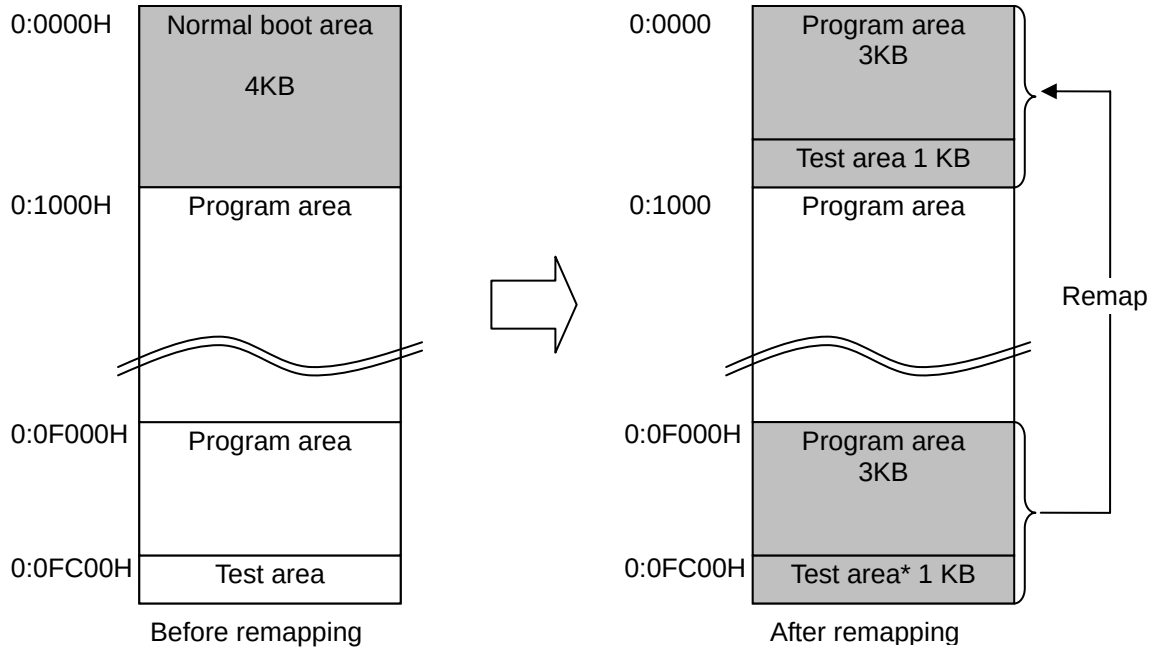


Figure 29-5 Memory Map before/after Remapping (ML620Q153A/ML620Q156A/ML620Q159A)

[Note]
To read the previous (before remapping) area 0:0000H to 0:0FFFH (4 KB) after remapping is completed, read from the segment 8. To write the previous area 0:0000H to 0:0FFFH (4 KB) before remapping, set the flash address register (FLASHAL,H) with the previous(before remapping) address (0:0000H to 0:1000H). For FLASHAL,H, see Section 29.2.2, "Flash Address Register (FLASHAL, H)".

29.3.5 Notes in Use

When the power is down or the operation is terminated forcibly during block/sector erase or 1-word write, retry the block erase and rewrite the block area of 8K words.
If the self-rewrite program does not work, write the program by using the on-chip debug emulator (µEASE).

Chapter 30 Code-Option

30 Code-Option

3.1 General Description

This LSI has the code-option function.
The code-option function can select the low-speed oscillation clock (External crystal oscillation or Internal RC oscillation), LLD circuit operation (Interrupt of Reset) and the LLD threshold voltage level.

3.1.1 Features

- External low-speed crystal oscillation or internal low—speed RC oscillation is selectable for the low-speed clock.
- Interrupt or Reset is selectable for LLD circuit operation.
- The LLD threshold voltage level is selectable.

30.2 Description of Registers

30.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F3D8H	Code option register 0	CODEOP0	—	R	8	—*

*: Initial value of CODEOP0 depends on the code-option data programmed in test data area.

30.2.2 Code-Option Register 0 (CODEOP0)

Address: 0F3D8H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CODEOP0	COLOSC	—*	—*	—*	—*	LLDSEL	LLD1	LLD0
R/W	R	R	R	R	R	R	R	R
Initial value	x	x	x	x	x	x	x	x

CODEOP0 is a special function register (SFR) that can read Code-Option data.
CODEOP0 is read only register and is not waritable by the software.
For the setting method of the code-option data, refer to 30.3 “The Setting Method of the Code-Option Data”.

[Description of Bits]

- **COLOSC** (bit 7)
  The COLOSC bit is used to select the type of low-speed oscillation clock.

COLOSC	Description
0	Internal low-speed RC oscillation
1	External low-speed crystal oscillation(32.768kHz)

- **LLDSEL** (bit 2)
  LLDSEL bit is used to select a behavoir of LLD circuit when VDD lowers a threshold voltage.

LLDSEL	Description
0	Interrupt output
1	Reset

- **LLD0,1** (bit 1,0)
  LLD1,0 are used to select the threshold voltage in LLD circuit.

LLD1	**LLD0**	Threshold Voltage V_{CMP}	Hysteresis Ta=25 ° C
0	0	1.90V	80mV(Typ.)
0	1	2.55V	
1	0	3.70V	
1	1	4.20V	

30.3 The Setting Method of the Code-Option Data

30.3.1 Code-Option Data Format

ML620Q151A/ML620Q154A/ML620Q157A :
The code-option data is set on address 0:7DE0H which is in writable test data area of program memory.

ML620Q152A/ML620Q155A/ML620Q158A :
The code-option data is set on address 0:BDE0H which is in writable test data area of program memory.

ML620Q153A/ML620Q156A/ML620Q159A :
The code-option data is set on address 0:FDE0H which is in writable test data area of program memory.

Address	7	6	5	4	3	2	1	0
0:xxE0H	COLOSC	—*	—*	—*	—*	LLDSEL	LLD1	LLD0

Address	15	14	13	12	11	10	9	8
0:xxE1H	—*	—*	—*	—*	—*	—*	—*	—*

30.3.2 Code-Option Programming Method

Figure 30-1 shows examples on how to specify the code-option data for ML620Q153A/ML620Q156A/ML620Q159A. The specified program code is to be programmed by Flash programming tools.

・ When using the external 32.768kHz crystal oscillation for the low-speed clock

```
; ------------------------------------------------------
;       Setting the code-option data
; ------------------------------------------------------
        cseg at 0:0fde0h                ; change the address for other devices
        dw      0080h
```

・ When using the external 32.768kHz crystal oscillation for the low-speed clock

```
; ------------------------------------------------------
;       Setting the code-option data
; ------------------------------------------------------
        cseg at 0:0fde0h                ; change the address for other devices
        dw      0000h
```

Figure 30-1 Examples on how to specify the code-option data

[Note]
・Specify the code-option data in the test data area of program memory.
・Fill the test data area with "0FFH" except the address for code-option.

Appendix A

Contents of Registers

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H
0F001H	Reserve	—	—	—	—	—
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	03H
0F005H	Frequency control register 3	FCON3		R/W	8	00H
0F008H	Stop code acceptor	STPACP	—	W	8	Undefined
0F009H	Standby control register	SBYCON	—	W	8	00H
0F00AH	Frequency status register	FSTAT	—	R	8	04H
0F00BH	Reserve	—	—	—	—	—
0F00CH	Reset Status register	RSTAT	—	R/W	8	Undefined
0F00DH	Reserve	—	—	—	—	—
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H
0F020H	Interrupt level control enable register	ILENL	ILEN	R/W	8/16	00H
0F021H	Reserve	—		R/W	8	00H
0F022H	Interrupt Current requeset level register	CILL	CIL	R/W	8/16	00H
0F023H	Reserve	—		R/W	8	00H
0F024H	Reserve	—	—	—	—	—
0F025H	Interrupt level control register 01	ILC01	—	R/W	8	00H
0F026H	Interrupt level control register 10	ILC10	ILC1W	R/W	8/16	00H
0F027H	Interrupt level control register 11	ILC11		R/W	8	00H
0F028H	Interrupt level control register 20	ILC20	ILC2W	R/W	8/16	00H
0F029H	Interrupt level control register 21	ILC21		R/W	8	00H
0F02AH	Interrupt level control register 30	ILC30	ILC3W	R/W	8/16	00H
0F02BH	Interrupt level control register 31	ILC31		R/W	8	00H
0F02CH	Interrupt level control register 40	ILC40	ILC4W	R/W	8/16	00H
0F02DH	Interrupt level control register 41	ILC41		R/W	8	00H

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F02EH	Interrupt level control register 50	ILC50	ILC5W	R/W	8/16	00H
0F02FH	Interrupt level control register 51	ILC51		R/W	8	00H
0F030H	Interrupt level control register 60	ILC60	ILC6W	R/W	8/16	00H
0F031H	Interrupt level control register 61	ILC61		R/W	8	00H
0F032H	Interrupt level control register 70	ILC70	ILC7W	R/W	8/16	00H
0F033H	Interrupt level control register 71	ILC71		R/W	8	00H
0F038H	External interrupt control register 0	EXICON0	–	R/W	8	00H
0F039H	External interrupt control register 1	EXICON1	–	R/W	8	00H
0F03AH	External interrupt control register 2	EXICON2	–	R/W	8	00H
0F060H	Low-speed time base counter register	LTBR	–	R/W	8	00H
0F061H	Reserve	–	–	–	–	–
0F062H	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F063H	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H
0F064H	Low-speed time base counter interrupt register L	LTBINTL	LTBINT	R/W	8/16	30H
0F065H	Low-speed time base counter interrupt register H	LTBINTH		R/W	8	06H
0F068H	Block control register 0	BLKCON0	–	R/W	8	00H
0F069H	Reserve	–	–	–	–	–
0F06AH	Block control register 2	BLKCON2	–	R/W	8	00H
0F06BH	Block control register 3	BLKCON3	–	R/W	8	00H
0F06CH	Block control register 4	BLKCON4	–	R/W	8	00H
0F06DH	Block control register 5	BLKCON5	–	R/W	8	00H
0F06EH	Block control register 6	BLKCON6	–	R/W	8	00H
0F06FH	Block control register 7	BLKCON7	–	R/W	8	00H
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	–	R/W	8	00H
0F0E5H	Reserve	–	–	–	–	–
0F0E6H	Flash acceptor	FLASHACP	–	R/W	8	00H
0F0E7H	Reserve	–	–	–	–	–
0F0E8H	Flash segment register	FLASHSEG	–	R/W	8	00H
0F0E9H	Reserve	–	–	–	–	–
0F0EAH	Flash self register	FLASHSLF	–	R/W	8	00H
0F0EBH	Reserve	–	–	–	–	–
0F0ECH	Flash remap register	REMAPADD	–	R/W	8	00H
0F0EDH	Reserve	–	–	–	–	–
0F0EEH	Flash status register	FLASHSTA	–	R/W	8	00H
0F0EFH	Reserve	–	–	–	–	–
0F20CH	Port 0 data register	P0D	–	R	8	Undefined
0F20DH	Reserve	–	–	–	–	–
0F20EH	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	10H
0F20FH	Port 0 control register 1	P0CON1		R/W	8	00H
0F21AH	Port 1 data register	P1D	–	R/W	8	Undefined

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F21BH	Port 1 direction register	P1DIR	—	R/W	8	18H
0F21CH	Port 1 control register 0	P1CON0	P1CON	R/W	8/16	00H
0F21DH	Port1 control register 1	P1CON1		R/W	8	00H
0F228H	Port 2 data register	P2D	—	R/W	8	00H
0F229H	Reserve	—	—	—	—	—
0F22AH	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F22BH	Port 2 control register 1	P2CON1		R/W	8	00H
0F22CH	Port 2 mode register 0	P2MOD0	P2MOD	R/W	8/16	00H
0F22DH	Port 2 mode register 1	P2MOD1		R/W	8	00H
0F236H	Port 3 data register	P3D	—	R/W	8	00H
0F237H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F238H	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F239H	Port 3 control register 1	P3CON1		R/W	8	00H
0F23AH	Port 3 mode register 0	P3MOD0	P3MOD	R/W	8/16	00H
0F23BH	Port 3 mode register 1	P3MOD1		R/W	8	00H
0F244H	Port 4 data register	P4D	—	R/W	8	00H
0F245H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F246H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F247H	Port 4 control register 1	P4CON1		R/W	8	00H
0F248H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F249H	Port 4 mode register 1	P4MOD1		R/W	8	00H
0F252H	Port 5 data register	P5D	—	R/W	8	00H
0F253H	Port 5 direction register	P5DIR	—	R/W	8	00H
0F254H	Port 5 control register 0	P5CON0	P5CON	R/W	8/16	00H
0F255H	Port 5 control register 1	P5CON1		R/W	8	00H
0F256H	Port 5 mode register 0	P5MOD0	P5MOD	R/W	8/16	00H
0F257H	Port 5 mode register 1	P5MOD1		R/W	8	00H
0F260H	Port 6 data register	P6D	—	R/W	8	00H
0F261H	Port 6 direction register	P6DIR	—	R/W	8	00H
0F262H	Port 6 control register 0	P6CON0	P6CON	R/W	8/16	00H
0F263H	Port 6 control register 1	P6CON1		R/W	8	00H
0F264H	Port 6 mode register 0	P6MOD0	P6MOD	R/W	8/16	00H
0F265H	Reserve	—		—	—	—
0F26EH	Port 7 data register	P7D	—	R/W	8	00H
0F26FH	Port 7 direction register	P7DIR	—	R/W	8	00H
0F270H	Port 7 control register 0	P7CON0	P7CON	R/W	8/16	00H
0F271H	Port 7 control register 1	P7CON1		R/W	8	00H
0F272H	Port 7 mode register 0	P7MOD0	P7CON	R/W	8/16	00H
0F273H	Port 7 mode register 1	P7MOD1		R/W	8	00H
0F27CH	Port 8 data register	P8D	—	R/W	8	00H
0F27DH	Port 8 direction register	P8DIR	—	R/W	8	00H
0F27EH	Port 8 control register 0	P8CON0	P8CON	R/W	8/16	00H
0F27FH	Port 8 control register 1	P8CON1		R/W	8	00H
0F280H	Port 8 mode register 0	P8MOD0	P8CON	R/W	8/16	00H
0F281H	Port 8 mode register 1	P8MOD1		R/W	8	00H
0F300H	Timer 0 data register	TM0D	TM01D	R/W	8/16	0FFH
0F301H	Timer 1 data register	TM1D		R/W	8	0FFH

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F310H	Timer 0 counter register	TM0C	TM01C	R/W	8/16	00H
0F311H	Timer 1 counter register	TM1C		R/W	8	00H
0F320H	Timer 0 control register	TM0CON	TM01CON	R/W	8/16	00H
0F321H	Timer 1 control register	TM1CON		R/W	8	00H
0F330H	Timer start register 0	TMSTR0	—	R/W	8	00H
0F331H	Reserve	—		—	—	—
0F332H	Timer stop register 0	TMSTP0	—	R/W	8	00H
0F333H	Reserve	—		—	—	—
0F334H	Timer status register 0	TMSTAT0	—	R/W	8	00H
0F335H	Reserve	—		—	—	—
0F340H	16bit Timer 8 data register L	TMH8DL	TMH8D	R/W	8	0FFH
0F341H	16bit Timer 8 data register H	TMH8DH		R/W	8/16	0FFH
0F342H	16bit Timer 9 data register L	TMH9DL	TMH9D	R/W	8	0FFH
0F343H	16bit Timer 9 data register H	TMH9DH		R/W	8/16	0FFH
0F344H	16bit Timer A data register L	TMHADL	TMHAD	R/W	8	0FFH
0F345H	16bit Timer A data register H	TMHADH		R/W	8/16	0FFH
0F346H	16bit Timer B data register L	TMHBDL	TMHBD	R/W	8	0FFH
0F347H	16bit Timer B data register H	TMHBDH		R/W	8/16	0FFH
0F350H	16bit Timer 8 counter register L	TMH8CL	TMH8C	R/W	8	00H
0F351H	16bit Timer 8 counter register H	TMH8CH		R/W	8/16	00H
0F352H	16bit Timer 9 counter register L	TMH9CL	TMH9C	R/W	8	00H
0F353H	16bit Timer 9 counter register H	TMH9CH		R/W	8/16	00H
0F354H	16bit Timer A counter register L	TMHACL	TMHAC	R/W	8	00H
0F355H	16bit Timer A counter register H	TMHACH		R/W	8/16	00H
0F356H	16bit Timer B counter register L	TMHBCL	TMHBC	R/W	8	00H
0F357H	16bit Timer B counter register H	TMHBCH		R/W	8/16	00H
0F360H	16bit Timer 8 control register	TMH8CON	—	R/W	8	00H
0F361H	Reserve	—	—	—	—	—
0F362H	16bit Timer 9 control register	TMH9CON	—	R/W	8	00H
0F363H	Reserve	—	—	—	—	—
0F364H	16bit Timer A control register	TMHACON	—	R/W	8/	00H
0F365H	Reserve	—	—	—	—	—
0F366H	16bit Timer B control register	TMHBCON	—	R/W	8	00H
0F367H	Reserve	—	—	—	—	—
0F370H	16bit Timer start register 0	TMHSTR0		R/W	8	00H
0F372H	16bit Timer stop register 0	TMHSTP0		R/W	8	00H
0F374H	16bit Timer status register 0	TMHSTAT0		R/W	8	00H
0F3D8H	Code-Option register 0	CODEOP0	—	R	8	XXH
0F4A0H	PWM4 period register L	PW4PL	PW4P	R/W	8/16	0FFH
0F4A1H	PWM4 period register H	PW4PH		R/W	8	0FFH
0F4A2H	PWM4 duty register L	PW4DL	PW4D	R/W	8/16	00H
0F4A3H	PWM4 duty register H	PW4DH		R/W	8	00H
0F4A4H	PWM4 counter register L	PW4CL	PW4C	R/W	8/16	00H
0F4A5H	PWM4 counter register H	PW4CH		R/W	8	00H
0F4A6H	PWM4 control register 0	PW4CON0	PW4CON	R/W	8/16	00H

0F4A7H	PWM4 control register 1	PW4CON1	0W	R/W	8	40H

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F4A8H	PWM4 control register 2	PW4CON2	PW4CON 2W	R/W	8/16	00H
0F4A9H	PWM4 control register 3	PW4CON3		R/W	8	10H
0F4AAH	PWM4 control register 4	PW4CON4	PW4CON 4W	R/W	8/16	00H
0F4ABH	PWM4 control register 5	PW4CON5		R/W	8	00H
0F4ACH	PWM4 control register 6	PW4CON6	—	R/W	8	00H
0F4B0H	PWM5 period register L	PW5PL	PW5P	R/W	8/16	0FFH
0F4B1H	PWM5 period register H	PW5PH		R/W	8	0FFH
0F4B2H	PWM5 duty register L	PW5DL	PW5D	R/W	8/16	00H
0F4B3H	PWM5 duty register H	PW5DH		R/W	8	00H
0F4B4H	PWM5 counter register L	PW5CL	PW5C	R/W	8/16	00H
0F4B5H	PWM5 counter register H	PW5CH		R/W	8	00H
0F4B6H	PWM5 control register 0	PW5CON0	PW5CON 0W	R/W	8/16	00H
0F4B7H	PWM5 control register 1	PW5CON1		R/W	8	40H
0F4B8H	PWM5 control register 2	PW5CON2	—	R/W	8	00H
0F4BAH	PWM5 control register 3	PW5CON4	PW5CON 4W	R/W	8/16	00H
0F4BBH	PWM5 control register 4	PW5CON5		R/W	8	00H
0F4BCH	PWM5 control register 5	PW5CON6	—	R/W	8	00H
0F4C0H	PWM6 period register L	PW6PL	PW6P	R/W	8/16	0FFH
0F4C1H	PWM6 period register H	PW6PH		R/W	8	0FFH
0F4C2H	PWM6 duty register L	PW6DL	PW6D	R/W	8/16	00H
0F4C3H	PWM6 duty register H	PW6DH		R/W	8	00H
0F4C4H	PWM6 counter register L	PW6CL	PW6C	R/W	8/16	00H
0F4C5H	PWM6 counter register H	PW6CH		R/W	8	00H
0F4C6H	PWM6 control register 0	PW6CON0	PW6CON 0W	R/W	8/16	00H
0F4C7H	PWM6 control register 1	PW6CON1		R/W	8	40H
0F4C8H	PWM6 control register 2	PW6CON2	PW6CON 2W	R/W	8/16	00H
0F4C9H	PWM6 control register 3	PW6CON3		R/W	8	10H
0F4CAH	PWM6 control register 4	PW6CON4	PW6CON 4W	R/W	8/16	00H
0F4CBH	PWM6 control register 5	PW6CON5		R/W	8	00H
0F4CCH	PWM6 control register 6	PW6CON6	—	R/W	8	00H
0F4D0H	PWM7 period register L	PW7PL	PW7P	R/W	8/16	0FFH
0F4D1H	PWM7 period register H	PW7PH		R/W	8	0FFH
0F4D2H	PWM7 duty register L	PW7DL	PW7D	R/W	8/16	00H
0F4D3H	PWM7 duty register H	PW7DH		R/W	8	00H
0F4D4H	PWM7 counter register L	PW7CL	PW7C	R/W	8/16	00H
0F4D5H	PWM7 counter register H	PW7CH		R/W	8	00H
0F4D6H	PWM7 control register 0	PW7CON0	PW7CON 0W	R/W	8/16	00H
0F4D7H	PWM7 control register 1	PW7CON1		R/W	8	40H
0F4D8H	PWM7 control register 2	PW7CON2	—	R/W	8	00H
0F4DAH	PWM7 control register 4	PW7CON4	PW7CON 4W	R/W	8/16	00H
0F4DBH	PWM7 control register 5	PW7CON5		R/W	8	00H
0F4DCH	PWM7 control register 6	PW7CON6	—	R/W	8	00H

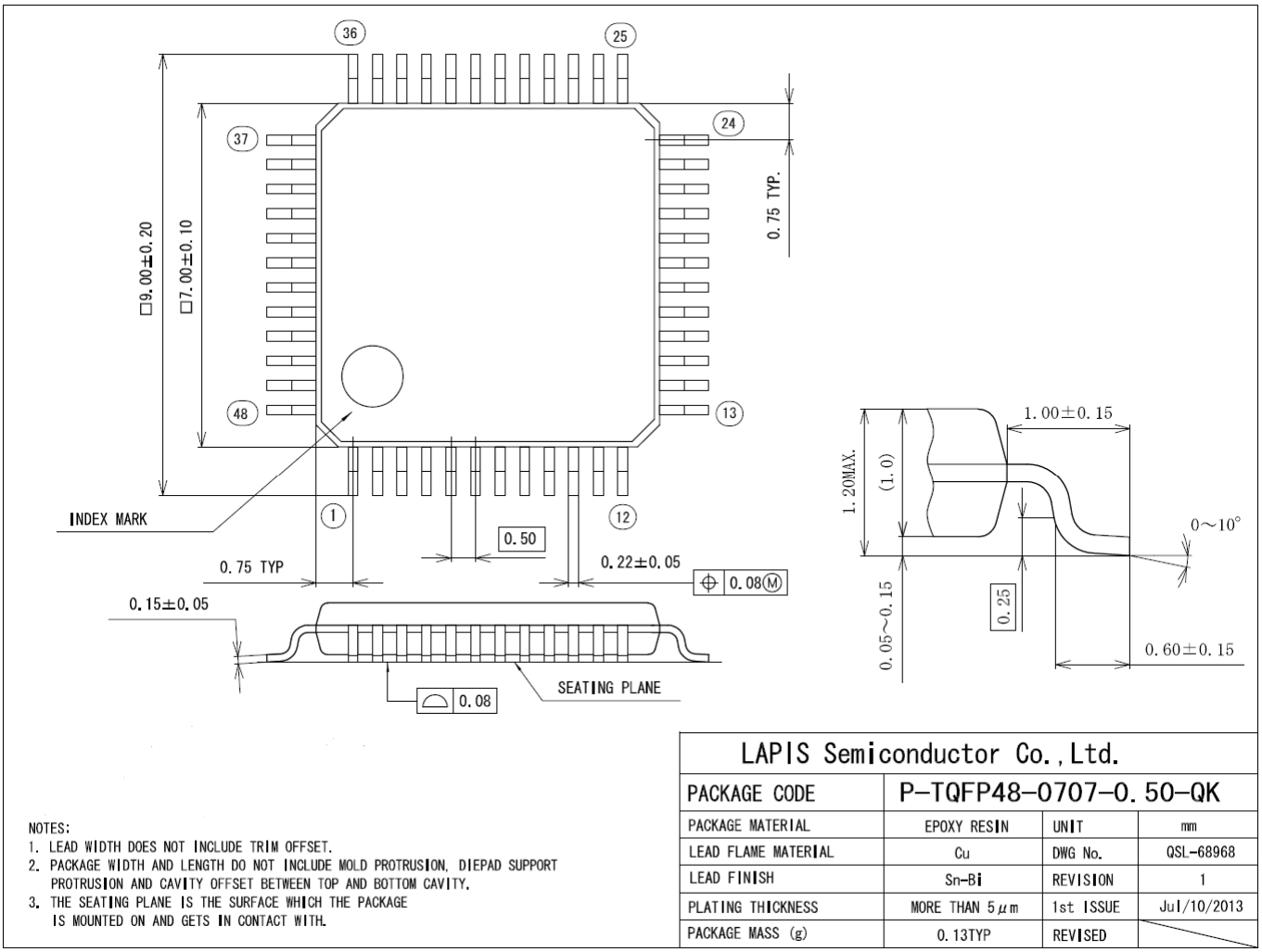
Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F700H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F701H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F702H	Serial port 0 control register	SIO0CON	–	R/W	8	00H
0F704H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F705H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F710H	UART0 transmit/receive buffer	UA0BUF	–	R/W	8	00H
0F711H	UART0 control register	UA0CON	–	R/W	8	00H
0F712H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F713H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F714H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F715H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F716H	UART0 status register	UA0STAT	–	R/W	8	00H
0F717H	Reserve	–	–	–	–	–
0F718H	UART1 transmit/receive buffer	UA1BUF	–	R/W	8	00H
0F719H	UART1 control register	UA1CON	–	R/W	8	00H
0F71AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F71BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F71CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F71DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F71EH	UART1 status register	UA1STAT	–	R/W	8	00H
0F740H	I2C bus 0 reception data register	I2C0RD	–	R	8	00H
0F741H	Reserve	–	–	–	–	–
0F742H	I2C bus 0 slave address regisiter	I2C0SA	–	R/W	8	00H
0F743H	Reserve	–	–	–	–	–
0F744H	I2C bus 0 transmission data register	I2C0TD	–	R/W	8	00H
0F745H	Reserve	–	–	–	–	–
0F746H	I2C bus 0 control register 0	I2C0CON0	I2C0CON	R/W	8/16	00H
0F747H	Reserve	–	–	–	–	–
0F748H	I2C bus 0 mode register L	I2C0MODL	I2C0MOD	R/W	8/16	00H
0F749H	I2C bus 0 mode register H	I2C0MODH	–	R/W	8	02H
0F74AH	I2C bus 0 status register L	I2C0STAL	I2C0STA	R	8/16	00H
0F8C0H	Reserve	–	–	–	–	–
0F8C1H	LLD circuit control register 1	LLDCON1	–	R/W	8	00H
0F8D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F8D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F8D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F8D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F8D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F8D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F8D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F8D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F8D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F8D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F8DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F8DBH	SA-ADC result register 5H	SADR5H		R	8	00H

Address [H]	name	Symbol Byte	Symbol Word	8/16	R/W	Initial value
0F8DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F8DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F8DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F8DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F8E0H	SA-ADC result register 8L	SADR8L	SADR8	R	8/16	00H
0F8E1H	SA-ADC result register 8H	SADR8H		R	8	00H
0F8E2H	SA-ADC result register 9L	SADR9L	SADR9	R	8/16	00H
0F8E3H	SA-ADC result register 9H	SADR9H		R	8	00H
0F8E4H	SA-ADC result register AL	SADRAL	SADRA	R	8/16	00H
0F8E5H	SA-ADC result register AH	SADRAH		R	8	00H
0F8E6H	SA-ADC result register BL	SADRBL	SADRB	R	8/16	00H
0F8E7H	SA-ADC result register BH	SADRBH		R	8	00H
0F8F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F8F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F8F2H	SA-ADC mode register 0	SADMOD0	SADMOD	R/W	8/16	00H
0F8F3H	SA-ADC mode register 1	SADMOD1		R/W	8	00H
0F950H	Comparator 0 control register 0	CMP0CON0	CMP0CON	R/W	8/16	00H
0F951H	Comparator 0 control register 1	CMP0CON1		R/W	8	00H

Appendix B

Appendix B Package Dimensions

- ML620Q151A/ML620Q152A/ML620Q153A Package Dimension (48pin TQFP)



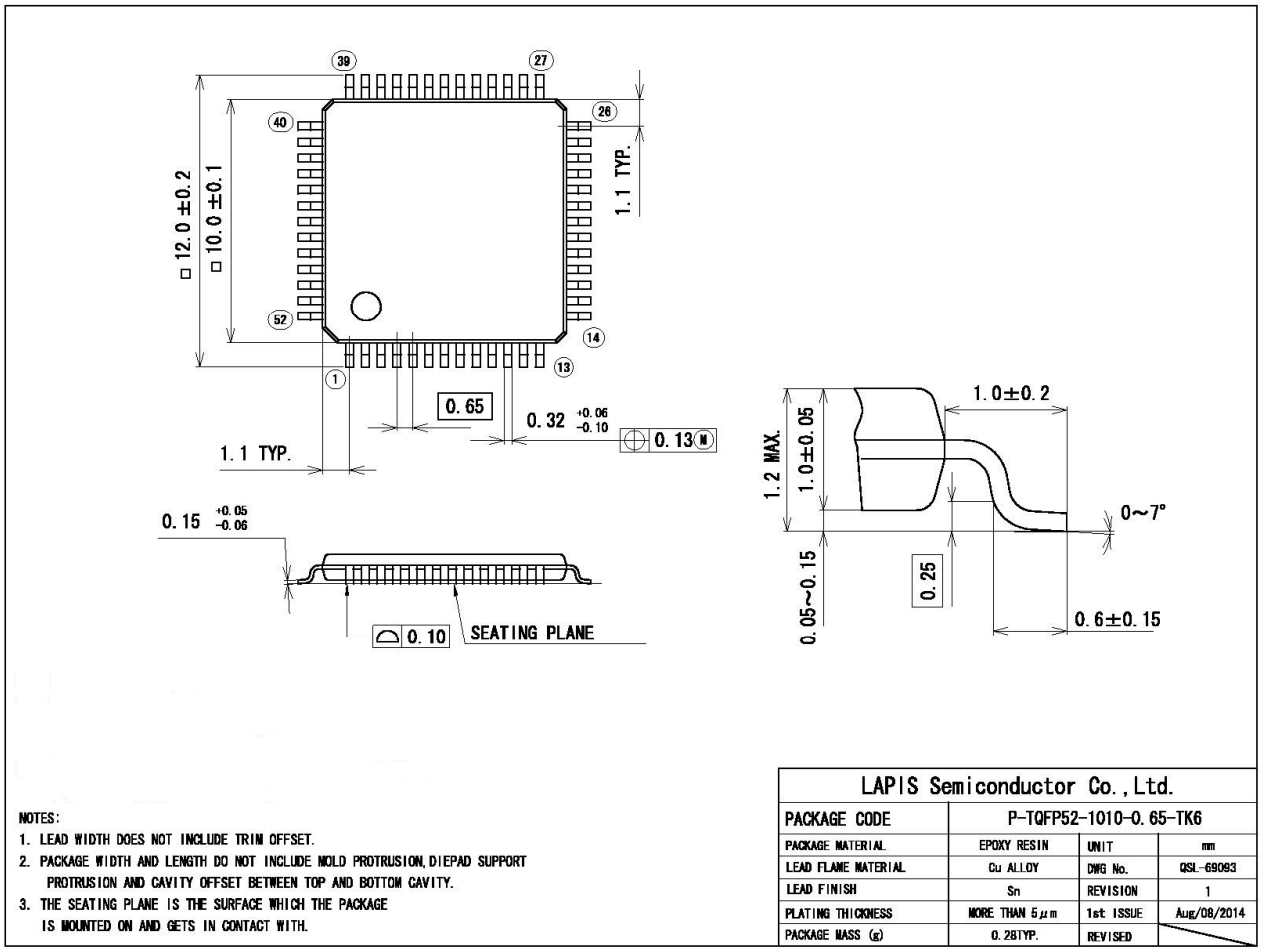
(Unit: mm)

Figure B-1. ML620Q151A/ML620Q152A/ML620Q153A Package Dimension (48pin TQFP)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

- ML620Q154A/ML620Q155A/ML620Q156A Package Dimension (52pin TQFP)



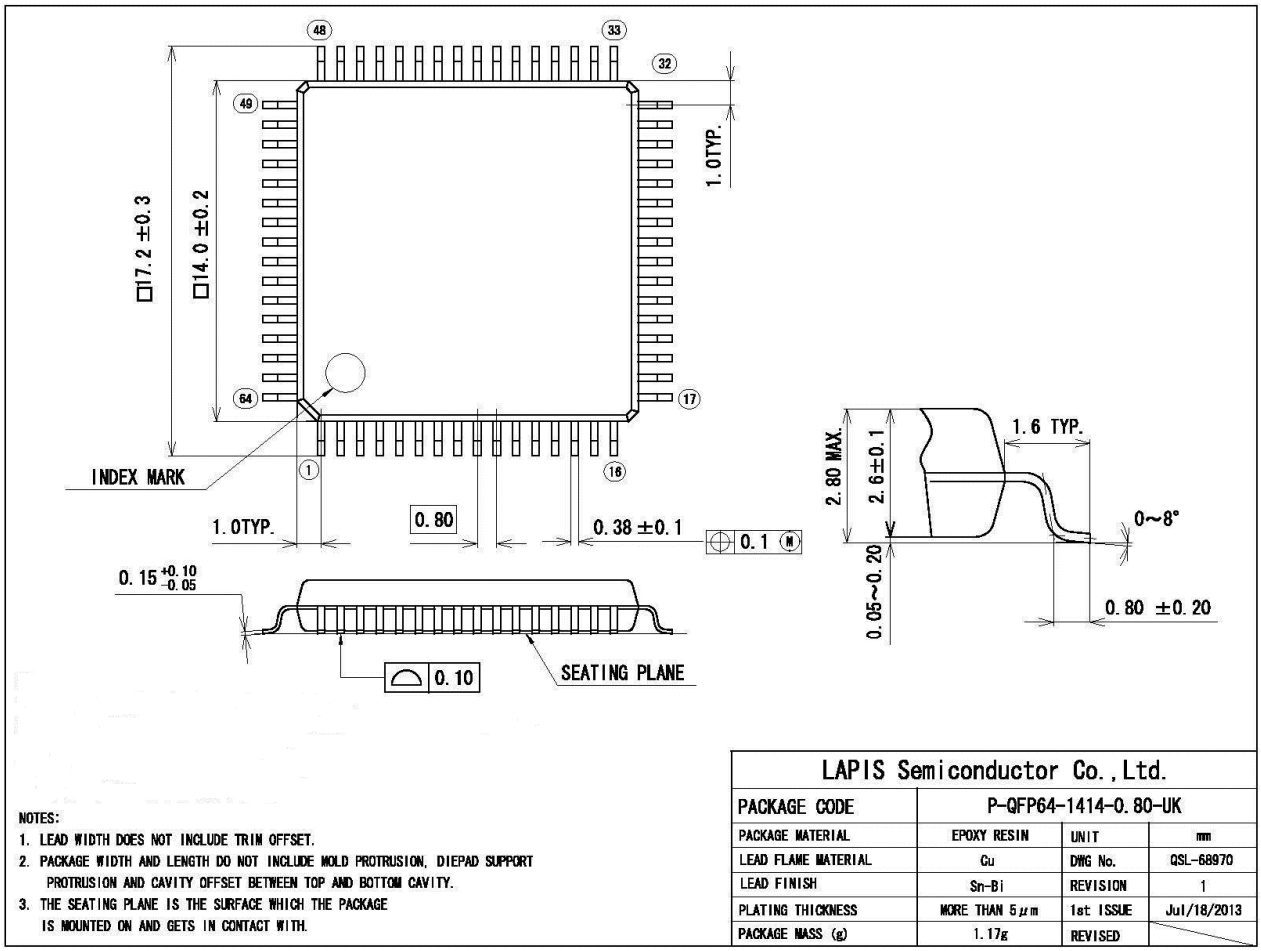
(Unit: mm)

Figure B-2. ML620Q154A/ML620Q155A/ML620Q156A Package Dimension (52pin TQFP)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

- ML620Q157A/ML620Q158A/ML620Q159A Package Dimension (64pin TQFP)



(Unit: mm)

Figure B-3. ML620Q157A/ML620Q158A/ML620Q159A Package Dimension (64pin TQFP)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C

Appendix C Electrical Characteristics

• Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	–0.3 to +2.0	V
Reference voltage	V_{REF}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3,4,5,6,7,8 Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2 Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T_{STG}	—	–55 to +150	°C

• Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +105	°C
Operating voltage	V_{DD}	—	1.8 to 5.5	V
Reference voltage	V_{REF}	—	1.8 to V_{DD}	V
Analog input voltage	V_{AI}	—	V_{SS} to V_{REF}	V
Operating frequency (CPU)	f_{OP}	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C_{DL}	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C_{GL}		12 to 25	
Capacitor externally connected to V_{DDL} pin	C_L	—	2.2±30%	μF

• Flash Memory Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +105	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		1.8 to 5.5	V
Maximum rewrite count	C_{EPD}	Data Flash		10,000	times
	C_{EPP}	Program Flash		100	
Erase unit	—	Chip erase		All area	—
	—	Block erase	Program Flash	8	KB
			Data Flash	2	KB
	—	Sector erase (Data Flash only)		1	KB
Erase time	—	Chip erase, Block erase, Sector erase		100	ms
Write unit	—	—		1 word (2 Bytes)	—
Write time (Max.)	—	1 word (2 Bytes)		40	μs
Data retention period	Y_{DR}	—		15	years

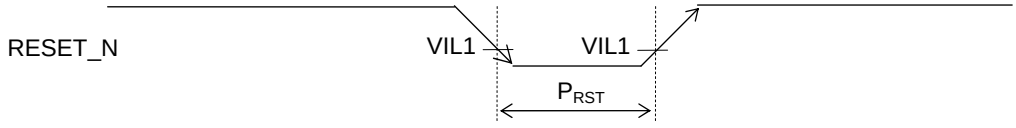
• DC Characteristics (Oscillation, Reset)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

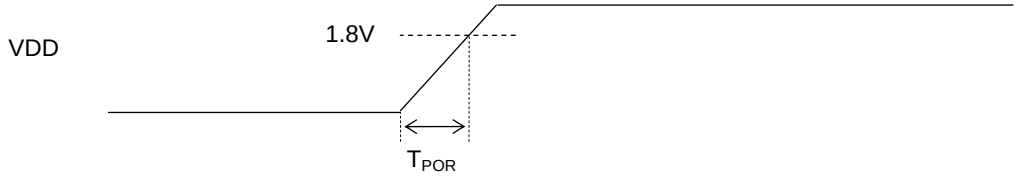
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed crystal oscillation start time*1	T_{XTL}	—	—	0.6	2	s	1
Low-speed RC oscillator frequency	f_{LCR}	Ta= +25°C	Typ -1%	32.768k	Typ +1%	Hz	
		Ta= -40 to 85°C	Typ -2.5%	32.768k	Typ +2.5%	Hz	
		Ta= -40 to 105°C	Typ -3%	32.768k	Typ +3%	Hz	
High-speed RC oscillator ferequency	f_{HCR}	Ta= +25°C	Typ -5%	2.097	Typ +5%	MHz	
		Ta= -40°C to +105°C	Typ -15%	2.097	Typ +15%	MHz	
PLL oscillation frequency	f_{PLL}	LSCLK=32.768kHz 2,048 clock average	Typ -1%	8.192	Typ +1%	MHz	
Reset pulse width	P_{RST}	—	100	—	—	μs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		
Power On Reset rising time	T_{POR}	—	—	—	10	ms	

*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance C_{GL}/C_{DL}=12pF.

Reset



Reset pulse width (P_{RST})



Power On Reset VDD Rising Time (T_{POR})

• DC Characteristics (LLD)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
LLD threshold voltage	V_{D-}	When power falling	LD1 to 0 = 0H	1.8	1.9	2	V	1
			LD1 to 0 = 1H	2.45	2.55	2.65		
			LD1 to 0 = 2H	3.6	3.7	3.8		
			LD1 to 0 = 3H	4.1	4.2	4.3		
	V_{D+}	When power rising	LD1 to 0 = 0H	1.85	1.98	2.1		
			LD1 to 0 = 1H	2.5	2.63	2.75		
			LD1 to 0 = 2H	3.65	3.78	3.9		
			LD1 to 0 = 3H	4.15	4.28	4.4		
Hysterisis	V_{hys}	—	—	—	80	—	mV	mA

• DC Characteristics (Analog Comparator)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Common mode Input voltage	CMPnM V_{IN}	—	0	—	V_{DD} -1.4	V	1
	CMPnP V_{IN}	—	0	—	V_{DD}		
Input offset voltage	V_{CMPOF}	—	—	5	100	mV	
Response time	T_{CMP}	CMPnP = CMPnM ± 100mV	—	—	1	μS	

• DC Characteristics (IDD)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU is in STOP state. Low-speed/high-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	1.0	6	μA	1
			-40 to +105℃	—	1.0	22		
Supply current 2	IDD2	Crystal Oscillating. CPU is in HALT state (LTBC,WBC: Operating*2). High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	2.5	7		
			-40 to +105℃	—	2.5	24		
		Internal RC Oscillating. CPU is in HALT state (LTBC,WBC: Operating*2). High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	3.5	9		
			-40 to +105℃	—	3.5	26		
Supply current 3	IDD3	CPU: Running at 32kHz*1 High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	13	20		
			-40 to +105℃	—	13	42		
Supply current 4	IDD4	CPU: Running at 2MHz RC oscillating mode*2 V_{DD}=5.0V		—	0.64	2.0	mA	
Supply current 5	IDD5	CPU: Running at 8.192MHz PLL oscillating mode*2 V_{DD}=5.0V		—	5	8		

*1: Case when the CPU operating rate is 100% (with no HALT state)

*2 : Significant bits of BLKCON0 to BLKCON4 registers are all “1”.

• DC Characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23)	VOL2	When LED drive mode is selected	IOL2 = +10mA $V_{DD} \geq$ 5.0V	—	—	0.5		
			IOL2 = +8mA $V_{DD} \geq$ 3.0V	—	—	0.5		
Output voltage 3 (P40 to P41) (P50 to P51)* (P60 to P61)* (P80 to P81)	VOL3	When I^2C mode is selected	IOL3 = +3mA $V_{DD} \geq$ 2.0V	—	—	0.4		
			IOL3 = +2mA 2.0V > $V_{DD} \geq$ 1.8V	—	—	VDD* 0.2		
Output leakage current (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		

*: ML620Q15X have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

• DC Characteristics (IIHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}	0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	–1500	–300	–20		
Input current 2 (P00 to P05)* (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IIH2	VIH2 = V_{DD} (when pulled down)	2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)	–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)	—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)	-1	—	—		

*: ML620Q15X have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

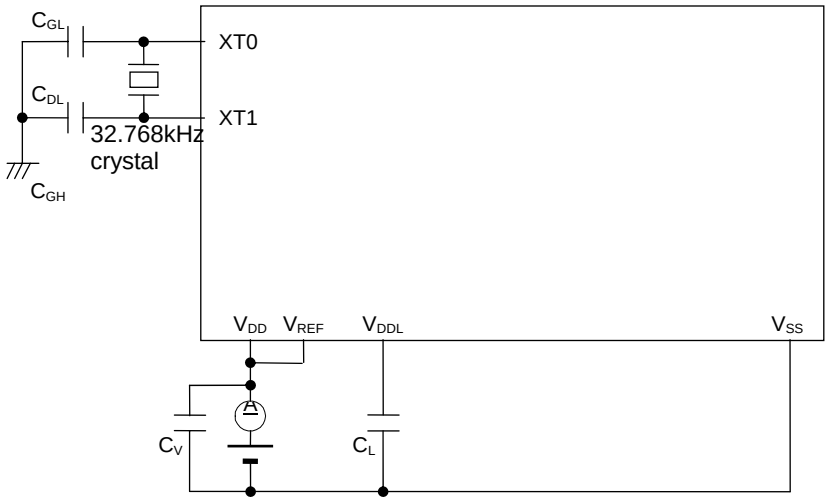
- DC Characteristics (VIHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Input pin capacitance (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

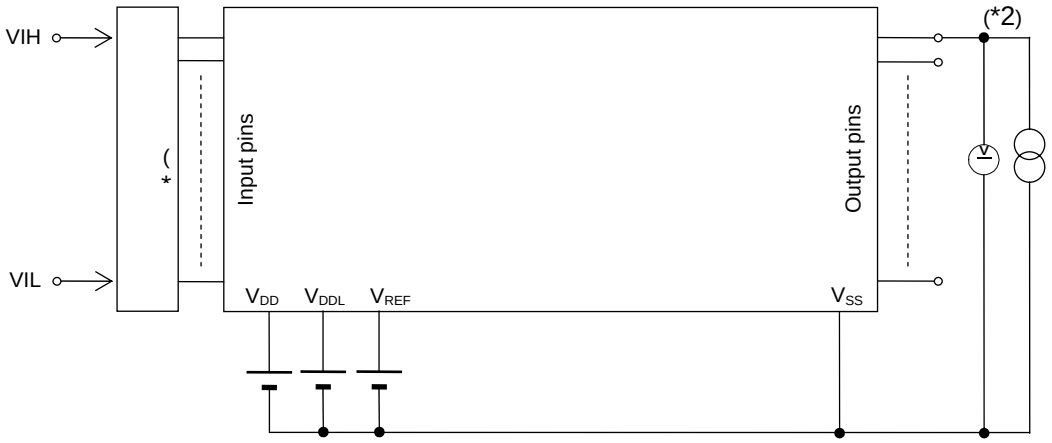
*: ML620Q15X have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

- Measuring circuit 1



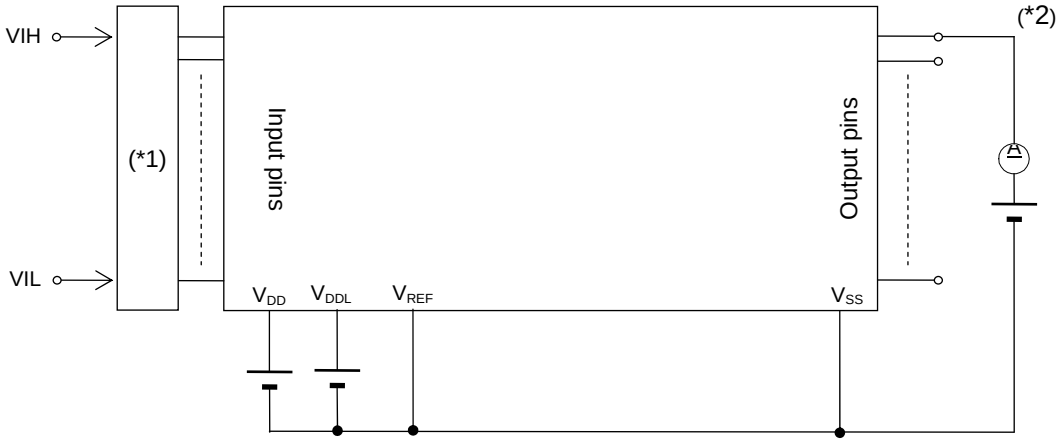
C_V : 2.2µF
C_L : 2.2µF
C_{GL} : 12pF
C_{DL} : 12pF
32.768kHz Crystal oscillator
(DT-26 DAISHINKU Corp.)

- Measuring circuit 2



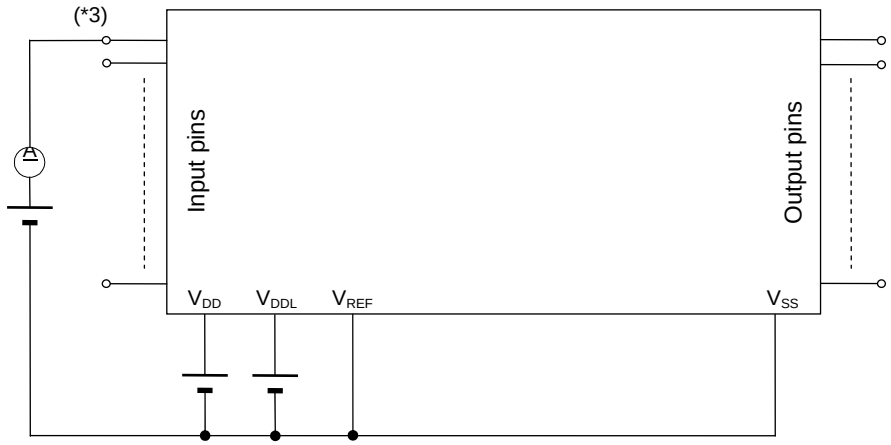
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

- Measuring circuit 3



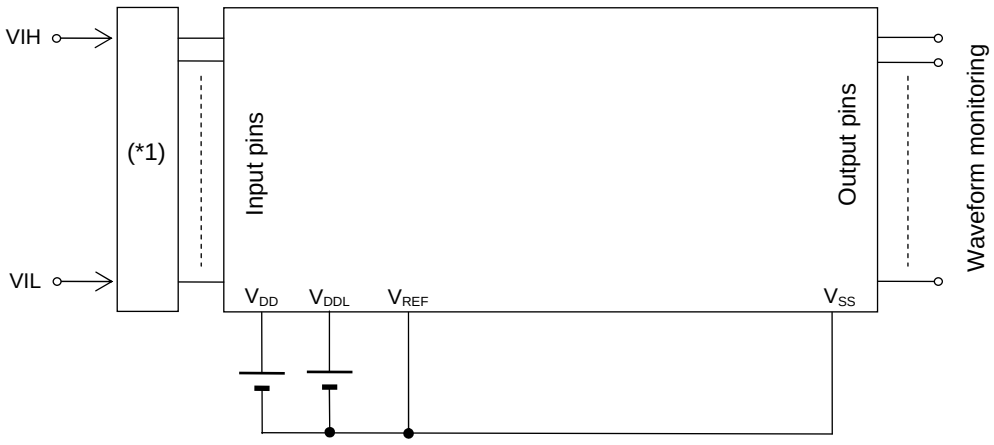
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

- Measuring circuit 4



*3: Measured at the specified input pins.

- Measuring circuit 5

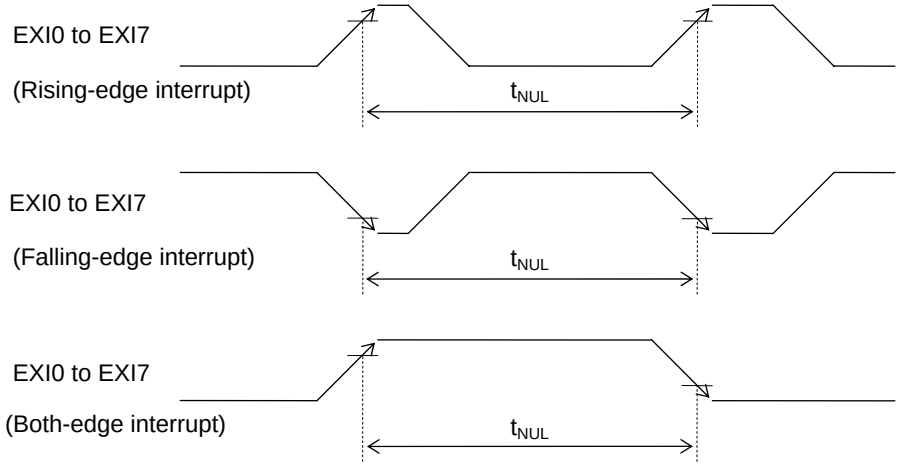


*1: Input logic circuit to determine the specified measuring conditions.

- AC Characteristics (External Interrupt)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× LSCLK	—	3.5× LSCLK	μs

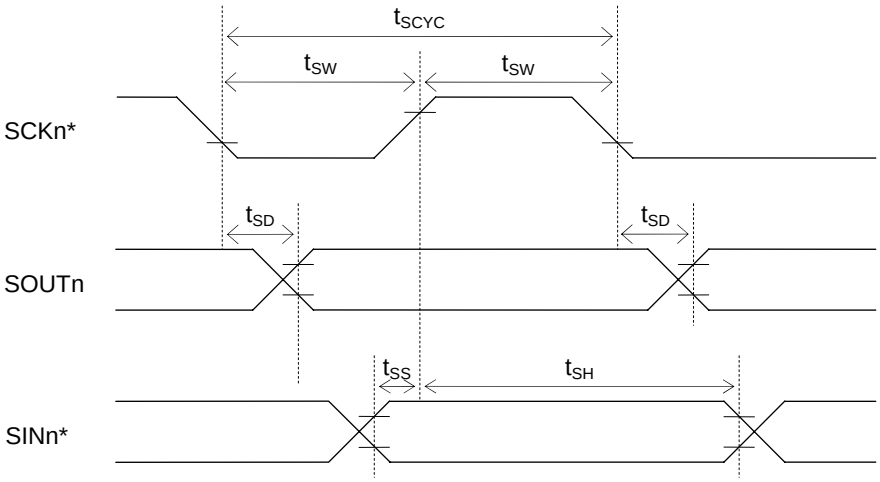


- AC Characteristics (Synchronous Serial Port)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (Master mode)	t_{SS}	—	240	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIOnMOD1)



*: Indicates the secondary function of the corresponding port.

•AC Characteristics (I^2C Bus Interface: Standard Mode 100kHz)

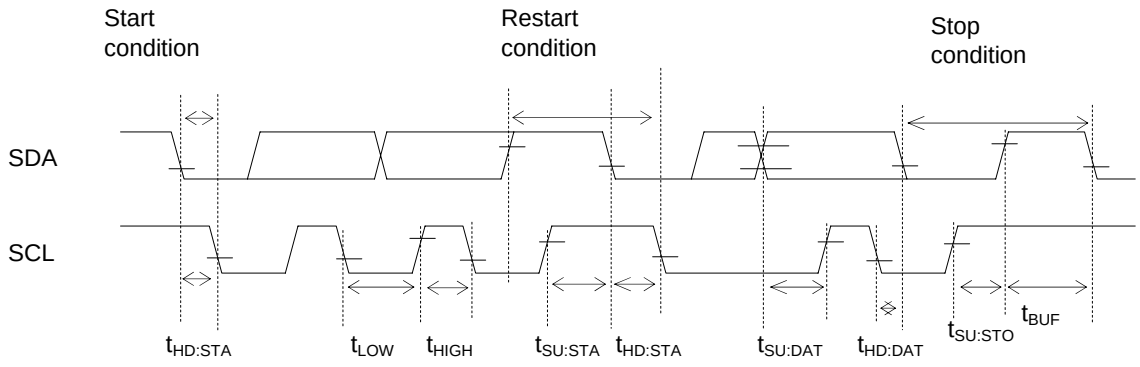
(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

•AC Characteristics (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

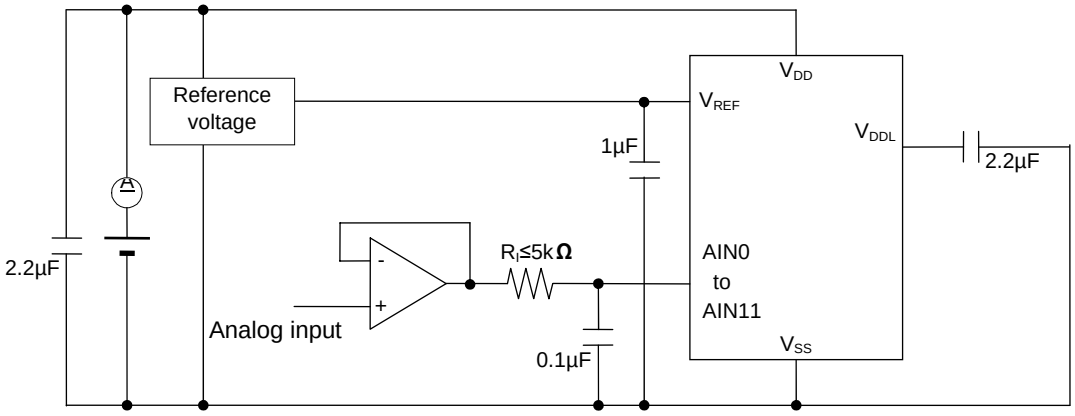
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



•Electrical Characteristics of Successive Approximation Type A/D Converter

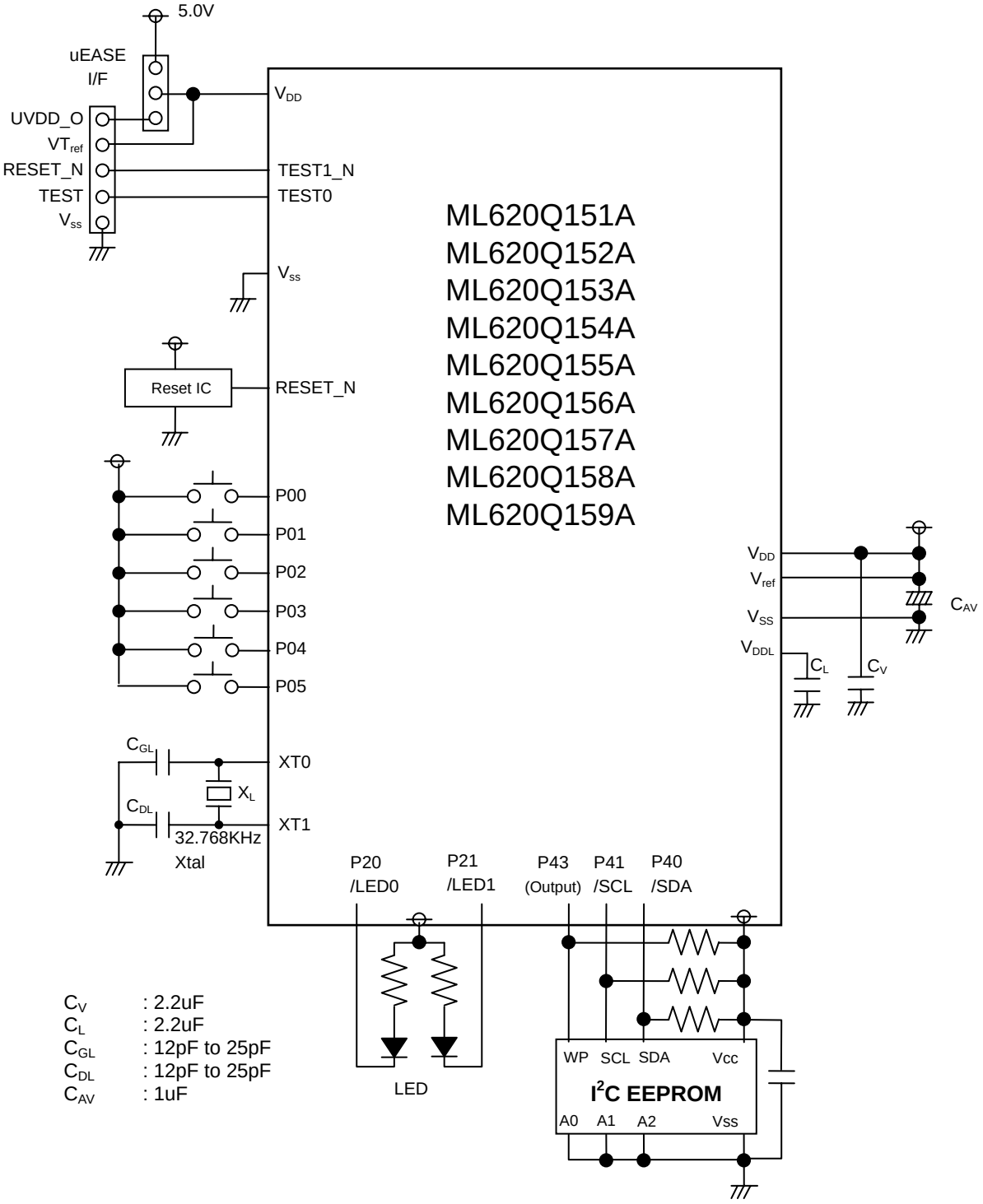
(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	INL	2.7V ≤ V_{REF} ≤ 5.5V	–4	—	+4	LSB
		2.2V ≤ V_{REF} < 2.7V	–6	—	+6	
		1.8V ≤ V_{REF} < 2.2V	–10	—	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	–3	—	+3	
		2.2V ≤ V_{REF} < 2.7V	–5	—	+5	
		1.8V ≤ V_{REF} < 2.2V	–9	—	+9	
Zero-scale error	V_{OFF}	RI ≤ 5kΩ	–6	—	+6	
Full-scale error	FSE	RI ≤ 5kΩ	–6	—	+6	
Input impedance	R_I	—	—	—	5k	Ω
A/D operating voltage	V_{REF}	V_{REF} ≤ V_{DD}	2.7	—	5.5	V
Conversion time	t_{CONV}	CPU works in PLL oscillation mode SACK bit = 0 2.7V ≤ V_{REF} ≤ 5.5V	—	13.5	—	µs
		CPU works in PLL oscillation mode SACK bit = 1 1.8V ≤ V_{REF} ≤ 5.5V	—	43	—	



Appendix D

Appendix D Application Circuit Example



Note:
Design the PCB layout having the shortest wiring distance between VDDL and VSS for noise reduction purpose.

Appendix E

Appendix E Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview

•About unused pins

[ ] Please confirm how to handle the unused pins(Refer to Section 1.3.4 in the user's manual).

Chapter 2 CPU and Memory Space

• Program Code size

[ ] 32,768 Byte (0:0000H to 0:7FFFH, ML620Q151A/ML620Q154A/ML620Q157A)
[ ] 49,152 Byte (0:0000H to 0:BFFFH, ML620Q152A/ML620Q155A/ML620Q158A)
[ ] 65,536 Byte (0:0000H to 0:FFFFH, ML620Q153A/ML620Q156A/ML620Q159A)

• Data Flash size

[ ] 2,048 Byte (7:0000H to 7:07FFH)

• Data RAM size

[ ] 2,048 Byte (0:E000H～0:E7FFH)

• Unused area

[ ] Please fill test area 0:7C00H to 0:7DFFH with BRK instruction code "0FFH" (ML620Q151A/ML620Q154A/ML620Q157A). Refer to a startup file "ML620151A.asm" or "ML620154A.asm" or "ML620157A.asm" for programming in the source code.
[ ] Please fill test area 0:BC00H to 0:BDFFH with BRK instruction code "0FFH" (ML620Q152A/ML620Q155A/ML620Q158A). Refer to a startup file "ML620152A.asm" or "ML620155A.asm" or "ML620158A.asm" for programming in the source code.
[ ] Please fill test area 0:FC00H to 0:FDFFH with BRK instruction code "0FFH" (ML620Q153A/ML620Q156A/ML620Q159A). Refer to a startup file "ML620153A.asm" or "ML620156A.asm" or "ML620159A.asm" for programming in the source code.
[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". Please fill the area with the code "0FFH" when you release a code for LAPIS Semiconductor's factory programming.

• Initializing RAM

[ ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Reset Function

• Reset activation pulse width

[ ] Minimum 100us (Refer to Appendix C-2 in the user's manual)

• BRK instruction reset

[ ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore initialize the SFRs by your software. (Refer to 3.3.1 in the user's manual)

Chapter 4 MCU Control Function

•STOP mode

[ ] When the MIE flag is "0", the stop code acceptor (STPACP) cannot be enabled under the condition where both the interrupt enable and request flags become "1" (Refer to Sections 4.2.2 and 4.2.3. in the user's manual).
[ ] Place two NOP instructions next to the instruction that sets the STP bit to "1" (Refer to Section 4.3.3. in the user's manual).

•HALT mode

[ ] Place two NOP instructions next to the instruction that sets the HLT bit to "1" (Refer to Section 4.3.2. in the user's manual).

•BLKCON register

[ ] BLKCON registers enable or disable corresponsive each peripheral (Refer to Section 4.2.4 - 4.2.9. in the user's manual).
[ ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

Chapter 5 Interrupts(INTs)

•Unused interrupt vector table

[ ] Please define all unused interrupt vector tables for fail safe.

•Non-maskable interrupt

[ ] The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE flag (Refer to Sections 5.2.10. and 5.3 in the User's Manual).

Chapter 6 Clock Generation Circuit

•Initial System clock

[ ] At power up or system reset, the 2.097MHz RC oscillation clock oscillates and approx. 262kHz clock which is 1/8 of 2.097MHz is supplied to CPU as the system clock.

•Switching high-speed clock operation mode to low-speed clock operation mode

[ ] When switching the high-speed clock to the low-speed clock after the recovery from the STOP mode, make sure the low-speed clock is oscillating by checking to see the low-speed time base counter's interrupt request bit becomes "1" (select T128Hz for one of QLTBC0~2).

•Port function setting

[ ] Specify the secondary function for the port 2 when driving a clock to the pin (Refer to Section 6.4 in the user's manual). (*)

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

Chapter 7 Time Base Counter

•How to read LTBC

[ ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Refer to Section 7.3.1 in the user's manual).

Chapter 8 8bit Timer

•How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 8.2.4 to 8.2.5 in the user's manual).

Chapter 9 16bit Timer

•How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 9.2.6 to 9.2.9 in the user's manual).

Chapter 10 Watchdog Timer

•Overflow period

Clear WDT during the selected overflow period:

[ ] 125ms, [ ] 500ms, [ ] 2s, [ ] 8s

•WDP

[ ] Check the WDP content before writing to the WDTCON register, then determine writing whether "5AH" or "0A5H" (Refer to Section 10.2.2. in the user’s manual).

Chapter 11 PWM

•Pins used

[ ] P20, P34, P43, P64 and/or P87 are used. (*)

[ ] P21, P35, P47, P65 and/or P83 are used. (*)

[ ] P22, P53, P60, P66 and/or P70 are used. (*)

[ ] P23, P57, P61 and/or P71 are used. (*)

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

•How to read the registers

[ ] Check notes for reading PWMn counter registers while the PWM is working (Refer to Sections 11.2.4, 11.2.14, 11.2.23 and 11.2.33 in the user's manual).

•Port function setting

[ ] Specify the tertiary or quaternary function for the port (Refer to Section 11.4 in the user’s manual).

Chapter 12 Synchronous Serial Port

•Pins used

[ ] Multiple ways to assign the pins(*): P40(SIN0), P41(SCK0), P42(SOUT0), P44(SIN0), P45(SCK0), P46(SOUT0), P50(SIN0), P51(SCK0), P52(SOUT0), P55(SIN0), P56(SCK0), P57(SOUT0), P72(SIN0), P73(SCK0), P74(SOUT0), P80(SIN0), P81(SCK0), P82(SOUT0), P84(SIN0), P85(SCK0), P86(SOUT0).

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

•Port function setting

[ ] Specify the tertiary function for the port (Refer to Section 12.4 in the user’s manual).

Chapter 13 UART

•Pins used

[ ] P02(RXD0), P42(RXD0), P54(RXD0) or P86(RXD0) is used. (*)

[ ] P03(RXD1), P52(RXD1), P72(RXD1) or P84(RXD1) is used. (*)

[ ] P43(TXD0), P55(TXD0), P73(TXD0) or P87(TXD0) is used. (*)

[ ] P43(TXD1), P53(TXD1), P55(TXD1), P73(TXD1) or P85(TXD1) is used. (*)

[ ] Select the P02, P42, P54 or P86 by specifying U0RSEL0 bit and R0RSEL1 bit of UA0MOD0 register.

[ ] Select the P03, P52, P72 or P84 by specifying U0RSEL0 bit and R0RSEL1 bit of UA1MOD0 register. (*)

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

•Port function setting

[ ] Specify the secondary or quaternary function for the port (Refer to Section 13.4 in the user’s manual).

Chapter 14 I^2C Bus Interface

•Pins used

[ ] P40(SDA), P50(SDA), P60(SDA) or P80(SDA) is used. (*)

[ ] P41(SCL), P51(SCL), P61(SCL) or P81(SCL) is used. (*)

[ ] Specify the secondary Function for the port(Refer to Section 13.4 in the user’s manual).

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

•Port function setting

[ ] Specify the secondary function for the port (Refer to Section 14.4 in the user’s manual).

Chapters 15 to 23 Port

•Pin Handling

[ ] Don’t leave Hi-impedance Input ports in floating state.

•Port function setting

[ ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port. (*)

(*) ML620Q150A series have a different pin configuration for each package. See the section 1.3.2 “LIST OF PINS” for more details.

Chapter 24 Successive Approximation Type A/D Converter

•Operating Conditions

[ ] Please confirm voltage of operation and a clock frequency.
HSCLK = 3MHz ~ 8.4MHz, AVDD=1.8V~5.5V

[ ] Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).

[ ] Do not start A/D conversion(set SARUN bit to “1”) with all of bits SACHB to SACH0 of the SADMOD0 register and the SADMOD1 register set to “0” (Refer to section 24.2.26 ~ 24.2.27 in the user's manual).

Chapter 26 LLD (Low Level Detector) Circuit

[ ] Please select the threshold voltage when the LLD circuit turns OFF.

Chapter 28 On-Chip Debug Function

• Operating Conditions

[ ] Supply a voltage from 3.0V to 5.5V to the VDD pin when programming (erasing and writing) the Flash ROM with LAPIS semiconductor development tool uEASE.

[ ] Please do not apply LSIs being used for debugging to mass production.

[ ] Please validate the ROM code on your production board without LAPIS semiconductor development tool uEASE.

Chapter 30 Code-Option

[ ] Set Code-option data into the test data area of program memory at the address 0:7DE0H (ML620Q151A/ML620Q154A/ML620Q157A) .
[ ] Set Code-option data into the test data area of program memory at the address 0:BDE0H (ML620Q152A/ML620Q155A/ML620Q158A) .
[ ] Set Code-option data into the test data area of program memory at the address 0:FDE0H (ML620Q153A/ML620Q156A/ML620Q159A) .
[ ] Fill the test data area with "0FFH" except for the code-option data are.

Appendix A SFR (Specific Function Registers)

•Initial value

[ ] Please confirm there are some SFRs have undefined initial value at reset (Refer to Appendix A in the user’s manual).

Appendix C Electrical Characteristics

•External capacitors for Power circuits

[ ] C_L=2.2uF （connected to V_{DDL} pin）, [ ] C_v =2.2uF (connected to V_{DD} pin）

•Operating voltage

[ ] +1.8V to +5.5V

•Operating temperature

[ ] -40°C to +105°C

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEU620Q150A-01	May 7, 2015	–	–	Fromal 1st Revision
FEU620Q150A-02	May 25, 2015	16-1, 16-4, 16-6, 28-1	16-1, 16-4, 16-6, 28-1	Add a notice about P14DIR bit.