

Test Procedure for the NCP1612GEVB Evaluation Board

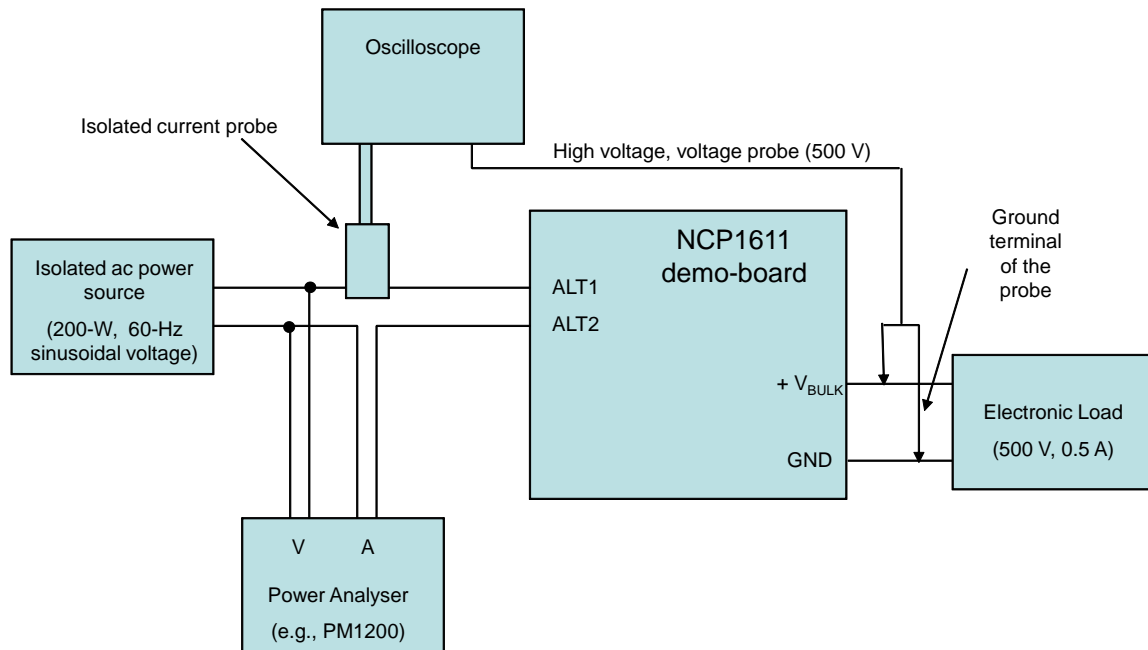


Figure 1 – Set-up for board testing

1. Equipments for measurement.

The board testing set-up is shown in Figure 1:

- Apply an electronic load across the output (between the V_{BULK} and “GND” terminals of the board). This equipment will adjust the current I_{LOAD} that loads the demo-board.
- Place a power analyzer able to measure the power factor (“PF”) and the Total Harmonic Distortion (“THD”) of the current absorbed from the ac power source.
- Apply a 200-W or more, 60-Hz, isolated ac power source between the “ALT1” and “ALT2” inputs of the demo-board. This source will adjust the sinusoidal input voltage, V_{in} , that is applied to the demo-board. The rms value of V_{in} must stay below 265 V.

2. Measurements



- **V_{BULK} , PF and THD measurements:**

Parameters	Comments	Limits
$V_{in,rms}=115\text{ V}$, $I_{LOAD}=0.1\text{ A}$		
V_{BULK}	Voltage measured between " V_{BULK} " and "GND"	$380\text{ V} < V_{BULK} < 400\text{ V}$
PF	Power Factor	> 0.950
THD	Total Harmonic Distortion	$< 15\%$
$V_{in,rms}=115\text{ V}$, $I_{LOAD}=0.4\text{ A}$		
V_{BULK}	Voltage measured between " V_{BULK} " and "GND"	$380\text{ V} < V_{BULK} < 400\text{ V}$
PF	Power Factor	> 0.990
THD	Total Harmonic Distortion	$< 15\%$
$V_{in,rms}=230\text{ V}$, $I_{LOAD}=0.4\text{ A}$		
V_{BULK}	Voltage measured between " V_{BULK} " and "GND"	$380\text{ V} < V_{BULK} < 400\text{ V}$
PF	Power Factor	> 0.950
THD	Total Harmonic Distortion	$< 20\%$

- **Brown-out levels:**

An external 12-V V_{CC} is applied. The load current being 0.1 A, set the input voltage to 82 Vrms and decrease the input voltage with 1-V steps of 1 s or more. The demo-board must still operate at 75 Vrms and turn off before reaching 70 Vrms.

The input voltage is increased from 70 Vrms with 1-V steps of 1 s or more, the PFC stage must stay off at 75 Vrms and recover operation at a voltage lower than 82 Vrms.

- **Skip.**

Observe the MOSFET drain-source voltage at 230 V / 50 Hz, 0.04-A load. There must be skip periods of time the duration of which must be between 2 and 7 ms (see Figure 2).

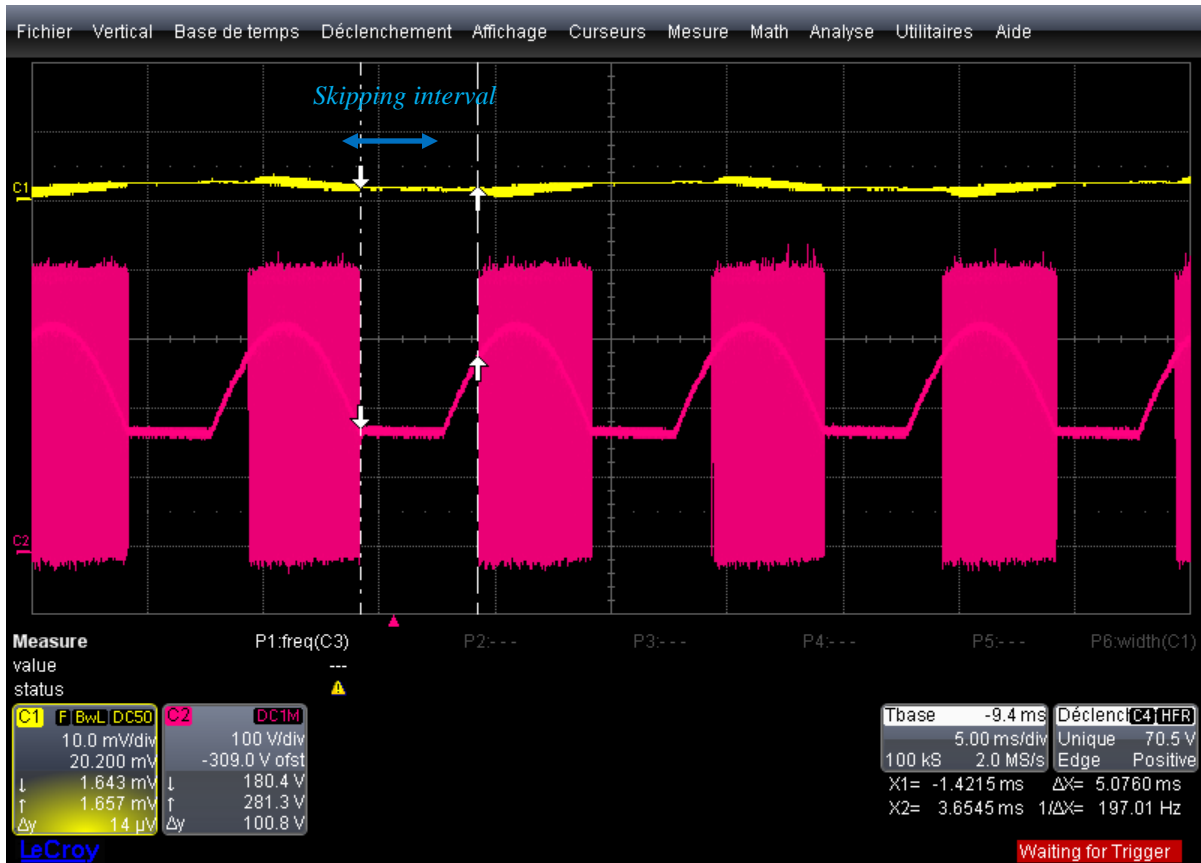


Figure 2 – MOSFET drain-source voltage ($V_{in,rms} = 230\text{ V}$, $I_{LOAD} = 0.04\text{ A}$)