PC7447A
PowerPC 7447A RISC Microprocessor

Datasheet

Features

- 3000 Dhrystone 2.1 MIPS at 1.3 GHz
- Selectable Bus Clock (30 CPU Bus Dividers up to 28x)
- Selectable MPx/60x Interface Voltage (1.8V, 2.5V)
- P_D Typically 18W at 1.33 GHz at V_{DD} = 1.3V; 8.0W at 1 GHz at V_{DD} = 1.1V Full Operating Conditions
- Nap, Doze and Sleep Power Saving Modes
- Superscalar (Four Instructions Fetched Per Clock Cycle)
- 4 GB Direct Addressing Range
- Virtual Memory: 4 Hexabytes (2^{52})
- 64-bit Data and 36-bit Address Bus Interface
- Integrated L1: 32 KB Instruction and 32 KB Data Cache
- Integrated L2: 512 KB
- 11 Independent Execution Units and three Register Files
- Write-back and Write-through Operations
- f_{INT} Max = 1.167 MHz
- f_{BUS} Max = 133 MHz/166 MHz

Description

The PC7447A host processor is a high-performance, low-power, 32-bit implementations of the PowerPC® Reduced Instruction Set Computer (RISC) architecture combined with a full 128-bit implementation of Freescale's AltiVec technology.

This microprocessor is ideal for leading-edge embedded computing and signal processing applications. The PC7447A features 512 KB of on-chip L2 cache. The PC7447A microprocessor has no backside L3 cache, allowing for a smaller package designed as a pin-for-pin replacement for the PC7447 microprocessor. This device benefits from a silicon-on-insulator (SOI) CMOS process technology, engineered to help deliver tremendous power savings without sacrificing speed. A low-power version of the PC7447A microprocessor is also available.

Figure 1-1 on page 2 shows a block diagram of the PC7447A. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit. The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to the main memory and other system resources.

Note that the PC7447A is a footprint-compatible, drop-in replacement in a PC7447 application if the core power supply is 1.3V.

Screening

- Full Military Temperature Range (T_J = -55°C, +125°C)
- Industrial Temperature Range (T_J = -40°C, +110°C)

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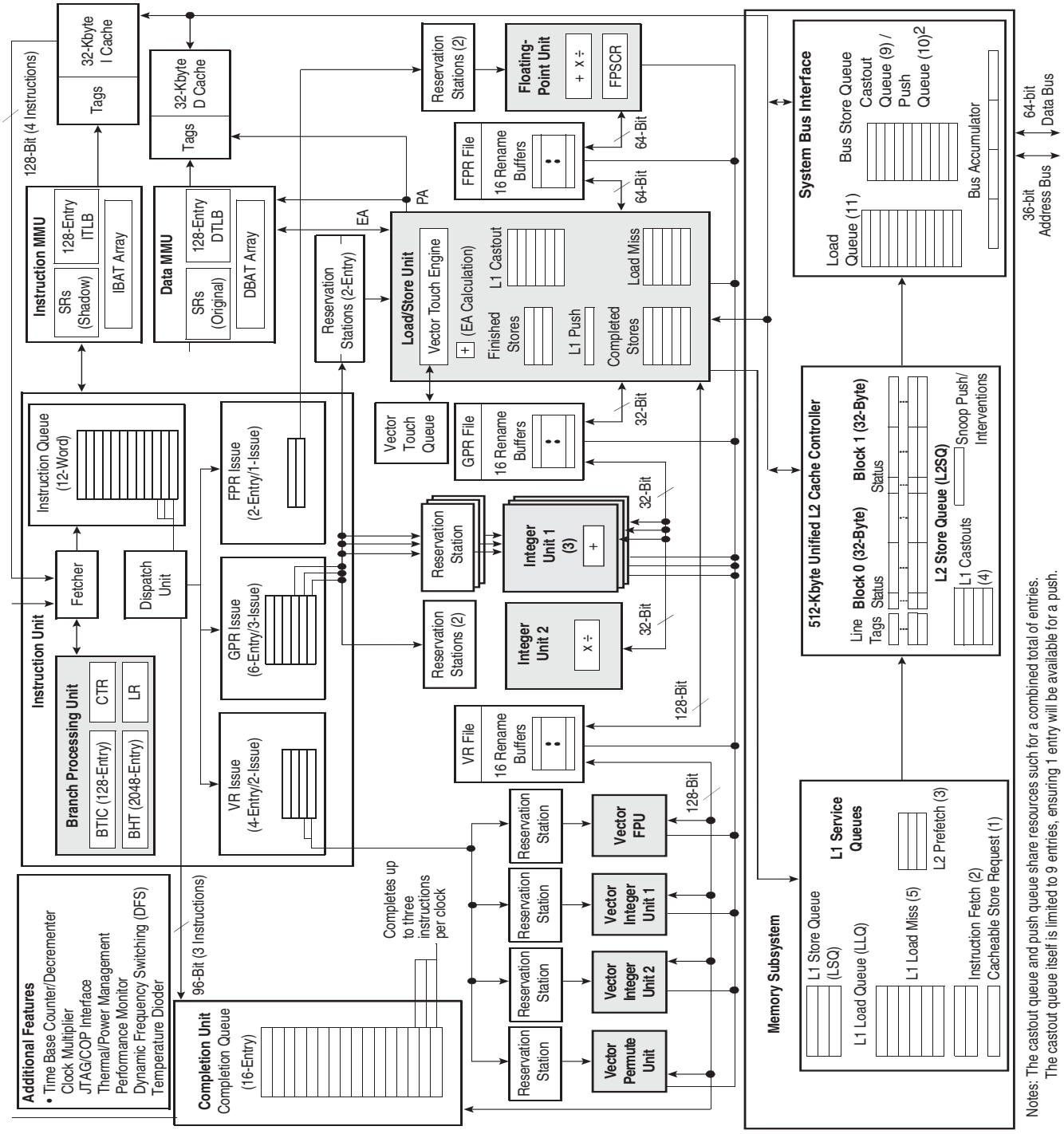
1. Block Diagram

Figure 1-1. PC7447A Microprocessor Block Diagram



Notes: The castout queue and push queue share resources such for a combined total of entries.
The castout queue itself is limited to 9 entries, ensuring 1 entry will be available for a push.

2. Features

This section summarizes features of the PC7447A implementation of the PowerPC architecture.

Major features of the PC7447A are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time
  - Up to 12 instructions can be in the instruction queue (IQ)
  - Up to 16 instructions can be at some stage of execution simultaneously
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.

    2048-entry branch history table (BHT) with two bits per entry for four levels of prediction: not taken, strongly not taken, taken, and strongly taken

    Up to three outstanding speculative branches

    Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream

    Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (BCLR) instructions

  - Four integer units (IUs) that share 32 GPRs for integer operands

    Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.

    IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.

  - Five-stage FPU and a 32-entry FPR file

    Fully IEEE® 754-1985-compliant FPU for both single- and double-precision operations

    Supports non-IEEE mode for time-critical operations

    Hardware support for denormalized number

Thirty-two 64-bit FPRs for single- or double-precision operands

– Four vector units and 32-entry vector register file (VRs)

Vector permute unit (VPU)

Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, vaddsbs, vaddshs, and vaddsws).

Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, vmhaddshs, vmhraddshs, and vmladduhm).

Vector floating-point unit (VFPU)

– Three-stage load/store unit (LSU)

Supports integer, floating-point, and vector instruction load/store traffic

Four-entry vector touch queue (VTQ) supports all four architectures of the AltiVec data stream operations

Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput

Four-cycle FPR load latency (single, double) with one-cycle throughput

No additional delay for misaligned access within double-word boundary
Dedicated adder calculates effective addresses (EAs)

Supports store gathering

Performs alignment, normalization, and precision conversion for floating-point data

Executes cache control and TLB instructions

Performs alignment, zero padding, and sign extension for integer data

Supports hits under misses (multiple outstanding misses)

Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  – Instructions can only be dispatched from the three lowest IQ entries: IQ0, IQ1, and IQ2
  – A maximum of three instructions can be dispatched to the issue queues per clock cycle
  – Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)

- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard Architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 512-Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - Cache write-back or write-through operation programmable on a per-page or per-block basis 64-byte, two-sectored line size
  - Parity support on cache
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address

  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation look aside buffers (TLBs)

    Both TLBs are 128-entry, two-way set-associative, and use a LRU replacement algorithm

    TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).
- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and the L2 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - A new dynamic frequency switching (DFS) feature allows the processor core frequency to be halved through software to reduce power consumption
  - The following three power-saving modes are available to the system:

    Nap: Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol.

    Sleep: Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.

    Deep sleep: When the part is in the deep Sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.

  - Instruction cache throttling provides control of instruction fetching to limit device temperature
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST), factory test only
- Reliability and serviceability
  - Parity checking on system bus
  - Parity checking on the L1 and L2 caches

3. General Parameters

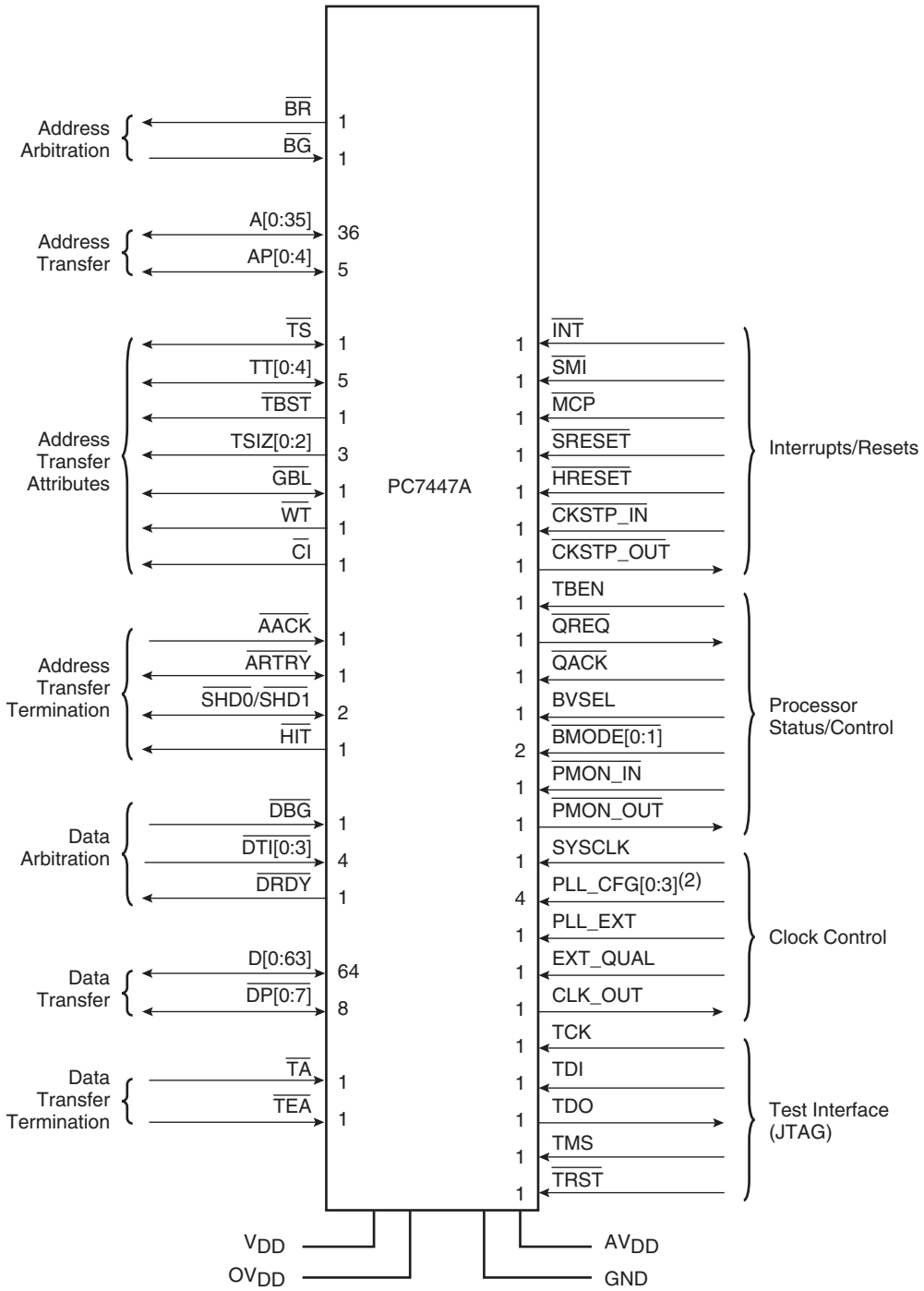
Table 3-1 provides a summary of the general parameters of the PC7447A.

Table 3-1. Device Parameters

Parameter	Description
Technology	0.13 µm CMOS, nine-layer metal
Die size	8.51 mm × 9.86 mm
Transistor count	48.6 million
Logic design	Fully-static
Packages	Surface mount 360 ceramic ball grid array (HITCE)
Core power supply	1.3V ± 50 mV and 1.1V ± 50 mV DC nominal
I/O power supply	1.8V ± 5% DC, or 2.5V ±5% DC

4. Signal Description

Figure 4-1. PC7447A Microprocessor Signal Groups



Note: For the PC7447A, there are 5 PLL_CFG signals, (PLL_CFG[0:4]

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7447A in compliance with e2v standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 8-1, Table 6-2 and Figure 4-1.

6.2 Absolute Maximum Ratings

The tables in this section describe the PC7447A DC electrical characteristics. Table 6-1 provides the absolute maximum ratings.

Table 6-1. Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
V_{IN}(6)(7)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 6-2 on page 10. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
3. Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to HRESET or 1, such that the bus is in 2.5V mode.
6. Caution: V_{IN} must not exceed OV_{DD} by more than 0.3V at any time including during power-on reset.
7. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration shown in Figure 6-1 on page 10.

6.3 Recommended Operating Conditions

Table 6-2 provides the recommended operating conditions for the PC7447A.

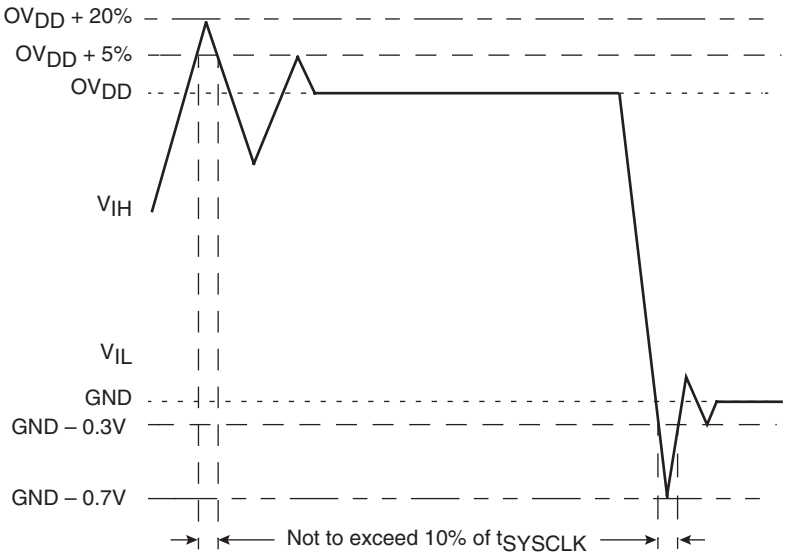
Table 6-2. Recommended Operating Conditions[1]

Symbol	Characteristic		Recommended Value		Unit
			Min	Max	
V_{DD}	Core supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
AV_{DD}[2]	PLL supply voltage		1.3V ± 50 mV or 1.1V ± 50 mV		V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8V ± 5%		V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	2.5V ± 5%		
V_{IN}	Input voltage	Processor bus	GND	OV_{DD}	V
V_{IN}		JTAG signals	GND	OV_{DD}	
T_J	Die-junction temperature		-55	125°C	°C

Notes: 1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2. This voltage is the input to the filter discussed in Section "PLL Power Supply Filtering" on page 41 and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

Figure 6-1. Overshoot/Undershoot Voltage



The PC7447A provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7447A core voltage must always be provided at a nominal 1.3V (see Table 6-2 on page 10 for the actual recommended core voltage). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OVDD power pins. Table 6-3 on page 11 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary.

Table 6-3. Input Threshold Voltage Setting[1]

BVSEL Signal	Processor Bus Input Threshold is Relative to:	Notes
0	1.8V	[2]
¬$\overline{\text{HRESET}}$	Not available	
$\overline{\text{HRESET}}$	2.5V	
1	2.5V	

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD} voltages supplied. See notes in Table 6-1 on page 9.
2. If used, pull-down resistors should be less than 250Ω.

6.4 Thermal Characteristics

6.4.1 Package Characteristics

Table 6-4. Package Thermal Characteristics[1]

Symbol	Characteristic	Value	Unit
$R_{\theta JA}$[2][3]	Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	26	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	19	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	20	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	16	°C/W
$R_{\theta JB}$[5]	Junction-to-board thermal resistance	10	°C/W
$R_{\theta JC}$[6]	Junction-to-case thermal resistance	< 0.1	°C/W

Notes: 1. See "Thermal Management Information" on page 12 for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between the die and the case top surface as measured with the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

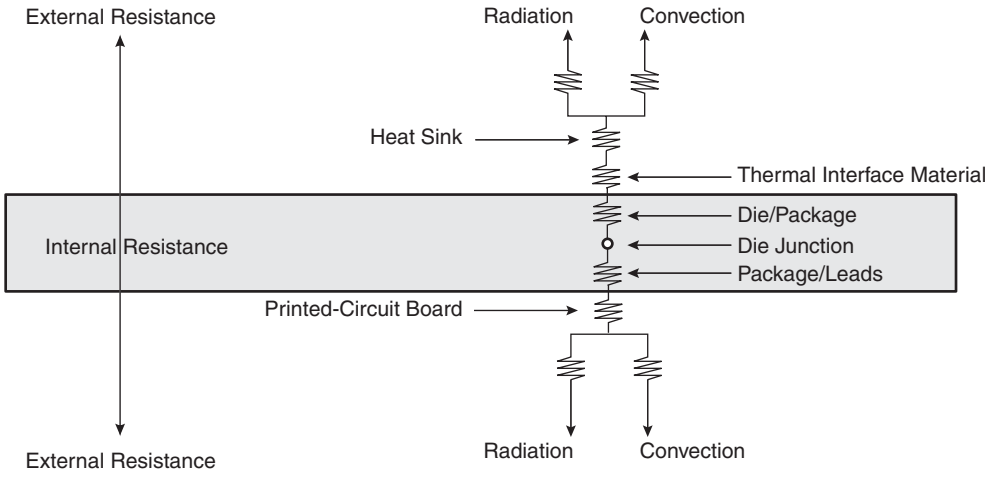
6.4.2 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 6-4 on page 11, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-ball thermal resistance

Figure 9-2 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

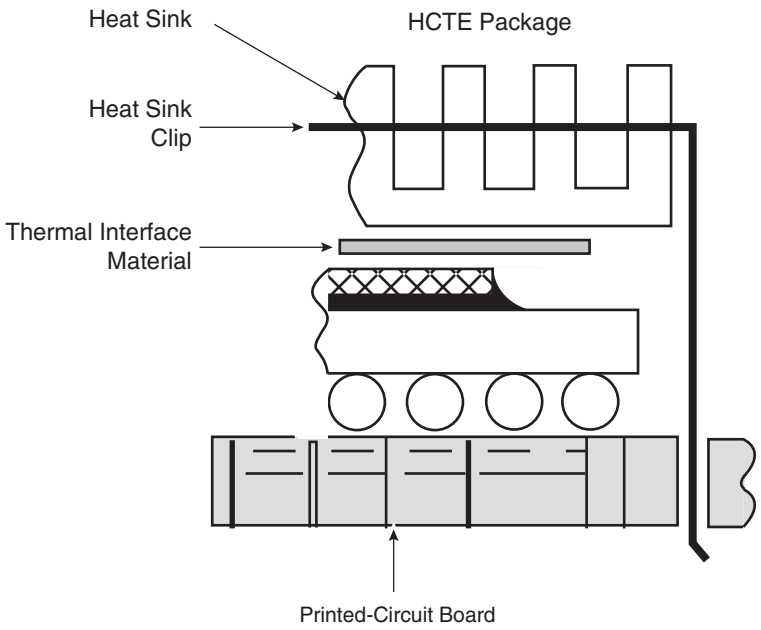
Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

6.4.3 Thermal Management Information

This section provides thermal management information for the high coefficient of the thermal expansion ceramic ball grid array (HITCE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design – the heat sink, airflow, and thermal interface material. The PC7447A implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Table 6-6 on page 19 for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see section “Temperature Diode” on page 16 for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods – spring clips to holes in the printed-circuit board or package, and mounting clips and screw assembly (see Figure 6-3); however, due to the potentially large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed ten pounds.

Figure 6-3. Package Exploded Cross-sectional View with Several Heat Sink Options



6.4.4 Thermal Interface Materials

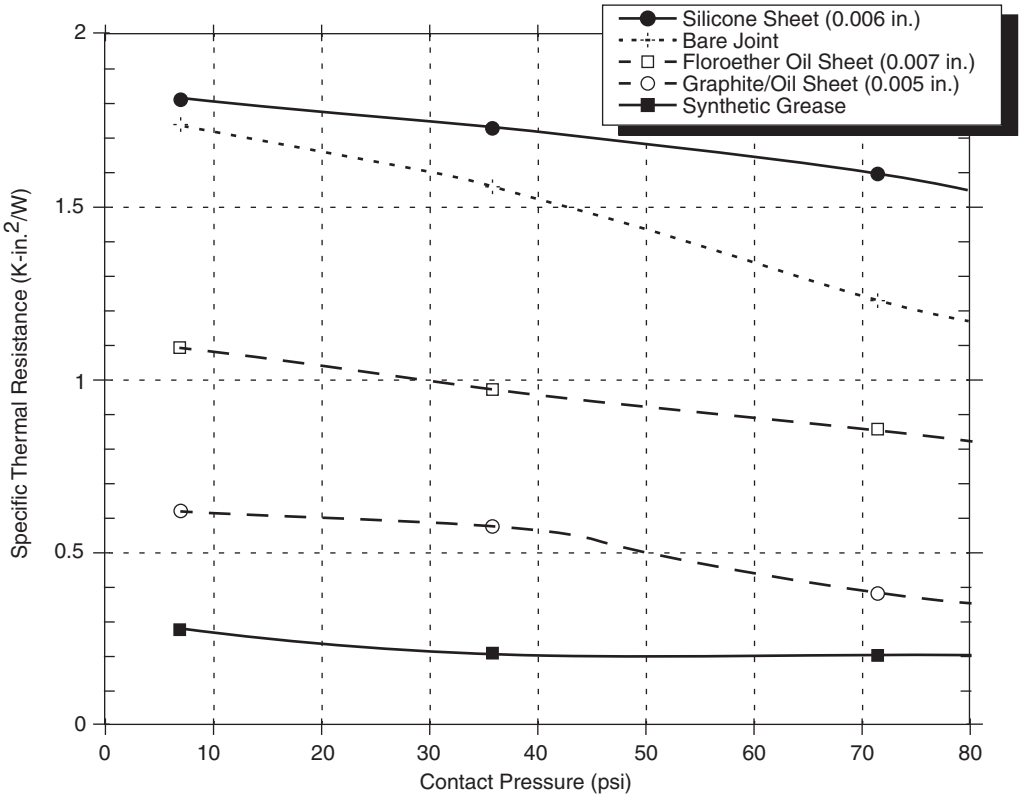
A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6-4 on page 14 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure.

As shown, the performance of these thermal interface materials improves with increasing contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 6-3 on page 13). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the PC7447A. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Figure 6-4. Thermal Performance of Select Thermal Interface Material



6.4.4.1 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in Table 6-2 on page 10. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, an HITCE package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7W, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 6-2 on page 10.

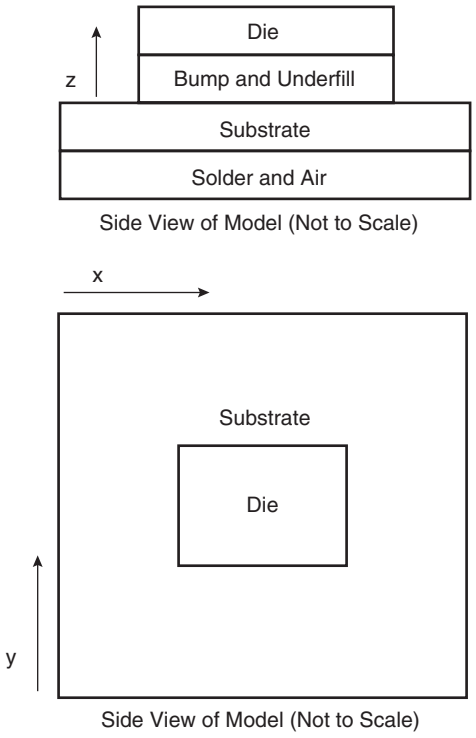
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature – airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the PC7447A thermal model is shown in Figure 6-5 on page 16. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die, and bump-underfill, have the same size as the die. The silicon die should be modeled 9.5 × 9.5 × 0.7 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 7.3 × 9.3 × 0.7 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m × K) in the xy-plane and 1.9 W/(m × K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm, and has 8.1 W/(m × K) isotropic conductivity in the xy-plane and 4 W/(m × K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and are 0.6 mm thick. They can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m × K) in the xy-plane direction and 3.8 W/(m × K) in the direction of the z-axis.

Figure 6-5. Recommended Thermal Model of PC7447A

Conductivity	Value	Unit
Bump and Underfill (7.3 x 9.3 x 0.070 mm)		
k_x	0.6	W/(m x K)
k_y	0.6	
k_z	1.9	
Substrate (25 x 25 x 1.2 mm)		
k_x	8.1	
k_y	8.1	
k_z	4.0	
Solder Ball and Air (25 x 25 x 0.6 mm)		
k_x	0.034	
k_y	0.034	
k_z	3.8	



6.4.4.2 Temperature Diode

The PC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices. These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC7447A's internal diode.

The following are the specifications of the PC7447A on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2 - 300 µA

Diode leakage < 10 nA at 125°C

Ideality factor over 5 µA – 150 µA at 60°C: 1 <= n <= TBD

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fW} = I_s\left[e^{\frac{qV_f}{nKT}} - 1\right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[In\frac{I_H}{I_L}\right]$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6×10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38×10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$V_H - V_L = 1.986 \times 10^{-4} \times nT$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1{,}986 \times 10^{-4}}$$

6.4.4.3 *Dynamic Frequency Switching (DFS)*

The new DFS feature in the PC7447A adds the ability to divide the processor-to-system bus ratio by two during normal functional operation by setting the HID1[DFS1] bit. The frequency change occurs in 1 clock cycle, and no idle waiting period is required to switch between modes. Additional information regarding DFS can be found in the MPC7450 RISC Microprocessor Family User's Manual.

6.4.4.4 *Power Consumption with DFS Enabled*

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}(P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 6-6 on page 19)

P_{DS} = Deep sleep mode power consumption (see Table 6-6 on page 19)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

6.4.4.5 *Bus-to-Core Multiplier Constraints with DFS*

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:4] during hard reset. Specifically, because the PC7447A does not support quarter clock ratios or the 1x multiplier, the DFS feature is limited to integer PLL multipliers of 4x and higher. The complete listing is shown in Table 6-5 on page 18.

Table 6-5. Valid Divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 12-1 on page 39)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
2x	N/A
3x	N/A
4x	2x
5x	2.5x
5.5x	2x
6x	3x
6.5x	N/A
7x	3.5x
7.5x	N/A
8x	4x
8.5x	N/A
9x	4.5x
9.5x	N/A
10x	5x
10.5x	N/A
11x	5.5x
11.5x	N/A
12x	6x
12.5x	N/A
13x	6.5x
13.5x	N/A
14x	7x
15x	7.5x
16x	8x
17x	8.5x
18x	9x
20x	10x
21x	10.5x
24x	12x
28x	14x

6.4.4.6 *Minimum Core Frequency Requirements with DFS*

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 9-2 on page 25. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

6.4.5 Power Consumption

Table 6-6 provides the power consumption for the PC7447A. For information regarding power consumption when dynamic frequency switching is enabled, See "Dynamic Frequency Switching (DFS)" on page 17.

Table 6-6. Power Consumption for PC7447A

	Processor (CPU) Frequency					
	1000	**1167**	**1267**	**1333**(5)	**1420**	**Unit**
Full-Power Mode						
Core Power Supply	1.1	1.1	1.3	1.3	1.3	
Typical(1)(2)	8	9.2	18.3	18	21	W
Maximum(1)(3)	11.5	13	26	25	30	W
Nap Mode						
Typical(1)(2)	1.3	1.3	4.1	3.3	4.1	W
Sleep Mode						
Typical(1)(2)	1.3	1.3	4.1	3.3	4.1	W
Deep Sleep Mode (PLL Disabled)						
Typical(1)(2)	1.2	1.2	4	3.2	4	W

Notes:
1. These values apply for all valid processor buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 6-2 on page 10) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz
3. Maximum power is the average measured at nominal V_{DD} and maximum operating junction temperature (see Table 6-2 on page 10) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Power consumption for these devices is artificially constrained during screening to assure lower power consumption than other speed grades.

7. Pin Assignment

Figure 7-1 shows the pinout of the PC7447A, 360 high coefficient of the thermal expansion ceramic ball grid array (HITCE) package as viewed from the top surface. Figure 7-2 shows the side profile of the HITCE package to indicate the direction of the top surface view.

Figure 7-1. Pinout of the PC7447A, 360 HITCE Package as Viewed from the Top Surface

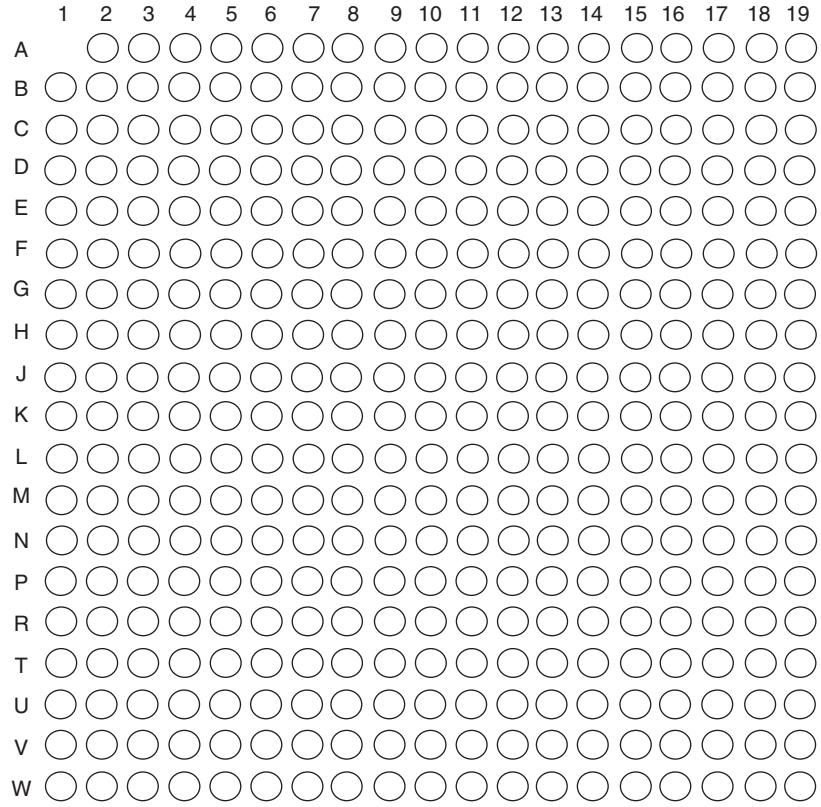
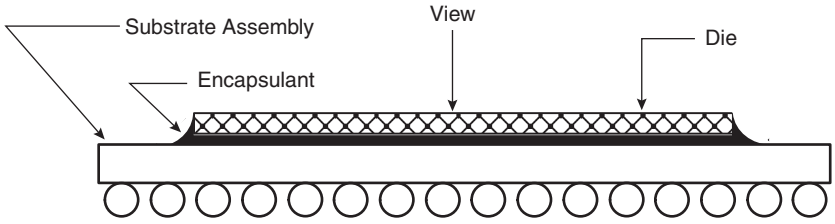


Figure 7-2. Side View of the CBGA Package



8. Pinout Listings

Table 8-1 provides the pinout listing for the PC7447A, 360 HITCE package. The pinouts of the PC7447A and PC7447 are pin compatible but there have been some changes. A PC7447A may be populated on a board designed for a PC7447 provided all pins defined as 'Not Connected' for the PC7447 are unterminated as required by the PC7457 RISC Microprocessor Specification. The PC7447A uses pins previously marked 'Not Connected' for the temperature diode pins and for additional power and ground connections. Because these 'Not Connected' pins in the PC7447 360 pin package are not driven in functional mode, a PC7447 can be populated in a PC7447A board. See section "Connection Recommendations" on page 41 for additional information.

Note: This pinout is not compatible with the PC750, PC7400, or PC7410 360 BGA package.

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package

Signal Name	Pin Number	Active	I/O	I/F Select(1)
A[0:35](2)	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL
AP[0:4](2)	C1, E3, H6, F5, G7	High	I/O	BVSEL
$\overline{\text{ARTRY}}$(3)	N2	Low	I/O	BVSEL
AV_{DD}	A8	–	Input	BVSEL
$\overline{\text{BG}}$	M1	Low	Input	BVSEL
$\overline{\text{BMODE0}}$(4)	G9	Low	Input	BVSEL
$\overline{\text{BMODE1}}$(5)	F8	Low	Input	BVSEL
$\overline{\text{BR}}$	D2	Low	Output	BVSEL
BVSEL(1)(6)	B7	High	Input	BVSEL
$\overline{\text{CI}}$(3)	J1	Low	Output	BVSEL
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL
CLK_OUT	H2	High	Output	BVSEL
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL
$\overline{\text{DRDY}}$(7)	R3	Low	Output	BVSEL
DTI[0:3](8)	G1, K1, P1, N1	High	Input	BVSEL
EXT_QUAL(9)	A11	High	Input	BVSEL
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	–	–	N/A
GND[15]	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	–	–	N/A
GND_SENSE[19]	G12, N13	–	–	N/A
$\overline{\text{HIT}}$[7]	B2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL
$\overline{\text{INT}}$	D4	Low	Input	BVSEL
L1_TSTCLK[9]	G8	High	Input	BVSEL
L2_TSTCLK[10]	B3	High	Input	BVSEL
No Connect[11]	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	–	–	–
$\overline{\text{LSSD\_MODE}}$[6][12]	E8	Low	Input	BVSEL
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	–	–	N/A
OV_{DD}_SENSE[16]	E18, G18	–	–	N/A
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[13]	D9	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	BVSEL
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1][3]	E4, H5	Low	I/O	BVSEL
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL
SYSCLK	A10	–	Input	BVSEL
$\overline{\text{TA}}$	K6	Low	Input	BVSEL
TBEN	E1	High	Input	BVSEL
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL
TCK	C6	High	Input	BVSEL
TDI[6]	B9	High	Input	BVSEL
TDO	A4	High	Output	BVSEL
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL
TEMP_ANODE[17]	N18			
TEMP_CATHODE[17]	N19			

Table 8-1. Pinout Listing for the PC7447A, 360 HITCE Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
TEST[0:3][12]	A12, B6, B10, E10	–	Input	BVSEL
TEST[4][9]	D10	–	Input	BVSEL
TMS[6]	F1	High	Input	BVSEL
$\overline{\text{TRST}}$[6][14]	A5	Low	Input	BVSEL
$\overline{\text{TS}}$[3]	L4	Low	I/O	BVSEL
TSIZ[0:2]	G6, F7, E7	High	Output	BVSEL
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	BVSEL
$\overline{\text{WT}}$[3]	D3	Low	Output	BVSEL
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	–	–	N/A
V_{DD}[15]	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	–	–	N/A
V_{DD}_SENSE[18]	G13, N12	–	–	N/A

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8V), or to $\overline{\text{HRESET}}$ or OV_{DD} (selects 2.5V); see Table 6-3 on page 11. If used, the pull-down resistor should be less than 250Ω. Because these settings may change in future products, it is recommended BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{IN} or supply voltages see Table 6-2 on page 10.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the PC7447A and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the PC7447A is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the PC7447, have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the PC7447. They may be left unconnected for backward compatibility with these devices, but it is recommended they be connected in new designs to facilitate future products. See section "Connection Recommendations" on page 41 for more information.
16. These pins were OV_{DD} pins on the PC7447. These pins are internally connected to OV_{DD} and are intended to allow an external device to detect the I/O voltage level present inside the device package. If unused, they must be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.

18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

Note: Caution must be exercised when performing boundary scan test operations on a board designed for a PC7447A but populated with an PC7447. This is because in the PC7447 it is possible to drive the latches associated with the former 'No Connect' pins in the PC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal PC7447 latches do not cause these pins to be driven during board testing.

9. Electrical Characteristics

9.1 Static Characteristics

Table 9-1 provides the DC electrical characteristics for the PC7447A.

Table 9-1. DC Electrical Specifications (see Table 6-2 on page 10 for Recommended Operating Conditions)

Symbol	Characteristic	Nominal Bus Voltage(1)	Min	Max	Unit	Notes
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)
I_{TSI}	High-impedance (off-state) leakage current, $V_{IN} = GV_{DD}/O_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)(4)
V_{OH}	Output high voltage at I_{OH} = -5 mA	1.8	OV_{DD} - 0.45	–	V	
		2.5	1.8	–		
V_{OL}	Output low voltage at I_{OL} = 5 mA	1.8	–	0.45	V	
		2.5	–	0.6		
C_{IN}	Capacitance, V_{IN} = 0V f = 1 MHz — All other inputs		–	8	pF	(5)
V_{IH}	Input high voltage (all inputs)	1.8	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
		2.5	1.7	$OV_{DD} + 0.3$		
V_{IL}	Input low voltage (all inputs)	1.8	-0.3	$OV_{DD} \times 0.35$	V	(2)(6)
		2.5	-0.3	0.7		
I_{IN}	Input leakge current, $V_{IN} = GV_{DD}/OV_{DD}$ V_{IN} = GND	–	–	30 -30	µA	(2)(3)

Notes: 1. Nominal voltages; see Table 6-2 on page 10 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.

3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Excludes signals with internal pull ups: BVSEL, $\overline{\text{LSSD\_MODE}}$, TDI, TMS, and $\overline{\text{TRST}}$. Characterization of leakage current for these signals is currently being conducted.

9.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7447A. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section "Clock AC Specifications" on page 25 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals, and can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; See "Ordering Information" on page 46. for information on ordering parts. DFS is described in Section "Dynamic Frequency Switching (DFS)" on page 17.

9.2.1 Clock AC Specifications

Table 9-2 provides the clock AC timing specifications as defined in Figure 9-1 on page 26 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 9-2 on page 25 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7447A will be a function of the AC timings of the PC7447A, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 9-2 on page 25.

Table 9-2. Clock AC Timing Specifications (See Table 6-2 on page 10 for Recommended Operating Conditions)

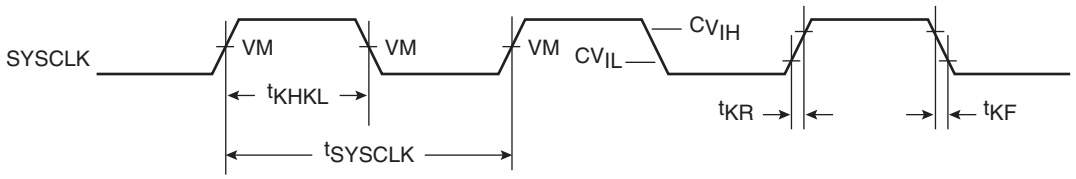
		Maximum Processor Core Frequency									
		1000 MHz		1267 MHz		1333 MHz		1420 MHz			
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3		V_{DD} = 1.3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
f_{CORE}	Processor core frequency	600	1000	600	1267	600	1333	600	1420	MHz	(1)(8)(9)
f_{VCO}	VCO frequency	1200	2000	1200	2533	1200	2667	1200	2840	MHz	(1)(9)
f_{SYSCLK}	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz	(1)(2)(8)
t_{SYSCLK}	SYSCLK cycle time	6.0	30	6	30	6	30	6	30	ns	(2)
t_{KR}, t_{KF}	SYSCLK rise and fall time	–	1.0	–	1	–	1	–	1	ns	(3)
t_{KHKL}/t_{SYSCLK}	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%	(4)
	SYSCLK jitter(5)(6)	–	150	–	150	–	150	–	150	ps	(5)(6)
	Internal PLL relock time(7)	–	100	–	100	–	100	–	100	µs	(7)

Symbol	Characteristic	Maximum Processor Core Frequency				Unit	Notes
		1000 MHz		1167 MHz			
		V_{DD} = 1.1V		V_{DD} = 1.1V			
		Min	Max	Min	Max		
f_{CORE}	Processor core frequency	500	1000	500	1167	MHz	(1)(8)(9)
f_{VCO}	VCO frequency	1000	2000	1000	2233	MHz	(1)(9)
f_{SYSCLK}	SYSCLK frequency	33	167	33	167	MHz	(1)(2)(8)
t_{SYSCLK}	SYSCLK cycle time	6	30	6	30	ns	(2)
t_{KR}, t_{KF}	SYSCLK rise and fall time	–	1	–	1	ns	(3)
t_{KHKL}/t_{SYSCLK}	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	%	(4)
	SYSCLK jitter(5)(6)	–	150	–	150	ps	(5)(6)
	Internal PLL relock time(7)	–	100	–	100	µs	(7)

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section "PLL Configuration" on page 38 for valid PLL_CFG[0:4] settings.
2. Assumes a lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time during the power-on reset sequence.
8. Caution: If DFS is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.
9. Caution: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced.

Figure 9-1 provides the SYSCLK input timing diagram.

Figure 9-1. SYSCLK Input Timing Diagram



V_M = Midpoint Voltage ($OV_{DD}/2$)

9.2.2 Processor Bus AC Specifications

Table 9-3 provides the processor bus AC timing specifications for the PC7447A as defined in Figure 7-2 on page 20 and Figure 9-2 on page 28..

Table 9-3. Processor Bus AC Timing Specifications[1] (at Recommended Operating Conditions, see Table 6-2 on page 10.)

Symbol[2]	Parameter	All Speed Grades		Unit
		Min	Max	
	Input setup times:			
t_{AVKH}	A[0:35], AP[0:4]	1.8	–	ns
t_{DVKH}	D[0:63], DP[0:7]	1.8	–	
t_{IVKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1],	1.8	–	
t_{MVKH}[8]	$\overline{BMODE}$[0:1], BVSEL	1.8	–	
	Input hold times:			
t_{AXKH}	A[0:35], AP[0:4]	0	–	ns
t_{DXKH}	D[0:63], DP[0:7]	0	–	
t_{IXKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1]	0	–	
t_{MXKH}[8]	BMODE[0:1], BVSEL	0	–	
	Output valid times:			
t_{KHAV}	A[0:35], AP[0:4]	–	2	ns
t_{KHDV}	D[0:63], DP[0:7]	–	2	
t_{KHOV}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3], $\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	–	2	
	Output hold times:			
t_{KHAX}	A[0:35], AP[0:4]	0.5	–	ns
t_{KHDX}	D[0:63], DP[0:7]	0.5	–	
t_{KHOX}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3], $\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	0.5	–	
t_{KHOE}[5]	SYSCLK to output enable	0.5	–	ns
t_{KHOZ}[5]	SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	–	3.5	ns
t_{KHTSPZ}[3][4][5]	SYSCLK to $\overline{TS}$ high impedance after precharge	–	1	t_{SYSCLK}
t_{KHARP}[3][5][6][7]	Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	–	1	t_{SYSCLK}
t_{KHARPZ}[3][5][6][7]	SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	–	2	t_{SYSCLK}

Notes: 1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 7-2 on page 20). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 9-3 on page 29. The nominal precharge width for $\overline{TS}$ is $0.5 \times t_{SYSCLK}$, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{TS}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for 1 clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 9-3 on page 29 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning the cycle of $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 9-2 on page 28 for sample timing.

Figure 9-2 provides the mode select input timing diagram for the PC7447A. The mode select inputs are sampled twice, once before and once after $\overline{HRESET}$ negation.

Figure 9-2. Mode Input Sample Timing Diagram

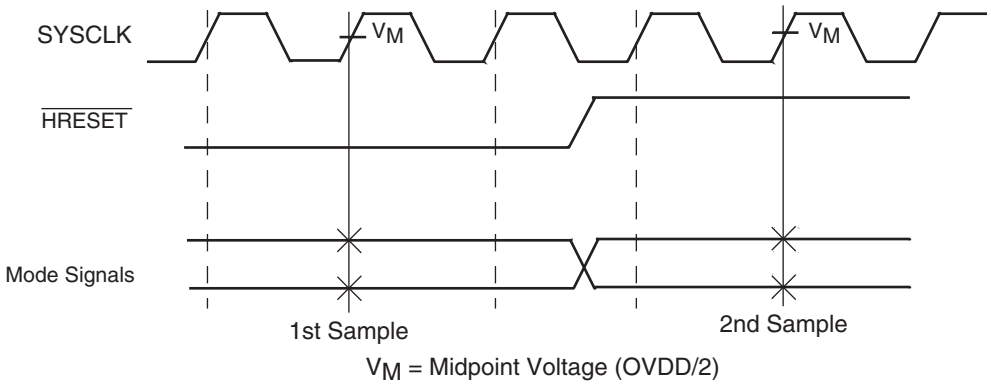
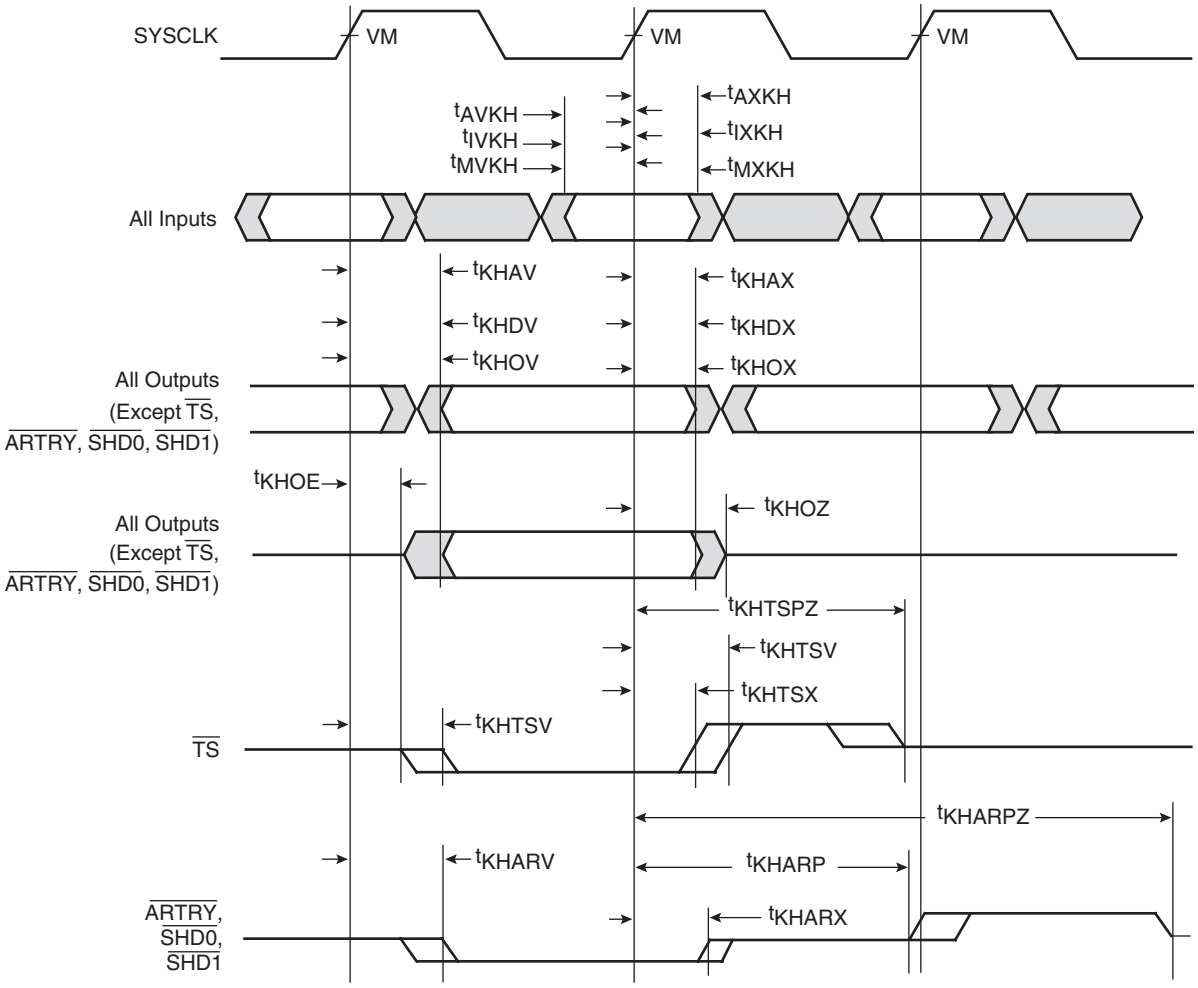


Figure 9-3 provides the input/output timing diagram for the PC7447A.

Figure 9-3. Input/Output Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

9.2.3 IEEE 1149.1 AC Timing Specifications

Table 9-4 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 9-5 through Figure 9-8 on page 32.

Table 9-4. JTAG AC Timing Specifications (Independent of SYSCLK)(1) at Recommended Operating Conditions (see Table 6-2 on page 10)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30	–	ns
t_{JHJL}	TCK clock pulse width measured at 1.4V	15	–	ns
t_{JR} and t_{JF}	TCK rise and fall times	–	2	ns
t_{TRST}(2)	$\overline{TRST}$ assert time	25	–	ns
t_{DVJH}(3) t_{IVJH}	Input Setup Times: Boundary-scan data TMS, TDI	 4 0	 – –	ns
t_{DXJH}(3) t_{IXJH}	Input Hold Times: Boundary-scan data TMS, TDI	 20 25	 – –	ns
t_{JLDV}(4) t_{JLOV}	Valid Times: Boundary-scan data TDO	 4 4	 20 25	ns
t_{JLDX}(4) t_{JLOX}	Output hold times: Boundary-scan data TDO	 30 30	 – –	
t_{JLDZ}(4)(5) t_{JLOZ}	TCK to output high impedance: Boundary-scan data TDO	 3 3	 19 9	ns

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 9-4). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 9-4 provides the AC test load for TDO and the boundary-scan outputs of the PC7457.

Figure 9-4. Alternate AC Test Load for the JTAG Interface

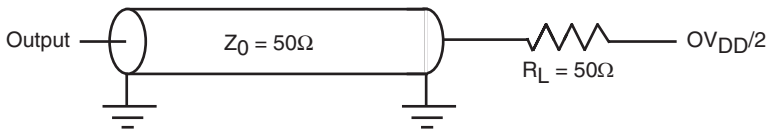
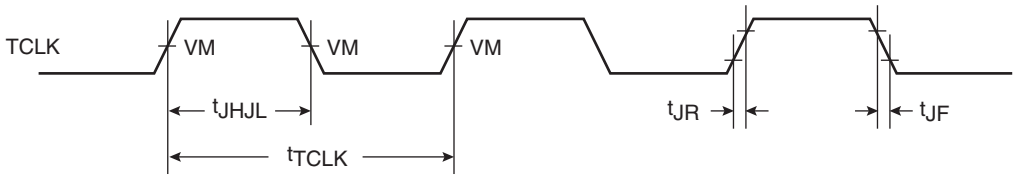
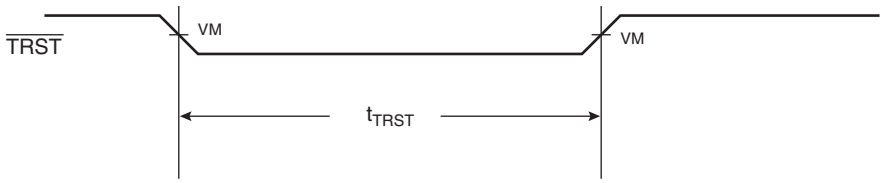


Figure 9-5. JTAG Clock Input Timing Diagram



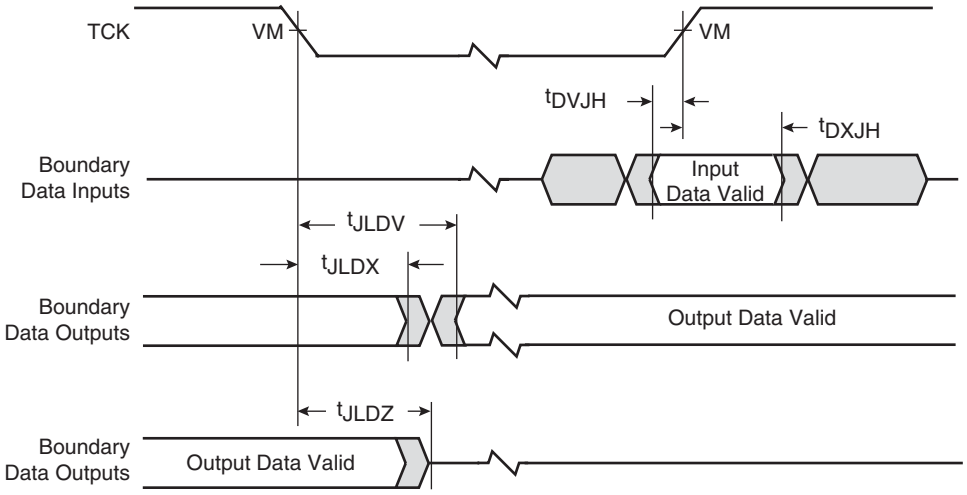
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 9-6. $\overline{\text{TRST}}$ Timing Diagram



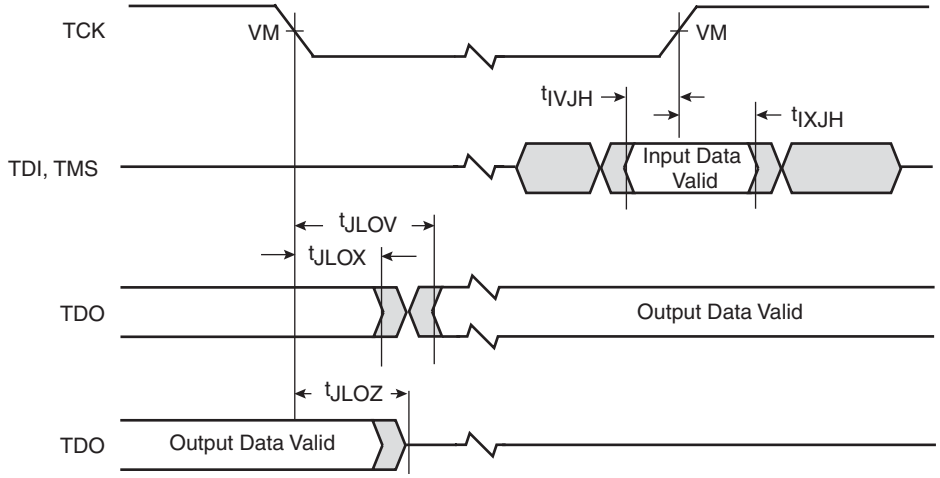
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 9-7. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 9-8. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

10. Preparation for Delivery

10.1 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces
- Ground test equipment, tools and operator
- Do not handle devices by the leads
- Store devices in conductive foam or carriers
- Avoid use of plastic, rubber or silk in MOS areas
- Maintain relative humidity above 50% if practical

11. Package Mechanical Data

The following sections provide the package parameters and mechanical dimensions for the HITCE package.

11.1 Package Parameters for the PC7447A, 360 HITCE

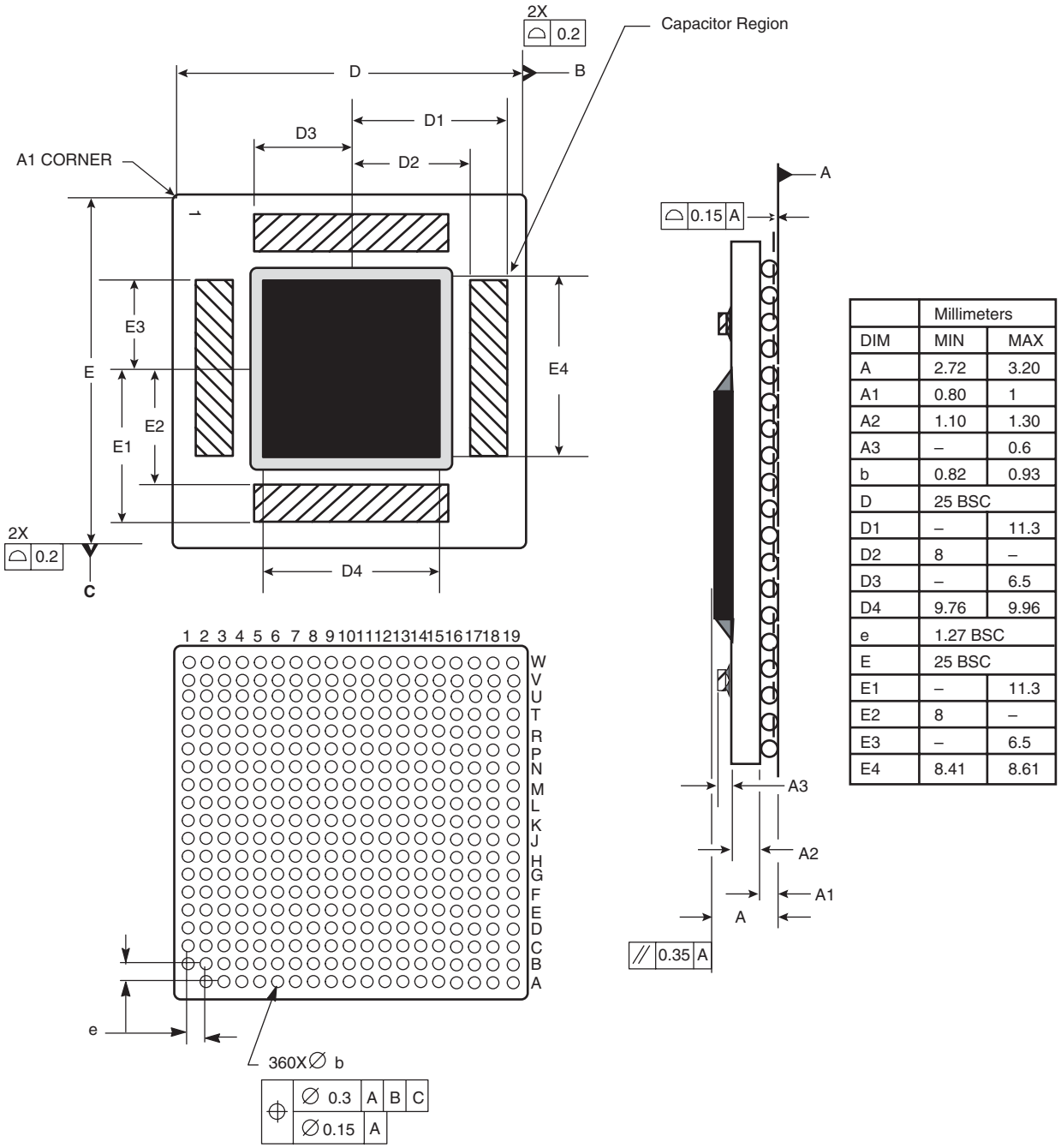
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of the thermal expansion ceramic ball grid array (HITCE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.24 mm
Ball diameter	0.89 mm (35 mil)

11.2 Mechanical Dimensions for the PC7447A, 360 HITCE

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7447A, 360 HITCE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7447A, 360 CBGA Package



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1
A2	1.10	1.30
A3	–	0.6
b	0.82	0.93
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	9.76	9.96
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	8.41	8.61

Notes:
1. Dimensioning and tolerance per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

11.3 Package Parameters for the PC7447A, 360 HITCE RoHS-Compliant BGA

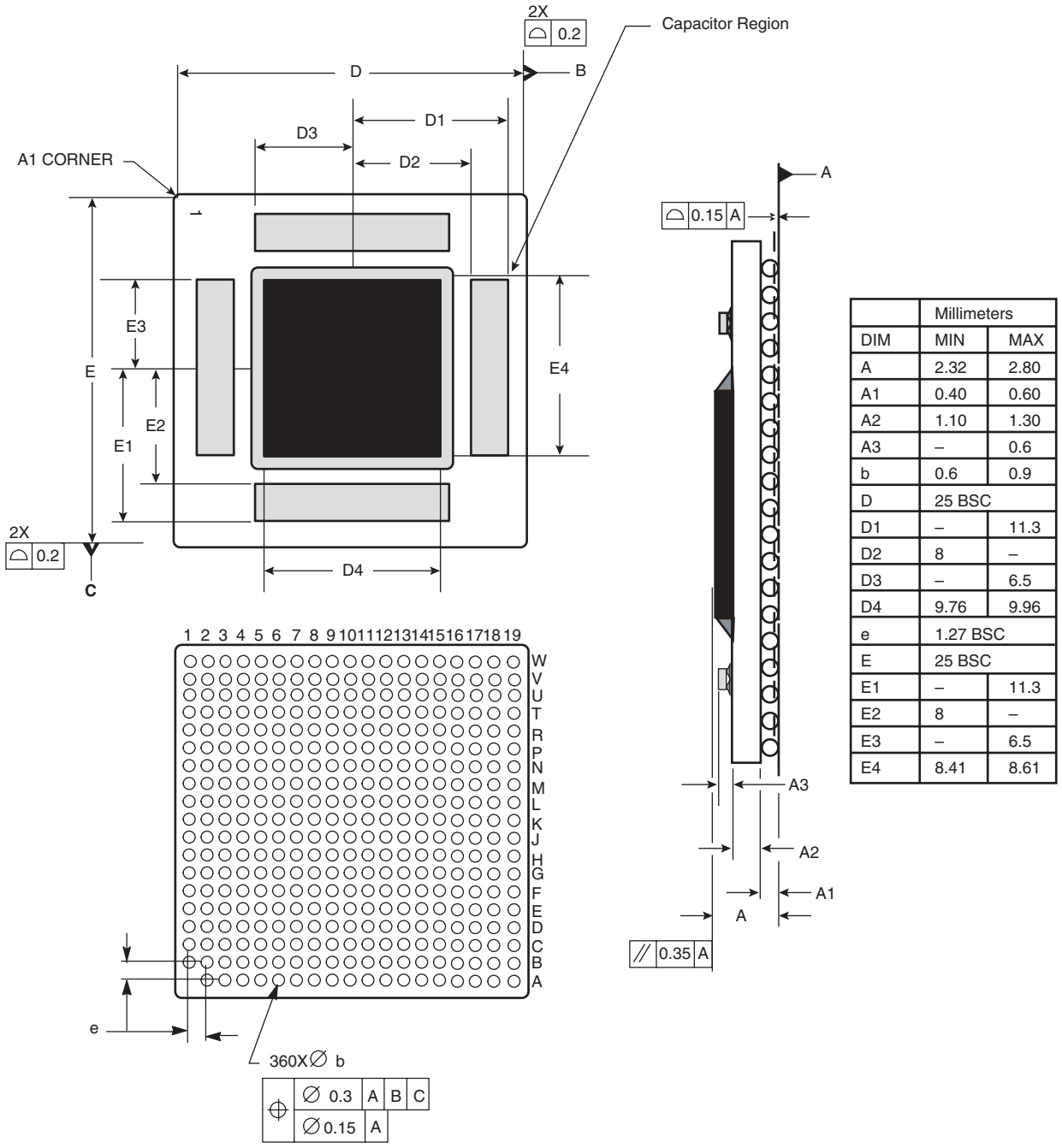
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 lead-free high coefficient of thermal expansion ceramic ball grid array (HITCE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

11.4 Mechanical Dimensions for the PC7447A, 360 HITCE RoHS-Compliant BGA

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7447A, 360 HITCE BGA package.

Figure 11-2. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7447A, 360 HITCE RoHS-Compliant BGA Package



	Millimeters	
DIM	MIN	MAX
A	2.32	2.80
A1	0.40	0.60
A2	1.10	1.30
A3	–	0.6
b	0.6	0.9
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	9.76	9.96
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	8.41	8.61

11.5 Package Parameters for the PC7447A, 360 HCTE LGA

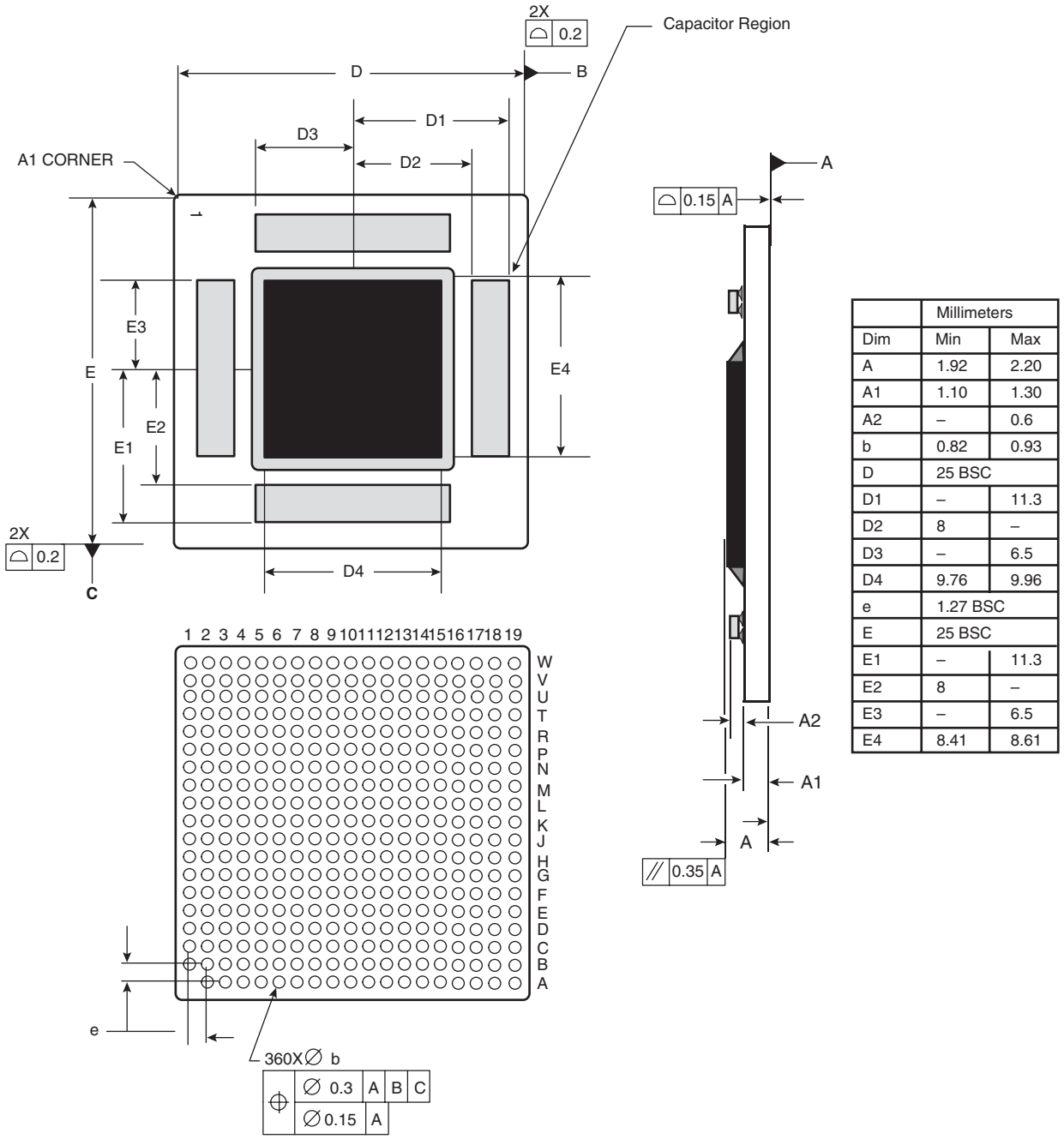
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3 ppm/°C

11.6 Mechanical Dimensions for the MPC7447A, 360 HCTE LGA

Figure 11-3 provides the mechanical dimensions and bottom surface nomenclature for the PC7447A, 360 HCTE LGA package.

Figure 11-3. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7447A, 360 HITCE LGA Package

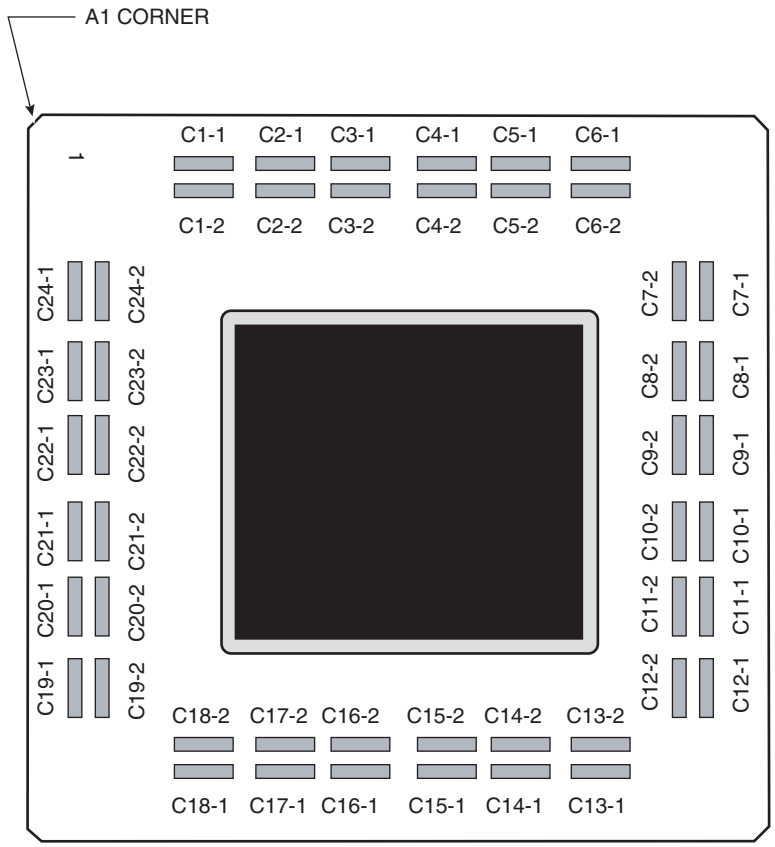


	Millimeters	
Dim	Min	Max
A	1.92	2.20
A1	1.10	1.30
A2	–	0.6
b	0.82	0.93
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	9.76	9.96
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	8.41	8.61

11.7 Substrate Capacitors for the PC7447A, 360 HITCE

Figure 11-4 shows the connectivity of the substrate capacitor pads for the PC7447A, 360 HITCE. All capacitors are 100 nF.

Figure 11-4. Substrate Bypass Capacitors for the PC7447A, 360 HITCE



Capacitor	Pad Number	
	-1	-2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	V_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	OV_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	OV_{DD}
C24	GND	V_{DD}

12. System Design Information

This section provides system and thermal design recommendations for successful application of the PC7447A.

12.1 PLL Configuration

The PC7447A PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC7447A is shown in Table 12-1 on page 39 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1400 MHz column in Table 9-2 on page 25. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving the bus-to-core multiplier; see section "Dynamic Frequency Switching (DFS)" on page 17 for more information.

Note that when DFS is enabled the resulting core frequency must meet the minimum core frequency requirements described in Table 9-2 on page 25.

Table 12-1. PC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts

	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
			Bus (SYSCLK) Frequency							
PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	33.33 MHz	50 MHz	66.66 MHz	75 MHz	83 MHz	100 MHz	133.33 MHz	166.66 MHz
01000	2x	2x								
10000	3x	2x								
10100	4x	2x								667 (1333)
10110	5x	2x							667 (1333)	835 (1670)
10010	5.5x	2x							733 (1466)	919 (1837)
11010	6x	2x						600 (1200)	800 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	866 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	1000 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	1336 (2672)
01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	1417 (2833)
01111	9x	2x			600 (1200)	675 (1350)	747 (1494)	900 (1800)	1197 (2394)	
01110	9.5x	2x			633 (1266)	712 (1524)	789 (1578)	950 (1900)	1264 (2528)	
10101	10x	2x			667 (1333)	750 (1500)	830 (1660)	1000 (2000)	1333 (2667)	
10001	10.5x	2x			700 (1400)	938 (1876)	872 (1744)	1050 (2100)	1397 (2793)	
10011	11x	2x			733 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			766 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)	1200 (2400)		

Table 12-1. PC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts (Continued)

PLL_CFG[0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus (SYSCLK) Frequency							
			33.33 MHz	50 MHz	66.66 MHz	75 MHz	83 MHz	100 MHz	133.33 MHz	166.66 MHz
11111	12.5x	2x		600 (1200)	833 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)	1079 (2158)	1300 (2600)		
11100	13.5x	2x		675 (1350)	900 (1800)	1013 (2026)	1121 (2242)	1350 (2700)		
11001	14x	2x		700 (1400)	933 (1866)	1050 (2100)	1162 (2324)	1400 (2800)		
00011	15x	2x		750 (1500)	1000 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1066 (2132)	1200 (2400)	1328 (2656)			
00001	17x	2x		850 (1900)	1132 (2264)	1275 (2550)	1411 (2822)			
00101	18x	2x	600 (1200)	900 (1800)	1200 (2400)	1350 (2700)				
00111	20x	2x	667 (1334)	1000 (2000)	1332 (2664)					
01001	21x	2x	700 (1400)	1050 (2100)	1399 (2797)					
01101	24x	2x	800 (1600)	1200 (2400)						
11101	28x	2x	933 (1866)	1400 (2800)						
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							
11110	PLL off		PLL off, no core clocking occurs							

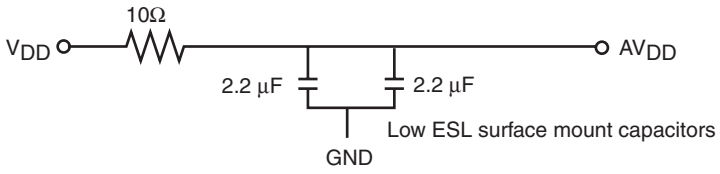
Notes:
1. PLL_CFG[0:4] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies that are not useful, not supported, or not tested for by the PC7455; see Section "Clock AC Specifications" on page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup tIVKH and hold time tIXKH (see Table 9-3 on page 27). The result will be that the processor bus frequency will be one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7447A regardless of the SYSCLK input.

12.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PC7447A to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 KHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 12-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 HITCE footprint.

Figure 12-1. PLL Power Supply Filter Circuit



12.3 Decoupling Recommendations

Due to the PC7447A dynamic power management feature, large address and data buses, and high operating frequencies, the PC7447A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7447A system, and the PC7447A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every 1-2 V_{DD} pins, and a similar or lesser amount for the OV_{DD} pins, placed as close as possible to the power pins of the PC7447A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale™ microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are: 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

12.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD}, and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the PC7447A.

For backward compatibility with the PC7447 to the PC7447A, the new power and ground signals (formerly NC, see Table 8-1 on page 21) may be left unconnected. There is no performance degradation associated with leaving these pins unconnected. However, future devices may require these additional power and ground signals to be connected to achieve maximum performance, and it is recommended that new designs include the additional connections to facilitate future upgrades. See also section "Pinout Listings" on page 21 for additional information.

12.5 Output Buffer DC Impedance

The PC7447A processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 12-2 on page 42 shows the driver impedance measurement.

The output impedance is the average of two components–the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 12-2. Driver Impedance Measurement

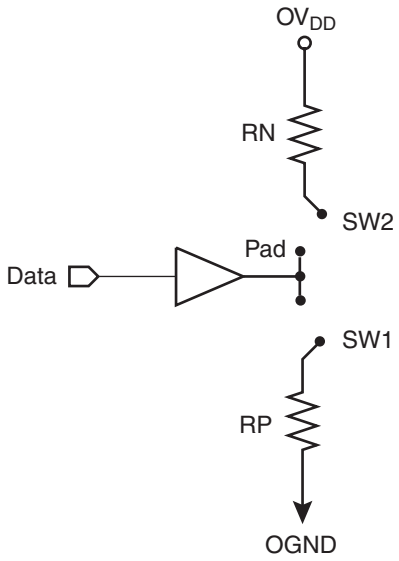


Table 12-2 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 12-2. Impedance Characteristics with V_{DD} = 1.5V, OV_{DD} = 1.8V ±5%, T_j = 5° - 85°C

Impedance		Processor bus	L3 Bus	Unit
Z_0	Typical	33 – 42	34 – 42	Ω
	Maximum	31 – 51	32 – 44	Ω

12.6 Pull-up/Pull-down Resistor Requirements

The PC7447A requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7447A or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the PC7447A, 360 BGA, the pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.
In addition, the PC7447A has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

If pull-down resistors are used to configure BVSEL, the resistors should be less than 250Ω (see Table 8-1 on page 21). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7447A must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7447A or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the PC7447A input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{CI}$, $\overline{WT}$, and $\overline{GBL}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, and may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the PC7447A is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors. The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

12.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 12-3 on page 45 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω. isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 12-3 on page 45, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

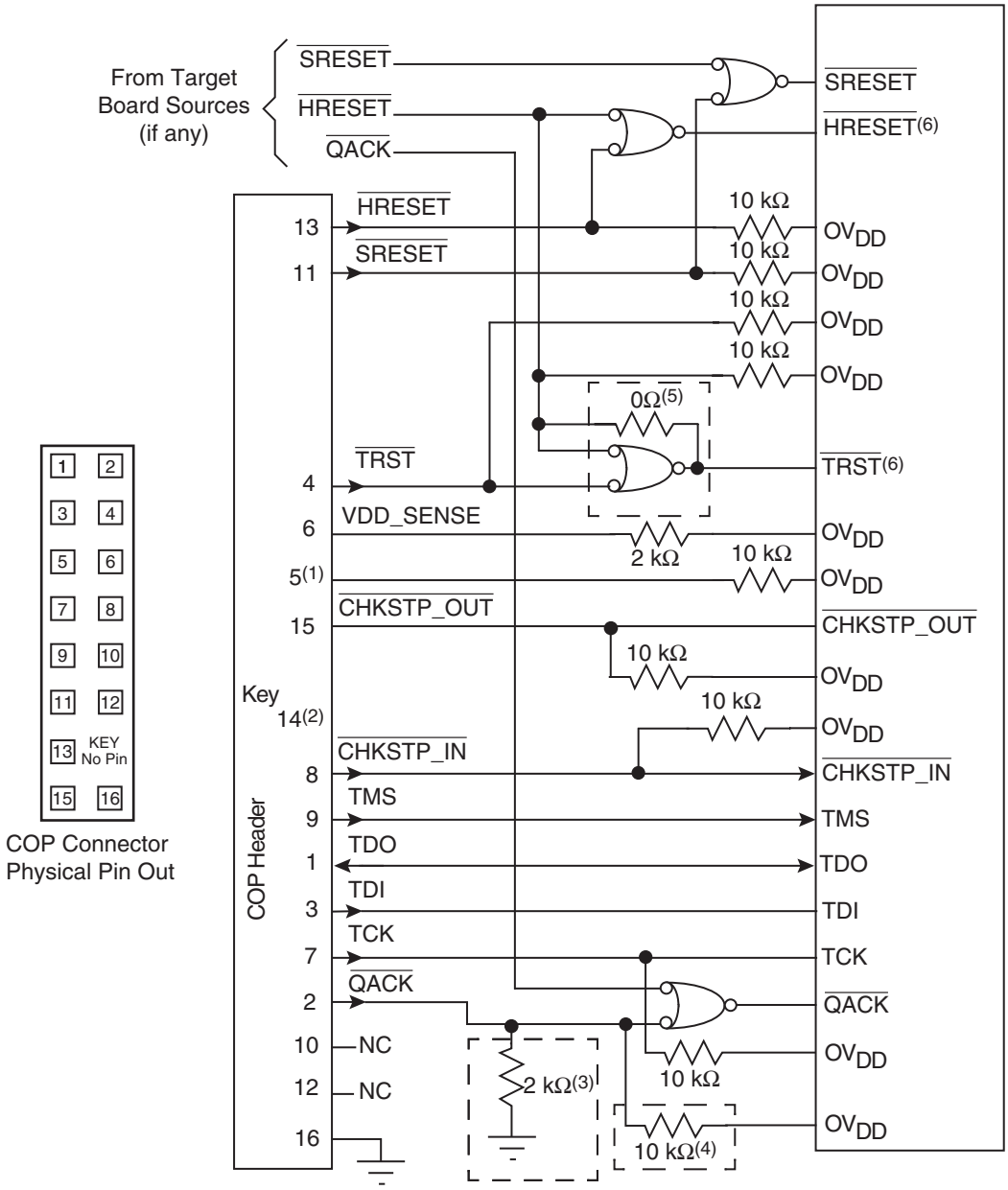
The COP header shown in Figure 12-3 on page 45 adds many benefits: breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface, and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025 inch square-post, 0.100 inch centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 12-3 on page 45; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 12-3 on page 45 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 12-3 on page 45 is usually connected to the PCI bridge chip in a system and is an input to the PC7447A informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the PC7447A must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the PCI bridge.

Figure 12-3. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7447A. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively de-assert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

13. Ordering Information

xx 7447 y xxx nnnn L x

Product Code[1]	Part Identifier	Temperature Range Tj[1]	Package[1]	Max Internal Processor Speed[1]	Application Modifier[1]	Revision Level[1]
PC(X)[2]	7447A	M: -55˚C, +125˚C V: -40˚C, +110˚C	GH: HiTCE GHY: HiTCE RoHS compliant LH: LGA	1167 MHz (N-Spec) 1000 MHz (N-Spec)	N: 1.1V ± 50 mV	B

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

14. Definitions

14.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

15. Document Revision History

Table 15-1 provides a revision history for this hardware specification.

Table 15-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	01/07	Name change from Atmel to e2v
D	07/06	Page 35: b parameter modification; remove preliminary.
C	12/05	Add RoHS package and LGA package.
B	07/05	Changed die size.
		Table 9-2 on page 25: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Added t_{KHTSV}, t_{KHARV}, t_{KHTSX}, and t_{KHARX} to Table 9-3 on page 27; these were previously grouped with t_{KHOV} and t_{KHOX}. Note: Documentation change only; the values for the output valid and output hold AC timing specifications remain unchanged for $\overline{TS}$, $\overline{ARTRY}$, and $\overline{SHD}$[0:1].
A	04/04	Initial revision.

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