

OptiMOS[®]-P Small-Signal-Transistor Feature

- P-Channel
- Enhancement mode
- Logic Level
- 150°C operating temperature
- Avalanche rated
- dv/dt rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen free according to IEC61249-2-21

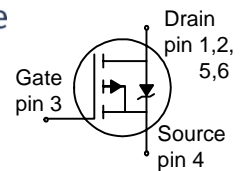
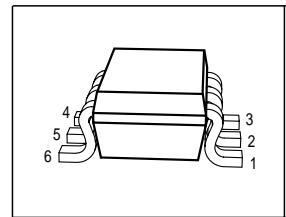


Halogen-Free

Product Summary

V_{DS}	-30	V
$R_{DS(on)}$	43	m Ω
I_D	-5.5	A

PG-TSOP-6-1



Type	Package	Tape and reel	Marking
BSL307SP	PG-TSOP-6-1	H6327: 3000pcs/r.	sPC

Maximum Ratings, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D		A
$T_A=25^\circ\text{C}$		-5.5	
$T_A=70^\circ\text{C}$		-4.4	
Pulsed drain current	$I_D \text{ puls}$	-22	
$T_A=25^\circ\text{C}$			
Avalanche energy, single pulse	E_{AS}	44	mJ
$I_D=-5.5\text{ A}$, $V_{DD}=-25\text{V}$, $R_{GS}=25\Omega$			
Reverse diode dv/dt	dv/dt	-6	kV/ μs
$I_S=-5.5\text{A}$, $V_{DS}=24\text{V}$, $dI/dt=200\text{A}/\mu\text{s}$, $T_{jmax}=150^\circ\text{C}$			
Gate source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	2	W
$T_A=25^\circ\text{C}$			
Operating and storage temperature	T_j, T_{stg}	-55... +150	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1		55/150/56	
ESD Class JEDEC22-A114-HBM		Class 1a	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - soldering point	R_{thJS}	-	-	50	K/W
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	230	
@ 6 cm ² cooling area ¹⁾		-	-	62.5	

Electrical Characteristics, at $T_j = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0, I_D=-250\mu A$	$V_{(BR)DSS}$	-30	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=-40\mu A$	$V_{GS(th)}$	-1	-1.5	-2	
Zero gate voltage drain current $V_{DS}=-30V, V_{GS}=0, T_j=25\text{ °C}$ $V_{DS}=-30V, V_{GS}=0, T_j=150\text{ °C}$	I_{DSS}	-	-0.1	-1	μA
		-	-10	-100	
Gate-source leakage current $V_{GS}=-20V, V_{DS}=0$	I_{GSS}	-	-10	-100	nA
Drain-source on-state resistance $V_{GS}=-4.5V, I_D=-4.2A$	$R_{DS(on)}$	-	52	74	m Ω
Drain-source on-state resistance $V_{GS}=-10V, I_D=-5.5A$	$R_{DS(on)}$	-	31	43	

¹Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air; $t \leq 5$ sec.

Electrical Characteristics, at $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic Characteristics

Transconductance	g_{fs}	$ V_{DS} \geq 2 * I_D * R_{DS(on)max}$ $I_D = -4.4\text{A}$	4.7	9.4	-	S
Input capacitance	C_{iss}	$V_{GS} = 0, V_{DS} = -25\text{V},$ $f = 1\text{MHz}$	-	805	-	pF
Output capacitance	C_{oss}		-	234	-	
Reverse transfer capacitance	C_{rss}		-	195	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{V}, V_{GS} = -10\text{V},$ $I_D = -1\text{A}, R_G = 6\Omega$	-	7.3	11	ns
Rise time	t_r		-	8.4	12.6	
Turn-off delay time	$t_{d(off)}$		-	36.4	55	
Fall time	t_f		-	29	44	

Gate Charge Characteristics

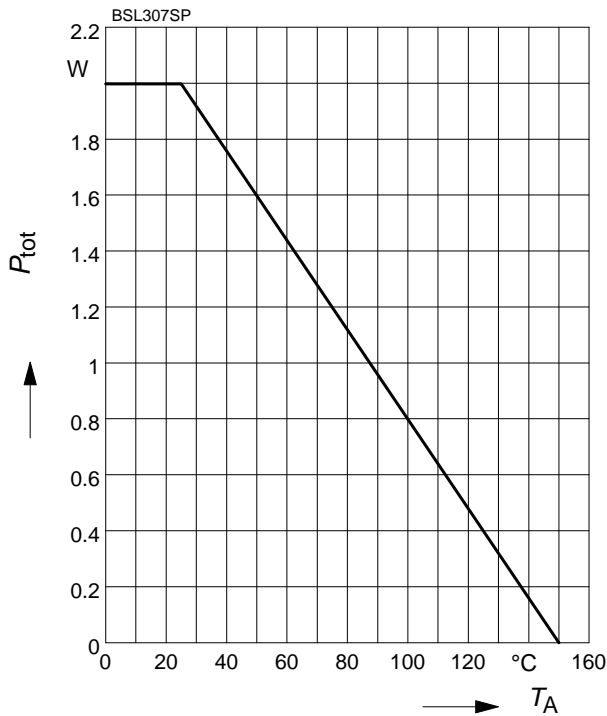
Gate to source charge	Q_{gs}	$V_{DD} = -24\text{V}, I_D = -5.5\text{A}$	-	-2	-2.5	nC
Gate to drain charge	Q_{gd}		-	-8.2	-12.3	
Gate charge total	Q_g	$V_{DD} = -24\text{V}, I_D = -5.5\text{A},$ $V_{GS} = 0 \text{ to } -10\text{V}$	-	-23.4	-29	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = -24\text{V}, I_D = -5.5\text{A}$	-	-2.8	-	V

Reverse Diode

Inverse diode continuous forward current	I_S	$T_A = 25\text{ }^\circ\text{C}$	-	-	-5.5	A
Inverse diode direct current, pulsed	I_{SM}		-	-	-22	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0, I_F = I_D $	-	-0.88	-1.3	V
Reverse recovery time	t_{rr}	$V_R = -15\text{V}, I_F = I_D ,$ $di_F/dt = 100\text{A}/\mu\text{s}$	-	16.6	21	ns
Reverse recovery charge	Q_{rr}		-	6.2	7.8	

1 Power dissipation

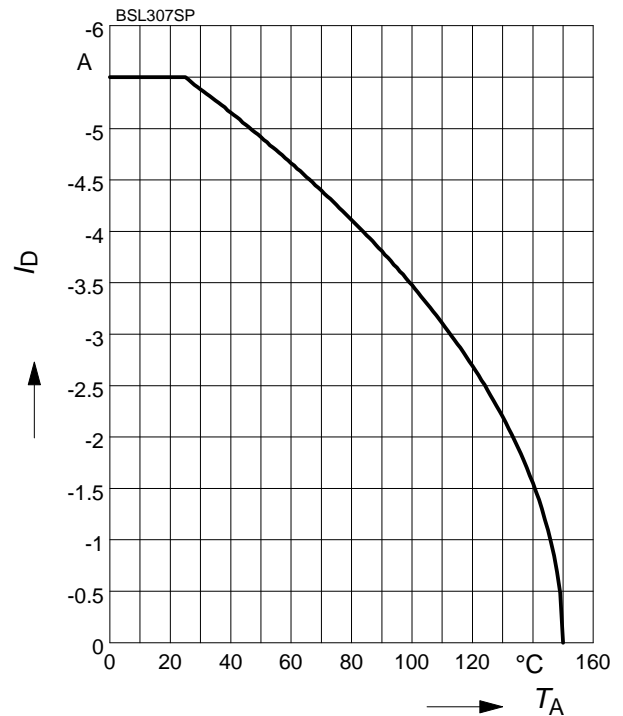
$$P_{tot} = f(T_A)$$



2 Drain current

$$I_D = f(T_A)$$

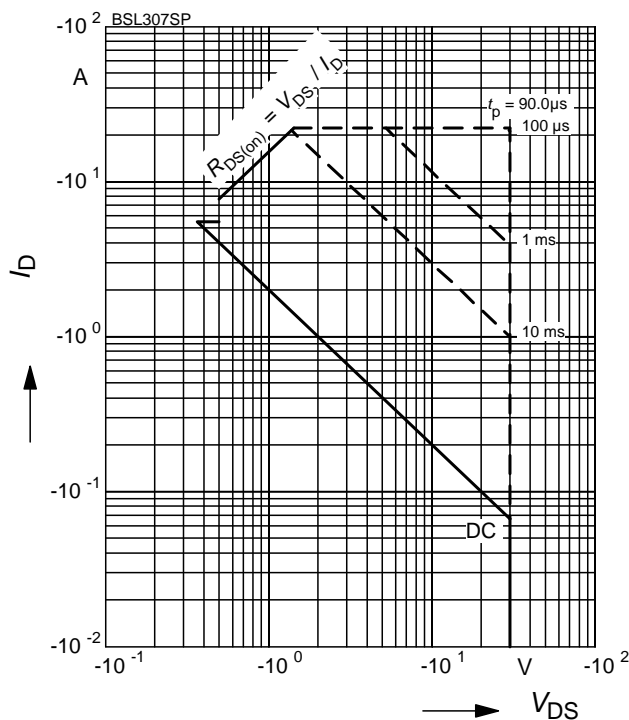
parameter: $|V_{GS}| \geq 10 \text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

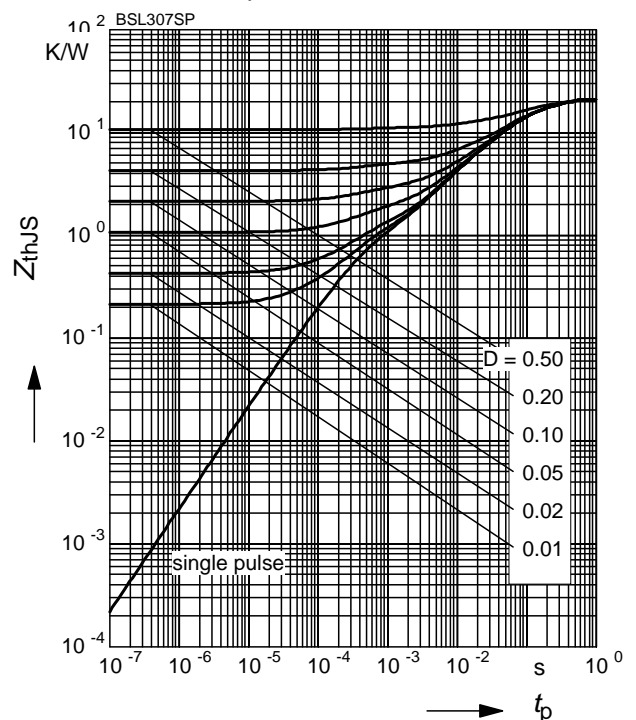
parameter: $D = 0, T_A = 25 \text{ °C}$



4 Transient thermal impedance

$$Z_{thJS} = f(t_p)$$

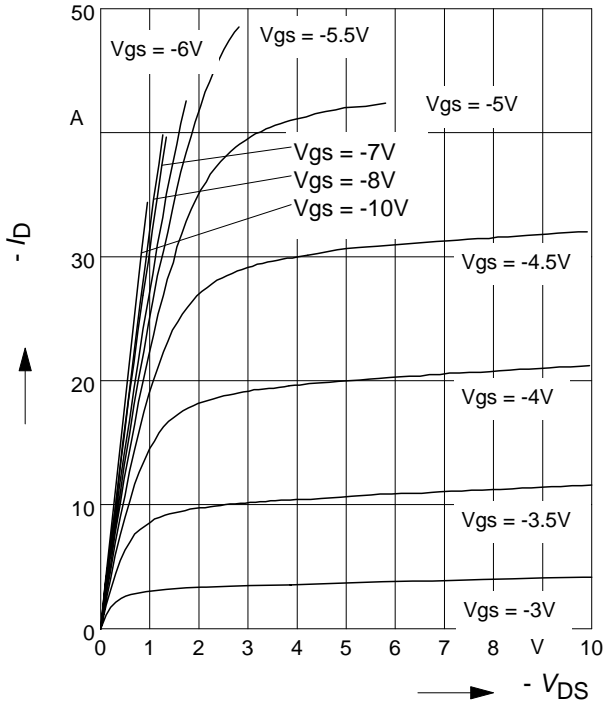
parameter: $D = t_p/T$



5 Typ. output characteristic

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

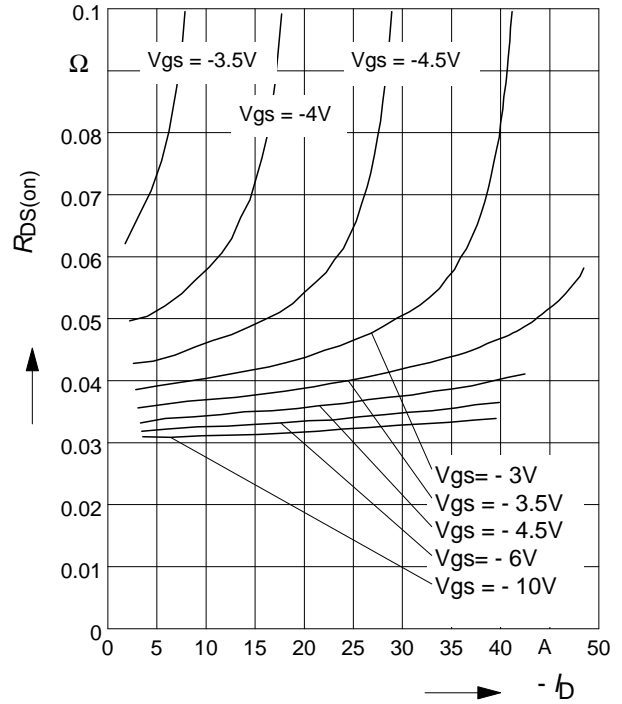
parameter: $t_p = 80 \mu\text{s}$



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$

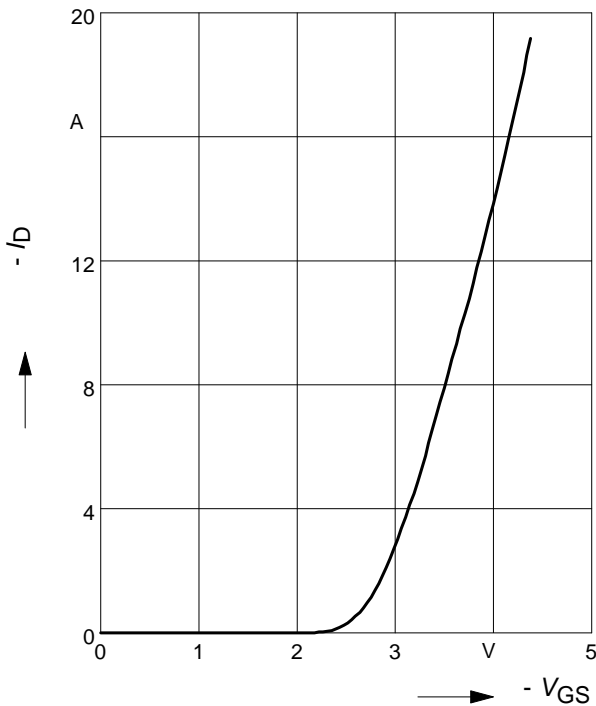
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| \geq 2 \times |I_D| \times R_{DS(on)max}$

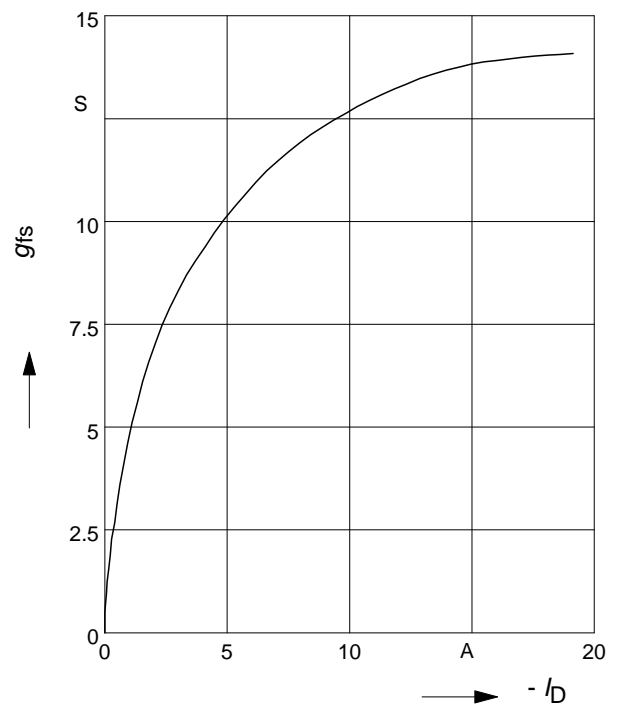
parameter: $t_p = 80 \mu\text{s}$



8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

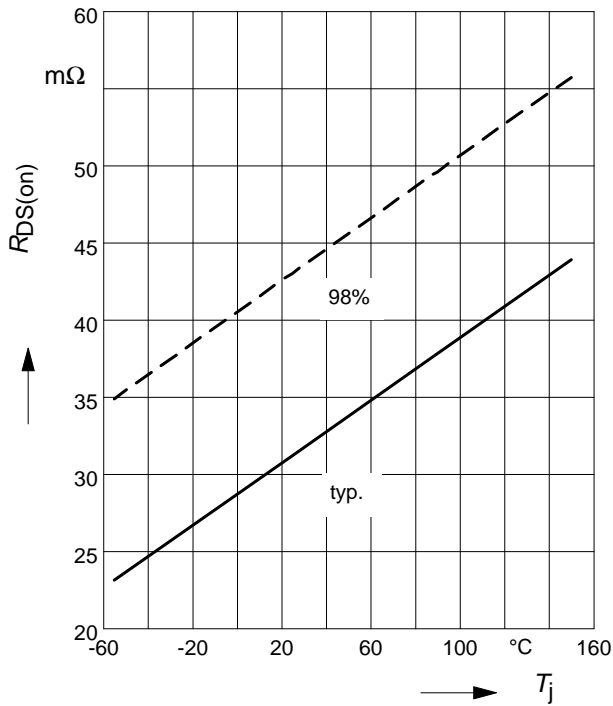
parameter: $t_p = 80 \mu\text{s}$



9 Drain-source on-resistance

$$R_{DS(on)} = f(T_j)$$

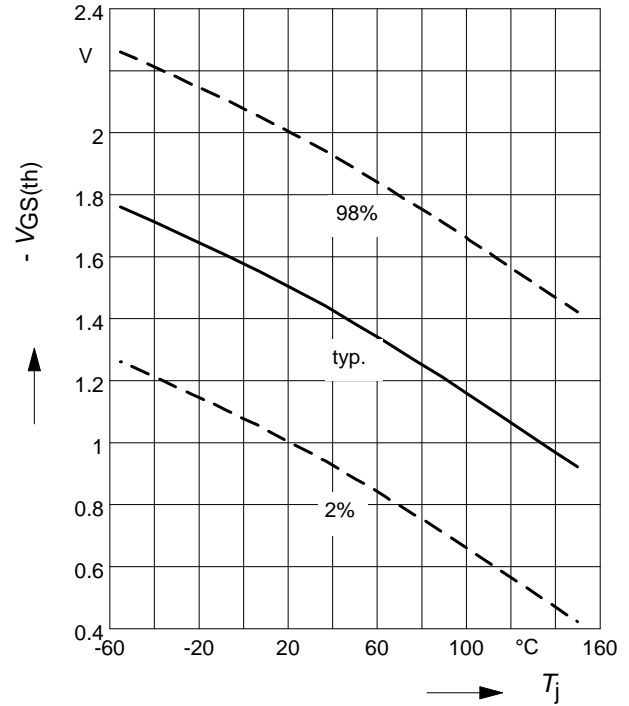
parameter: $I_D = -5.5 \text{ A}$, $V_{GS} = -10 \text{ V}$



10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

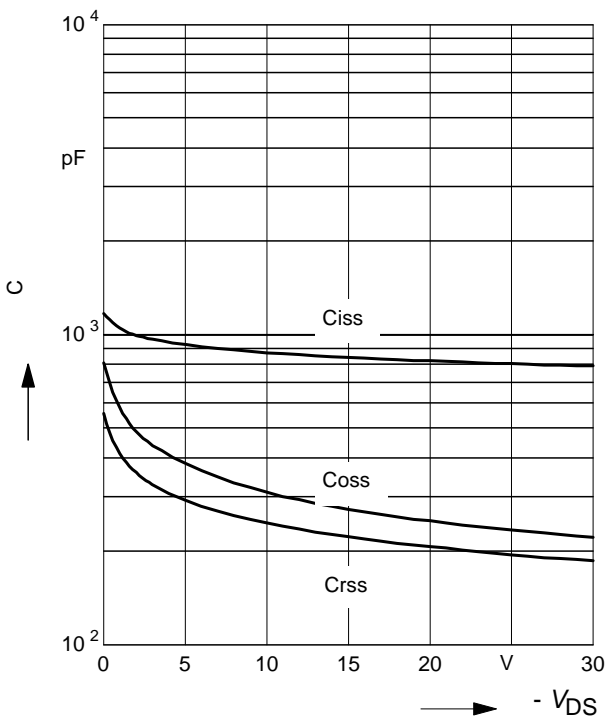
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$$C = f(V_{DS})$$

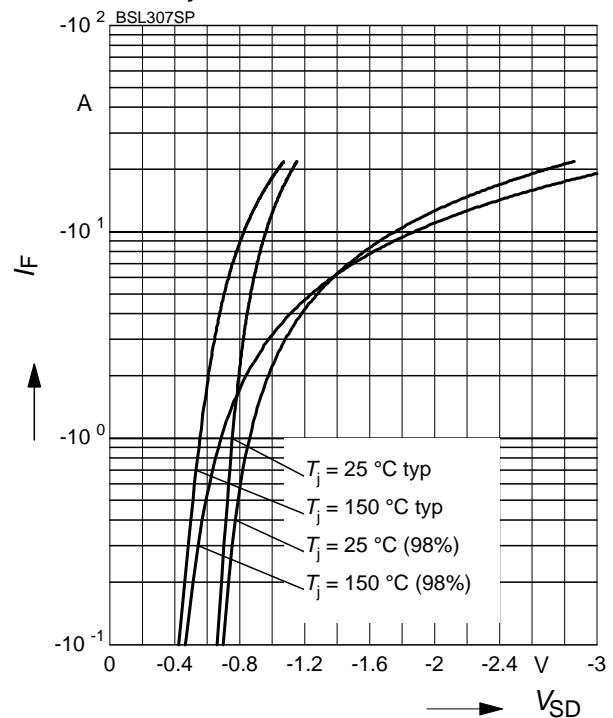
parameter: $V_{GS}=0$, $f=1 \text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

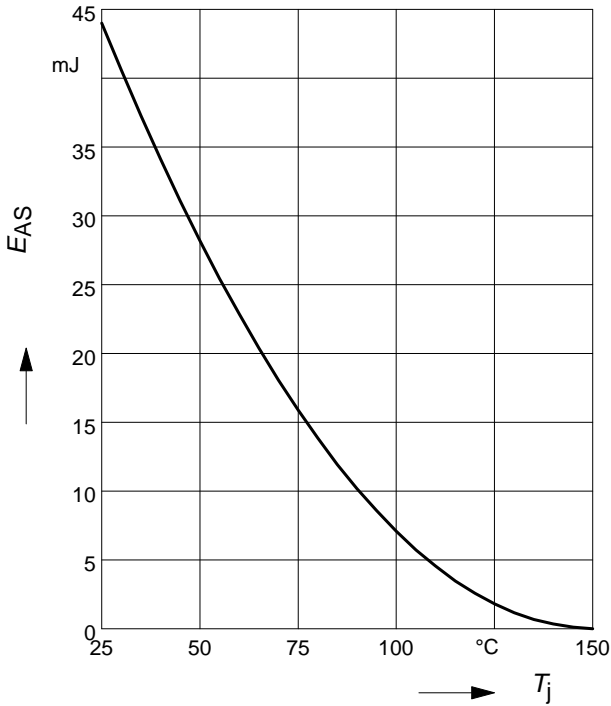
parameter: T_j , $t_p = 80 \mu\text{s}$



13 Typ. avalanche energy

$E_{AS} = f(T_j)$, par.: $I_D = -5.5 \text{ A}$

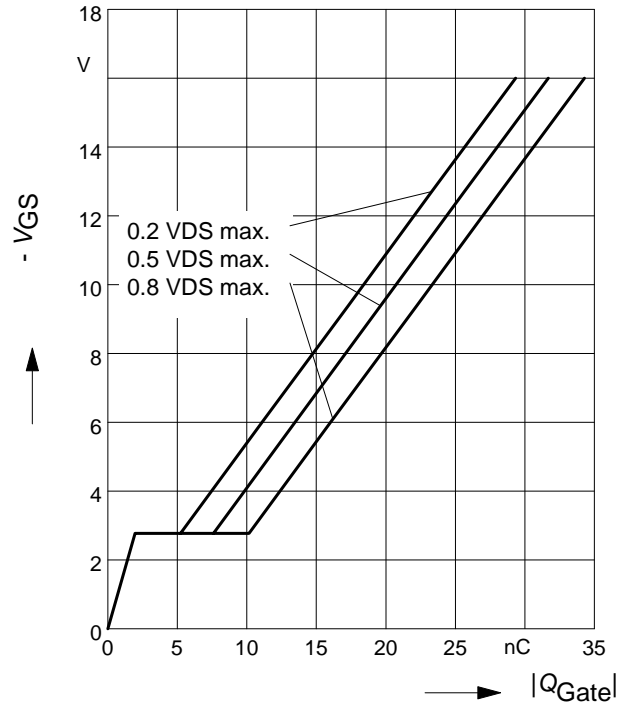
$V_{DD} = -25 \text{ V}$, $R_{GS} = 25 \Omega$



14 Typ. gate charge

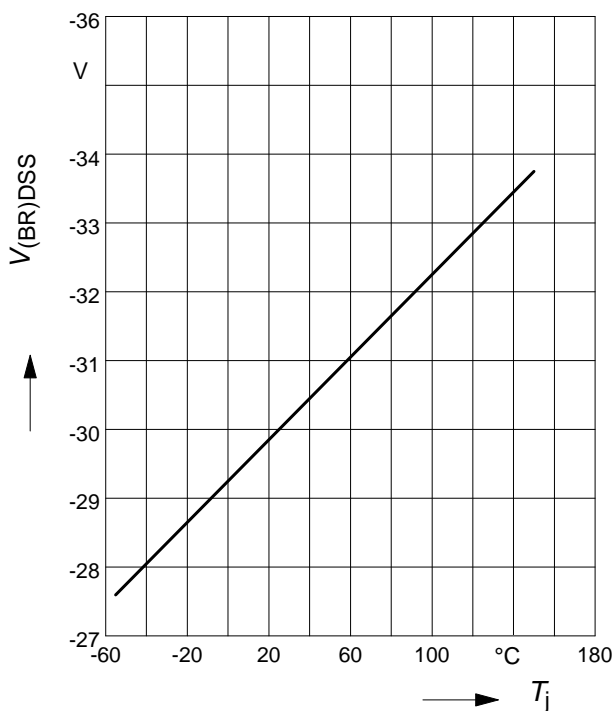
$|V_{GS}| = f(Q_{Gate})$

parameter: $I_D = -5.5 \text{ A}$ pulsed



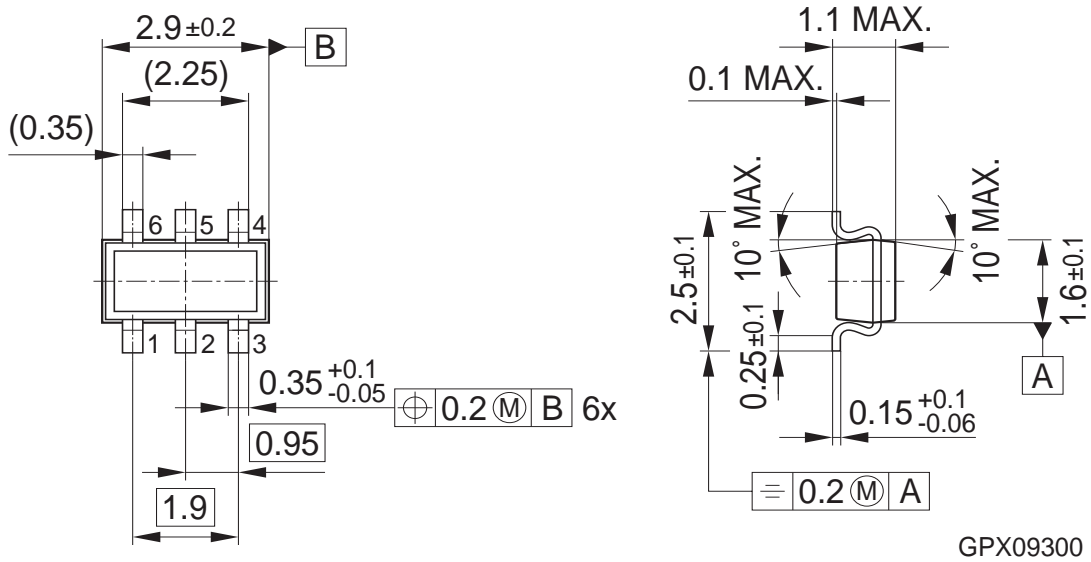
15 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$

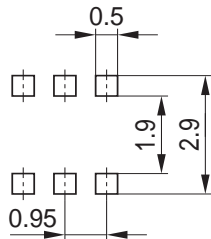


Package Outline:

TSOP6



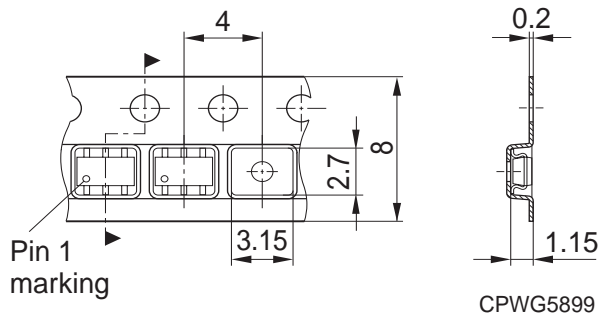
Footprint:



Remark: Wave soldering possible dep. on customers process conditions

HLG09283

Packaging:



Dimensions in mm

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