ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC

User Guide

UG850 (v1.5) September 4, 2015

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/24/2012	1.0	Initial Xilinx release.
10/08/2012	1.1	The board photo in Figure 1-2 was updated. Table 1-2, Switch SW16 Configuration Option Settings was added. The part number in Quad-SPI Flash Memory, page 21 changed to N25Q128A13ESF40F. In Table 1-6, the J35 shunt controls OTG and Device mode. The frequency jitter in System Clock, page 29 changed from 20 ppm to 50 ppm. The action description under Program_B Pushbutton, page 50 changed. The 34 differential user-defined signals are defined as 34 LA pairs, LA00–LA33, in LPC Connectors J3 and J4, page 52. In the same section, 34 differential user-defined pairs changed to 68 single-ended or 34 differential user-defined signals. Appendix F, Regulatory and Compliance Information now includes a link to the Declaration of Conformity and markings for waste electrical and electronic equipment (WEEE), restriction of hazardous substances (RoHS), and CE compliance.

Date	Version	Revision
04/04/2013	1.2	Chapter 1, ZC702 Evaluation Board Features: Marvell 88E1111 was changed to Marvell 88E1116R throughout the document. The bullet just before Block Diagram, page 10 changed from PL JTAG header to PS JTAG header. In Table 1-1, page 12, callout 3, PC28F00AG18FE StrataFlash memory changed to 128 Mb, N25Q128A11ESF40G. In callout 9, Marvell M88E1116R-BAB1C000 changed to 88E1116RA0-NNC1C000. Callout 30 for J59 and 31 for J60 were added. The Zynq-7000 XC7Z020 AP SoC, page 13 description for callout 1 changed. Callout 29 added a link to Table 1-2. Table 1-2 was removed because it is a duplicate of Table 1-10. Above Table 1-2, page 16, "configuration option" was changed to "*JTAG* configuration option." In Table 1-2, the *PLL Used mode* row was removed and the default setting changed. Section Encryption Key Backup Circuit, page 17 was added. In I/O Voltage Rails, page 18, "There are four I/O banks available on the XC7Z020 AP SoC" was changed to "There are four *PL* I/O banks available on the XC7Z020 AP SoC." A note about DDR3 memory was added after Table 1-4, page 18. In Quad-SPI Flash Memory, page 21 and Figure 1-6, *N25Q128A13ESF40F* (Micron/Numonyx) changed to N25Q128A11ESF40G. In Quad-SPI Flash Memory, page 21, "The configuration section of UG585..." was changed to add "The configuration *and QSPI* section of UG585..." JTAG information in Figure 1-10 and Table 1-10 was updated. In Figure 1-10 pin numbers 5 and 6 are swapped and in U76, IN2 and IN1 switched places. In Table 1-10, *SW10* became SW10[1:2] in the table column heading and the default setting was added. In Processing System Clock Source, page 30, frequency jitter changed from 20 ppm to 50 ppm. In I2C Bus, page 37, NXP semiconductor changed to TI. Figure 1-15 is updated. R249 was added to Figure 1-17. In Table 1-22, reference designator DS12 changed to DS14. U3 level shifter was changed to TXS0104E in Figure 1-19 and Table 1-21. The User I/O, page 43 section was updated. Figure 1-21 added two LEDs. Table 1-23 added Net Name PS_LED1 and PS_MIO8_LED0 and removed pin info. Section User PS Switches, page 48 was added. The Figure 1-26 title changed. A paragraph about design criteria was added to Power Management, page 56. A paragraph about the TI Fusion Digital Power graphical user interface precedes Table 1-30. Voltages were added to the description of U19 in Table 1-30. The TI link on page 59 was updated. Appendix A, Default Switch and Jumper Settings: In Table A-1, SW16 position 4 changed from right to left. Appendix C, Master Constraints File Listing: A reminder was added to use the latest UCF listing. Minor changes were made to the list, and power and ground pin constraints were removed. Appendix D, Board Specifications: This appendix was added to the book. Appendix F, Regulatory and Compliance Information: A link to the ZC702 board master answer record was added.
06/04/2014	1.3	Table 1-6 USB Jumper Settings was updated to highlight default shunt positions. GND changed to GA0 = 0 = GND in Table 1-28 and Table 1-29. The Appendix C Master UCF Listing was replaced with the Xilinx Design Constraints (XDC) file listing. The link in Declaration of Conformity was updated.
04/30/2015	1.4	Description added to FMC Connector JTAG Bypass. Modifications to Table 1-12, Table 1-16, Table 1-17, Table 1-23, Table 1-25, Table 1-27, Table 1-28, and Table 1-29. Note added to Table 1-20. Revised the PMBus Controller–Aux address for U34 from 53 to 54 in Table 1-30. Annotations added to ZC702 Board Constraints File Listing. Added Figure Figure A-1, page 66 to identify jumper locations referenced in Table A-2, page 64.

Date	Version	Revision
09/04/2015	1.5	Added missing *symbol* font to fix improperly rendered text (kW, mF) to the correct units (kΩ, µF) in Table 1-6, rows 3 and 4. Removed base ambiguity from PMBUS address numbers 52, 53, and 54 by updating them according to context to 52 *decimal*, 53 *decimal*, and 54 *decimal* or to binary 0b0110100, 0b0110101 and 0b0110110 in Table 1-19, in Figure 1-29, in Table 1-30, in the first paragraph under Monitoring Voltage and Current, page 59, in Table 1-31, in Table 1-32, and in Table 1-33.

Table of Contents

ZC702 Evaluation Board Features

Overview

The ZC702 evaluation board for the XC7Z020 All Programmable SoC (AP SoC) provides a hardware environment for developing and evaluating designs targeting the Zynq® XC7Z020-1CLG484C device. The ZC702 board provides features common to many embedded processing systems, including DDR3 component memory, a tri-mode Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to either of two low pin count (LPC) FMC connectors.

ZC702 Board Features

The ZC702 board features are listed in here. Detailed information for each feature is provided in Feature Descriptions starting on page 13.

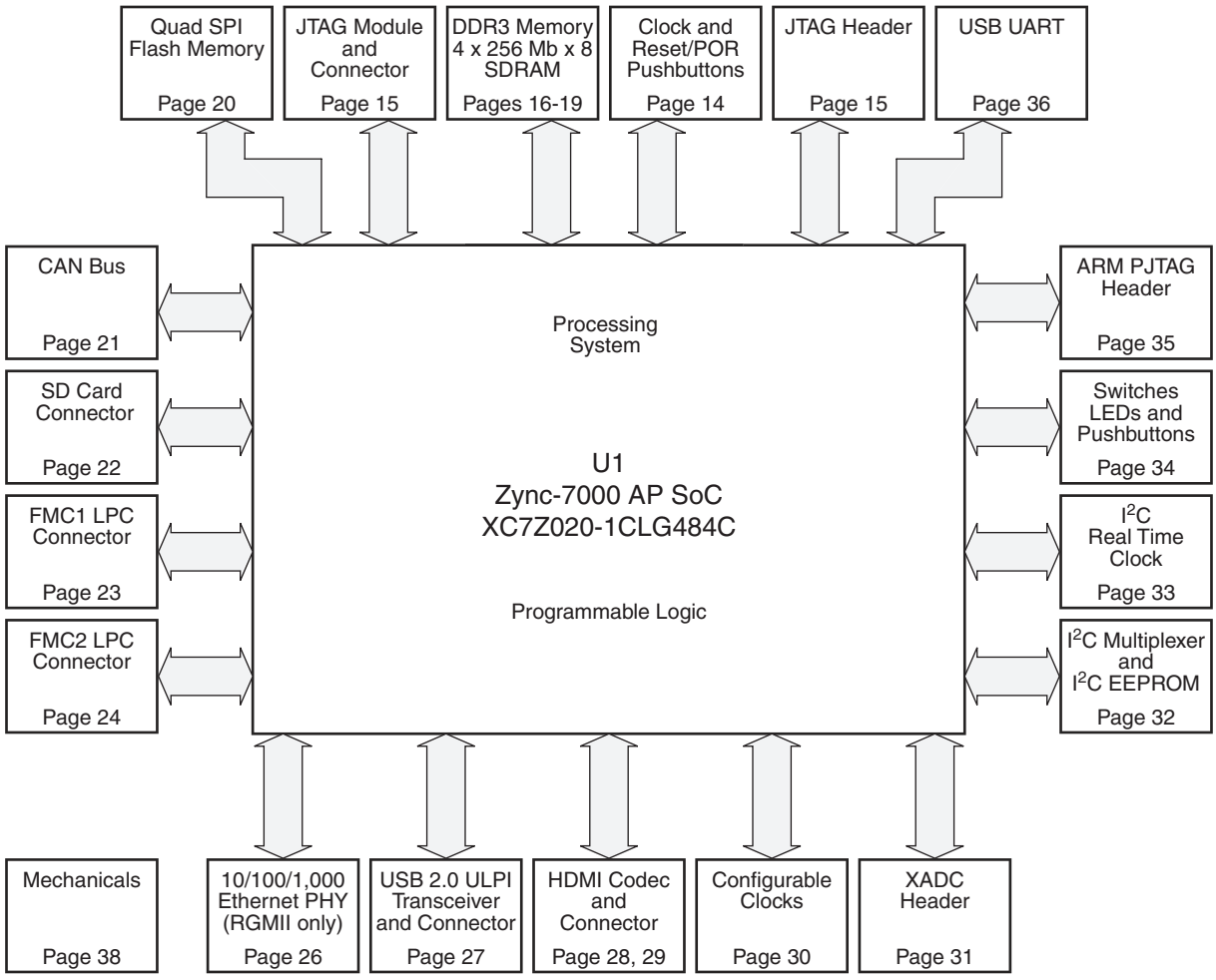
- Zynq XC7Z020-1CLG484C device
- 1 GB DDR3 component memory (four 256 Mb x 8 devices)
- 128 Mb Quad SPI flash memory
- USB 2.0 ULPI (UTMI+ low pin interface) transceiver
- Secure Digital (SD) connector
- USB JTAG interface using a Digilent module
- Clock sources:
  - Fixed 200 MHz LVDS oscillator (differential)
  - I2C programmable LVDS oscillator (differential)
  - Fixed 33.33 MHz LVCMOS oscillator (single-ended)
- Ethernet PHY RGMII interface with RJ-45 connector
- USB-to-UART bridge
- HDMI codec
- I2C bus

- I2C bus multiplexed to:
  - Si570 user clock
  - ADV7511 HDMI codec
  - M24C08 EEPROM (1 kB)
  - 1-To-16 TCA6416APWR port expander
  - RTC-8564JE real time clock
  - FMC1 LPC connector
  - FMC2 LPC connector
  - PMBUS data/clock
- Status LEDs:
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O:
  - Two programmable logic (PL) user pushbuttons
  - PL user DIP switch (2-pole)
  - Eight PL user LEDs
  - Two processing system (PS) pushbuttons shared with PS 2-pole DIP switch
  - Two PS user LEDs
  - Dual row Pmod GPIO header
  - Single row Pmod GPIO header
- AP SoC PS Reset Pushbuttons:
  - SRST_B PS reset button
  - POR_B PS reset button
- Two VITA 57.1 FMC LPC connectors
- Power on/off slide switch
- Power management with PMBus voltage and current monitoring via TI power controllers
- Dual 12-bit 1 MSPS XADC analog-to-digital front end
- Configuration options:

- Quad SPI flash memory
- USB JTAG configuration port (Digilent module)
- Platform cable header JTAG configuration port
- 20-pin PL PJTAG header
- 20-pin PS JTAG header

Block Diagram

The ZC702 board block diagram is shown in Figure 1-1.



Note: Page numbers reference the page number of schematic 0381449.

Figure 1-1: **ZC702 Board Block Diagram**

Board Layout

Figure 1-2 shows the ZC702 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 with a link to detailed information provided under Feature Descriptions starting on page 13. Note that the image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

CAUTION! *The ZC702 board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

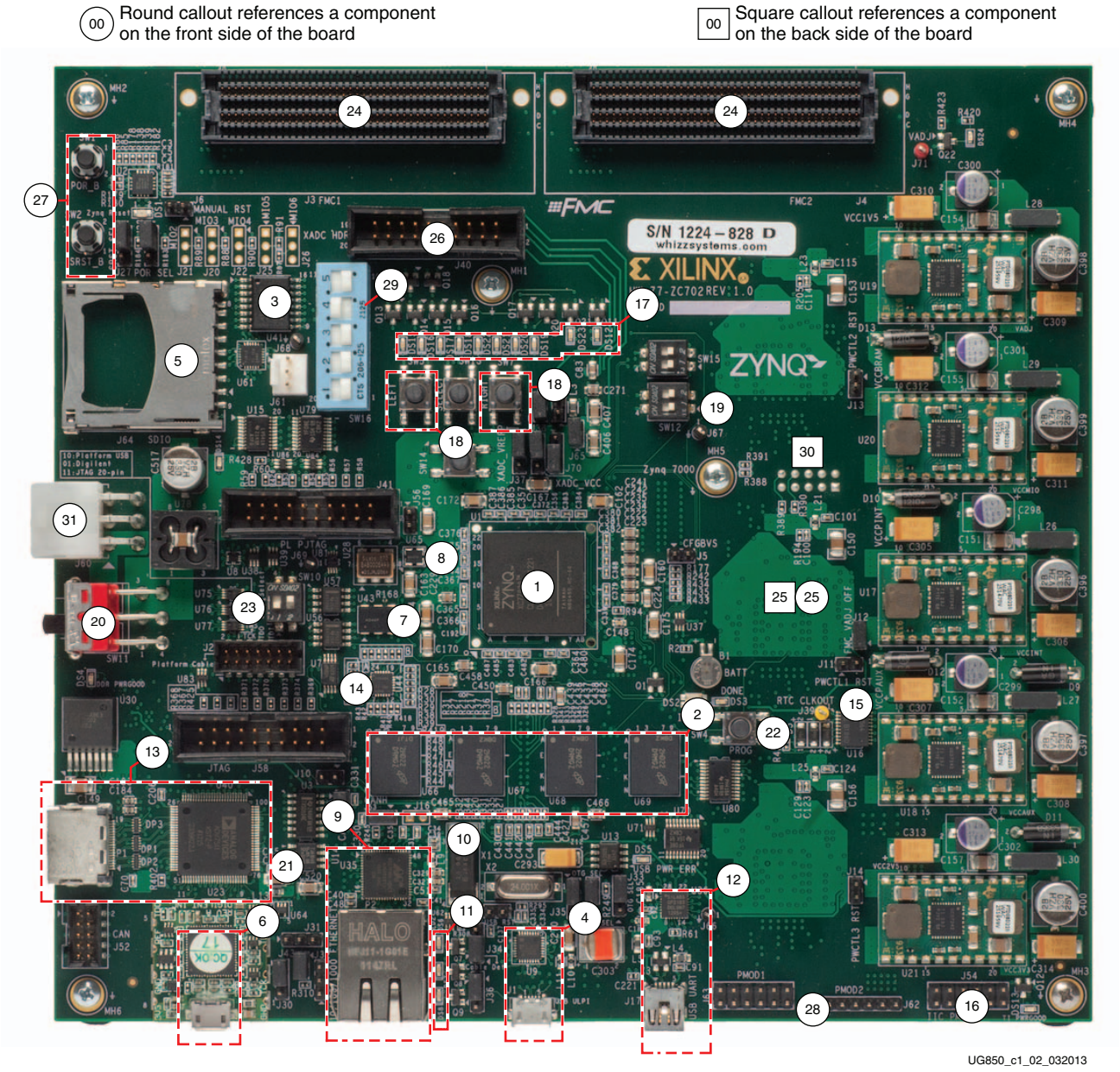


Figure 1-2: **ZC702 Board Component Locations**

Table 1-1: **ZC702 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic[1] 0381449 Page Number
1	U1	Zynq-7000 XC7Z020 AP SoC	Xilinx part number: XC7Z020-1CLG484C	
2	U66–U69	DDR3 Component Memory, 1 GB	4 each 256Mb X 8 SDRAM Micron Technology Inc, MT41J256M8DA-107	16–19
3	U41	Quad-SPI Flash Memory, 128 Mb	Micron N25Q128A11ESF40G	20
4	U9, J1	USB 2.0 ULPI Transceiver, USB Mini-B connector	SMSC USB3320-EZK High-Speed USB transceiver	27
5	J64	SD Card Interface connector	Molex 67840-8001 SDIO Memory card connector	22
6	U23	Programmable Logic JTAG Programming Options with integrated Micro-B connector	Digilent USB JTAG Module	15
7	U43	System Clock, 200 MHz, 2.5V LVDS oscillator	SiTime SIT9102-243N25E200.0000	30
8	U28, U65	Programmable User Clock and Processing System Clock Source	Silicon Labs SI570BAB0000544DG, default 156.250MHz, PS fixed 33 MHz clock	30
9	U35, P2	10/100/1000 MHz Tri-Speed Ethernet PHY, RJ45 w/magnetics	Marvell 88E1116RA0-NNC1C000, Halo HFJ11-1G01ERL	25–26
10	X1	Ethernet PHY Clock Source, 25.000 MHz	Epson MA-506-25.000m-CO:ROHS	25
11	DS6–DS8	Ethernet PHY User LEDs	Ethernet PHY User LEDs, GREEN	25
12	U36, J17	USB-to-UART Bridge, USB Mini-B connector	Silicon Labs CP2103GM, Molex 54819-0589	36
13	U40, P1	HDMI Video Output	Analog Devices ADV7511KSTZ-P HDMI transmitter, Molex 500254-1927 HDMI receptacle	28–29
14	U44	I2C Bus	TI PCA9548ARGER	32
15	U16	Real-Time Clock	Epson RTC-8564JE:3:ROHS	33
16	J54	I/O Expansion Header driven from I2C Expander U80	2-row pin header	33
17	DS15–DS22	User LEDs	GPIO LEDs, GREEN 0603	34
18	SW5, SW7	User Pushbuttons SW5 = Left, SW7 = Right	E-Switch TL3301EP100QG	34
19	SW12	GPIO DIP Switch	2-pole C&K SDA02H1SBD	34
20	SW11	Power On/Off Slide Switch	C and K 1201M2S3AQE2	47
21	U14	High Speed CAN Transceiver	NXP TJA1040T/VM	21
22	SW4	Program_B Pushbutton	E-Switch TL3301EP100QG	34
23	SW10, J2	Programmable Logic JTAG Select Switch, JTAG Cable Connector	2-pole C and K SDA02H1SBD MOLEX 87832-1420	15
24	J3, J4	FPGA Mezzanine (FMC) Card Interface	Samtec ASP_134486_01	23, 24
25	U32, U33, U34	Power Management (bottom and top of board)	TI UCD9248PFC in conjunction with various regulators	39–47
26	J40	XADC Analog-to-Digital Converter	2X10 0.-inch male header	31

Table 1-1: **ZC702 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic[1] 0381449 Page Number
27	SW1, SW2	PS Power-On and System Reset Pushbuttons	Panasonic EVQ-11L07K 14	35, 36
28	J62, J63	User PMOD GPIO Headers	J63 2 x 6 0.1 inch J63 1 x 6 0.1 inch male headers	34, 35
29	SW16	5-pole SPDT MIO DIP switch	CTS 206-125. See Table 1-2 for switch settings.	14
30	J59	2x5 shrouded PMBus connector (bottom of board)	ASSMAN HW10G-0202	47
31	J60	12V power input 2x6 connector	MOLEX 39-30-1060	47

Notes:

1. The ZC702 board schematics are available for download. See ZC702 Evaluation Kit.
2. Jumper locations are shown in Figure A-1, page 66.

Feature Descriptions

Detailed information for each feature shown in Figure 1-2 and listed in Table 1-1 is provided in this section.

Zynq-7000 XC7Z020 AP SoC

[Figure 1-2, callout 1]

The ZC702 board is populated with the Zynq-7000 XC7Z020-1CLG484C AP SoC. The XC7Z020 AP SoC consists of an SoC-style integrated processing system (PS) and programmable logic (PL) on a single die.

The high-level block diagram is shown in Figure 1-3.

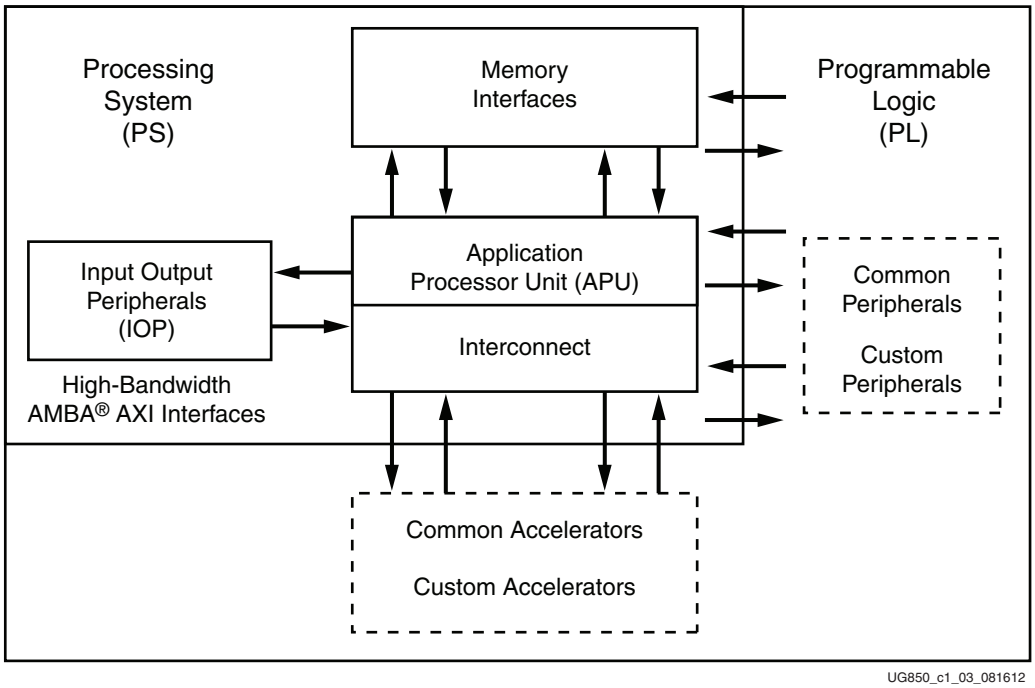


Figure 1-3: **High-Level Block Diagram**

The PS integrates two ARM® Cortex™-A9 MPCore™ application processors, AMBA® interconnect, internal memories, external memory interfaces, and peripherals including USB, Ethernet, SPI, SD/SDIO, I2C, CAN, UART, and GPIO. The PS runs independently of the PL and boots at power-up or reset.

A system level block diagram is shown in Figure 1-4.

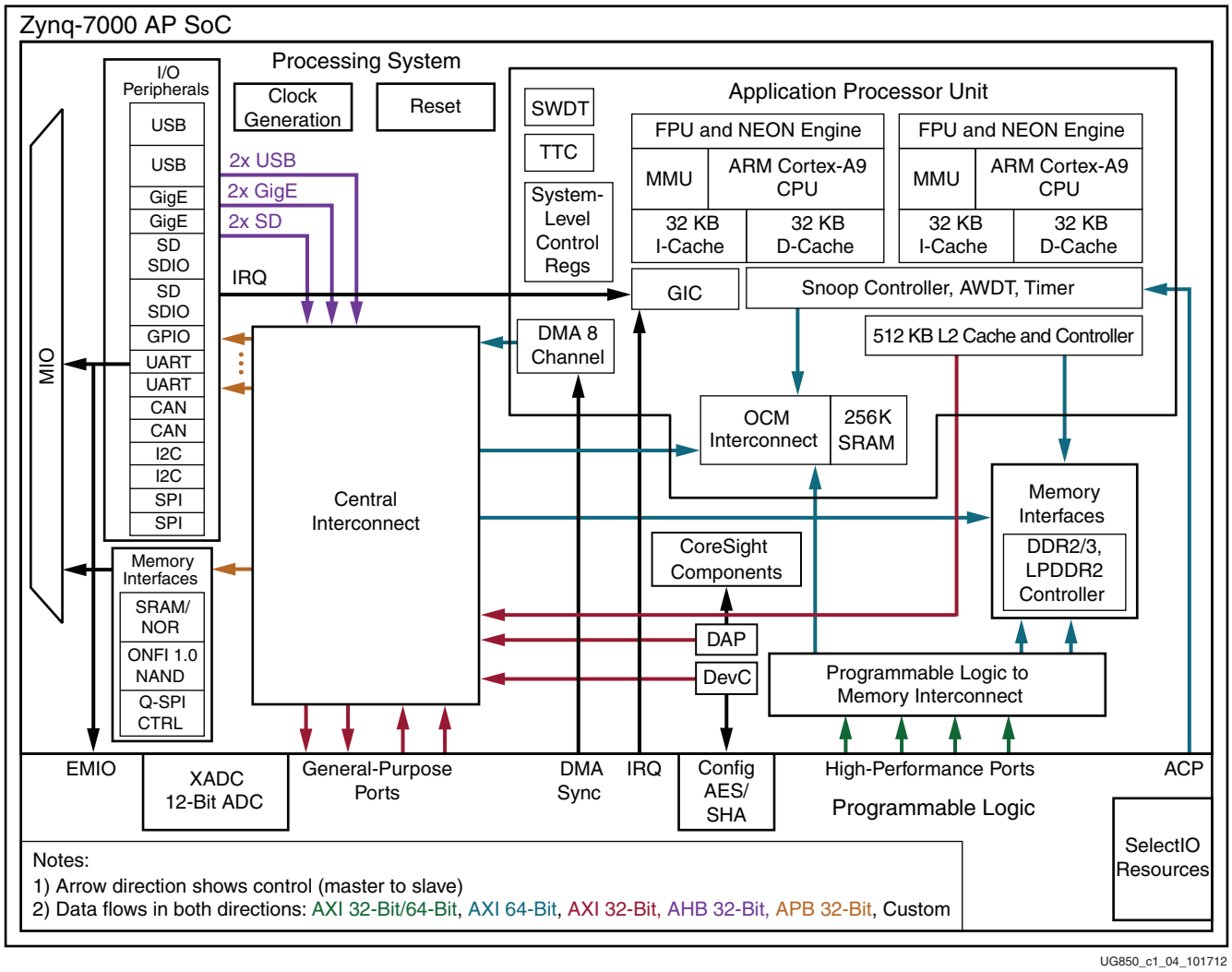


Figure 1-4: **Zynq-7000 AP SoC Block Diagram**

For additional information on Zynq-7000 AP SoC devices, see the *Zynq-7000 All Programmable SoC Overview* (DS190) [Ref 1], and the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 9] for more information about Zynq-7000 AP SoC configuration options.

Device Configuration

Zynq-7000 XC7Z020 AP SoC uses a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the PL must be powered on to enable the use of the security block located within the PL, which provides 256-bit AES and SHA decryption/authentication.

The ZC702 board supports these configuration options:

- PS Configuration: Quad SPI flash memory
- PS Configuration: Processor System Boot from SD Card (J64)
- PL Configuration: USB JTAG configuration port (Digilent module)
- PL Configuration: Platform cable header J2 and flying lead header J58 JTAG configuration ports

TIP: *Designs using serial configuration based on Quad-SPI flash memory can take advantage of low-cost commodity SPI flash memory.*

The JTAG configuration option is selected by setting SW16 as shown in Table 1-2 and SW10 as described in Programmable Logic JTAG Programming Options, page 26 for PL configuration details. SW10 is callout 23 in Figure 1-2.

Table 1-2: **Switch SW16 Configuration Option Settings**

Boot Mode	SW16.1	SW16.2	SW16.3	SW16.4	SW16.5
JTAG mode(1)	0	0	0	0	0
Independent JTAG mode	1	0	0	0	0
Quad SPI mode	0	0	0	1	0
SD mode	0	0	1	1	0
MIO configuration pin	MIO2	MIO3	MIO4	MIO5	MIO6

Notes:

1. Default switch setting

Note: For more information about Zynq-7000 AP SoC configuration settings, see the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 9].

Encryption Key Backup Circuit

The XC7Z020 AP SoC U1 implements bitstream encryption key technology. The ZC702 board provides the encryption key backup battery circuit shown in Figure 1-5.

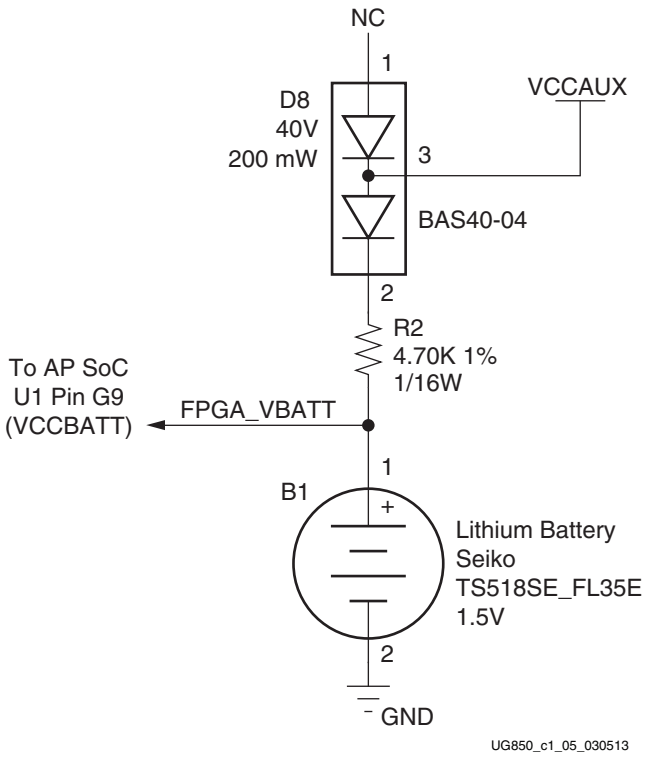


Figure 1-5: **Encryption Key Backup Circuit**

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XC7Z020 AP SoC U1 VCCBATT pin G9. The battery supply current IBATT specification is 150 nA maximum when board power is off. B1 is charged from the VCCAUX 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

There are four PL I/O banks available on the XC7Z020 AP SoC. The voltages applied to the XC7Z020 AP SoC I/O banks used by the ZC702 board are listed in Table 1-3.

Table 1-3: **I/O Voltage Rails**

XC7Z020 (U1) Bank	Net Name	Voltage	Connected To
PL Bank 0	VCC2V5_PL	2.5V	AP SoC Configuration Bank 0
PL Bank 13	VADJ(1)	2.5V	FMC2, GPIO, PL_PJTAG, IIC_MAIN
PL Bank 33			FMC2, HDMI Codec
PL Bank 34			FMC1, HDMI Codec
PL Bank 35			FMC1, HDMI Codec, XADC_GPIO, GPIO
PS Bank 500	VCCMIO_PS	1.8V	Quad-SPI flash memory, misc
PS Bank 501			Ethernet PHY, USB ULPI Transceiver, SDIO, CAN
PS Bank 502	VCC1V5_PS	1.5V	PS_DDR3 MEM

Notes:
1. The ZC702 board is shipped with V_{ADJ} set to 2.5V.

DDR3 Component Memory

[Figure 1-2, callout 2]

The 1 GB, 32-bit wide DDR3 memory system is comprised of four 256 Mb x 8 SDRAMs (Micron MT41J256M8HX-15E) at U66–U69. This memory system is connected to the XC7Z020 AP SoC processing system (PS) memory interface bank 502. The DDR3 0.75V V_{TT} termination voltage is sourced from linear regulator U22. The connections between the DDR3 memory and XC7Z020 AP SoC bank 502 are listed in Table 1-4.

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC**

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
E3	PS_DDR3_DQ0	B3	DQ0	U66
C3	PS_DDR3_DQ1	C7	DQ1	U66
F2	PS_DDR3_DQ2	C2	DQ2	U66
D1	PS_DDR3_DQ3	C8	DQ3	U66
F1	PS_DDR3_DQ4	E3	DQ4	U66
E1	PS_DDR3_DQ5	E8	DQ5	U66
B2	PS_DDR3_DQ6	D2	DQ6	U66
D3	PS_DDR3_DQ7	E7	DQ7	U66

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
G2	PS_DDR3_DQ8	B3	DQ8	U67
L1	PS_DDR3_DQ9	C7	DQ9	U67
G1	PS_DDR3_DQ10	C2	DQ10	U67
K1	PS_DDR3_DQ11	C8	DQ11	U67
L3	PS_DDR3_DQ12	E3	DQ12	U67
L2	PS_DDR3_DQ13	E8	DQ13	U67
J1	PS_DDR3_DQ14	D2	DQ14	U67
K3	PS_DDR3_DQ15	E7	DQ15	U67
M1	PS_DDR3_DQ16	B3	DQ16	U68
T3	PS_DDR3_DQ17	C7	DQ17	U68
N3	PS_DDR3_DQ18	C2	DQ18	U68
T1	PS_DDR3_DQ19	C8	DQ19	U68
R3	PS_DDR3_DQ20	E3	DQ20	U68
T2	PS_DDR3_DQ21	E8	DQ21	U68
M2	PS_DDR3_DQ22	D2	DQ22	U68
R1	PS_DDR3_DQ23	E7	DQ23	U68
U1	PS_DDR3_DQ24	B3	DQ24	U69
AA1	PS_DDR3_DQ25	C7	DQ25	U69
U2	PS_DDR3_DQ26	C2	DQ26	U69
AA3	PS_DDR3_DQ27	C8	DQ27	U69
W1	PS_DDR3_DQ28	E3	DQ28	U69
Y3	PS_DDR3_DQ29	E8	DQ29	U69
W3	PS_DDR3_DQ30	D2	DQ30	U69
Y1	PS_DDR3_DQ31	E7	DQ31	U69
B1	PS_DDR3_DM0	B7	DM0	U66
C2	PS_DDR3_DQS0_P	C3	DQS0_P	U66
D2	PS_DDR3_DQS0_N	D3	DQS0_N	U66
H3	PS_DDR3_DM1	B7	DM1	U67
H2	PS_DDR3_DQS1_P	C3	DQS1_P	U67
J2	PS_DDR3_DQS1_N	D3	DQS1_N	U67
P1	PS_DDR3_DM2	B7	DM2	U68
N2	PS_DDR3_DQS2_P	C3	DQS2_P	U68
P2	PS_DDR3_DQS2_N	D3	DQS2_N	U68

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
AA2	PS_DDR3_DM3	B7	DM3	U69
V2	PS_DDR3_DQS3_P	C3	DQS3_P	U69
W2	PS_DDR3_DQS3_N	D3	DQS3_N	U69
M4	PS_DDR3_A0	K3	A0	U66, U67, U68, U69
M5	PS_DDR3_A1	L7	A1	U66, U67, U68, U69
K4	PS_DDR3_A2	L3	A2	U66, U67, U68, U69
L4	PS_DDR3_A3	K2	A3	U66, U67, U68, U69
K6	PS_DDR3_A4	L8	A4	U66, U67, U68, U69
K5	PS_DDR3_A5	L2	A5	U66, U67, U68, U69
J7	PS_DDR3_A6	M8	A6	U66, U67, U68, U69
J6	PS_DDR3_A7	M2	A7	U66, U67, U68, U69
J5	PS_DDR3_A8	N8	A8	U66, U67, U68, U69
H5	PS_DDR3_A9	M3	A9	U66, U67, U68, U69
J3	PS_DDR3_A10	H7	A10	U66, U67, U68, U69
G5	PS_DDR3_A11	M7	A11	U66, U67, U68, U69
H4	PS_DDR3_A12	K7	A12	U66, U67, U68, U69
F4	PS_DDR3_A13	N3	A13	U66, U67, U68, U69
G4	PS_DDR3_A14	N7	A14	U66, U67, U68, U69
L7	PS_DDR3_BA0	J2	BA0	U66, U67, U68, U69
L6	PS_DDR3_BA1	K8	BA1	U66, U67, U68, U69
M6	PS_DDR3_BA2	J3	BA2	U66, U67, U68, U69
N4	PS_DDR3_CLK_P	F7	CK	U66, U67, U68, U69
N5	PS_DDR3_CLK_N	G7	CK_B	U66, U67, U68, U69
V3	PS_DDR3_CKE	G9	CKE	U66, U67, U68, U69
R4	PS_DDR3_WE_B	H3	WE_B	U66, U67, U68, U69
P3	PS_DDR3_CAS_B	G3	CAS_B	U66, U67, U68, U69
R5	PS_DDR3_RAS_B	F3	RAS_B	U66, U67, U68, U69
F3	PS_DDR3_RESET_B	N2	RESET_B	U66, U67, U68, U69
P6	PS_DDR3_CS_B	H2	CS_B	U66, U67, U68, U69
P5	PS_DDR3_ODT	G1	ODT	U66, U67, U68, U69
M7	PS_VRN			
N7	PS_VRP			

Table 1-4: **DDR3 Component Memory Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1) Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Reference Designator
H7	VTTVREF_PS			
P7	VTTVREF_PS			

Note: The ZC702 DDR3 4x 8-bit component memory interface adheres to the constraints guidelines documented in the DDR3 Design Guidelines section of the *7 Series FPGAs Memory Interface Solutions v1.8 User Guide* (UG586) [Ref 10]. The ZC702 DDR3 memory interface is a 40Ω impedance implementation. Other memory interface details are available in UG586 and the *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 5]. For more details, see the Micron MT41J256M8HX-15E data sheet at the Micron website [Ref 15].

Quad-SPI Flash Memory

[Figure 1-2, callout 3]

The Quad-SPI flash memory located at U41 provides 128 Mb of non-volatile storage that can be used for configuration and data storage.

- Part number: N25Q128A11ESF40G (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: Various depending on Single/Dual/Quad mode

The connections between the SPI flash memory and the XC7Z020 AP SoC are listed in Table 1-5.

Table 1-5: **Quad SPI Flash Memory Connections to the XC7Z020 AP SoC**

XC7Z020 (U1)			Schematic Net Name	Quad-SPI Flash Memory (U41)		MIO Select Header
Pin Name	Bank	Pin Number		Pin Number	Pin Name	
PS_MIO6	500	A4	QSPI_CLK	16	C	J26.2
PS_MIO5	500	A3	QSPI_IO3	1	DQ3_HOLD_B	J25.2
PS_MIO4	500	E4	QSPI_IO2	9	WP_B	J22.2
PS_MIO3	500	F6	QSPI_IO1	8	DQ1	J20.2
PS_MIO2	500	A2	QSPI_IO0	15	DQ0	J21.2
PS_MIO1	500	A1	QSPI_CS_B	7	S_B	NA

Notes:

Each three-pin MIO select header has pin 1 wired to VCCMIO and pin 3 wired to GND.

The configuration and Quad SPI section of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 9] provides details on using the Quad-SPI flash memory.

Figure 1-6 shows the connections of the linear Quad SPI flash memory on the ZC702 board. For more details, see the Micron N25Q128A11ESF40G data sheet at the Micron website [Ref 15].

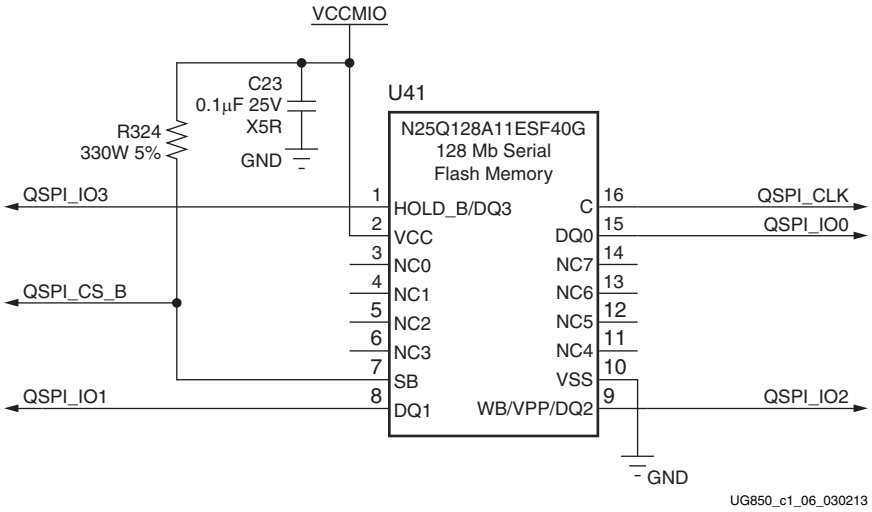


Figure 1-6: **128 Mb Quad-SPI Flash Memory (U41)**

USB 2.0 ULPI Transceiver

[Figure 1-2, callout 4]

The ZC702 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver at U9 to support a USB connection to the host computer. A USB cable is supplied in the ZC702 Evaluation Kit (Standard-A connector to host computer, Mini-B connector to ZC702 board connector J1). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal. Consult the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details [Ref 16].

The interface to the USB3320 transceiver is implemented through the IP in the XC7Z020 AP SoC Processor System.

Table 1-6 describes the jumper settings for the USB 2.0 circuit. **Bold** text identifies the default shunt positions for USB 2.0 high speed on-the-go (OTG) mode.

Table 1-6: **USB Jumper Settings**

Header	Function	Shunt Position	Notes
J44	USB PHY reset	Shunt ON = USB PHY reset **Shunt OFF = USB PHY normal operation**	Clean reset requires external debouncing
J7	VBUS 5V supply	**Shunt ON = Host or OTG mode** Shunt OFF = Device mode	
J33	RVBUS select	Position 1–2 = Device mode (10 kΩ) **Position 2–3 = OTG mode (1 kΩ)**	Overvoltage protection
J35	CVBUS select	Position 1-2 = OTG and Device mode (1 µF) **Position 2-3 = Host mode (120 µF)**	VBUS load capacitance
J34	Cable ID select	**Position 1-2 = A/B cable detect** Position 2-3 = ID not used	Used in OTG mode.
J36	USB Micro-B	**Position 1-2 = Shield connected to GND** Position 2-3 = Shield floating	

The connections between the USB Mini-B connector at J1 and the PHY at U9 are listed in Table 1-7.

Table 1-7: **USB Connector Pin Assignments and Signal Definitions Between J1 and U9**

USB Connector J1		Net Name	Description	USB3320 (U9) Pin
Pin	Name			
1	VBUS	USB_VBUS_SEL	+5V from host system	22
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	18
5	GND	GND	Signal ground	33

The connections between the USB 2.0 PHY at U9 and the XC7Z020 AP SoC are listed in Table 1-8.

Table 1-8: **USB 2.0 ULPI Transceiver Connections to the XC7Z020 AP SoC**

XC7Z020 (U1)			Schematic Net Name	USB3320 (U9) Pin
Pin Name	Bank	Pin Number		
PS_MIO36	501	A9	USB_CLKOUT	1
PS_MIO31	501	F9	USB_NXT	2
PS_MIO32	501	C7	USB_DATA0	3
PS_MIO33	501	G13	USB_DATA1	4
PS_MIO34	501	B12	USB_DATA2	5

Table 1-8: **USB 2.0 ULPI Transceiver Connections to the XC7Z020 AP SoC *(Cont'd)***

XC7Z020 (U1)			Schematic Net Name	USB3320 (U9) Pin
Pin Name	Bank	Pin Number		
PS_MIO35	501	F14	USB_DATA3	6
PS_MIO28	501	A12	USB_DATA4	7
PS_MIO37	501	B14	USB_DATA5	9
PS_MIO38	501	F13	USB_DATA6	10
PS_MIO39	501	C13	USB_DATA7	13
PS_MIO30	501	A11	USB_STP	29
PS_MIO29	501	E8	USB_DIR	31
PS_MIO7	500	D5	USB_RESET_B_AND	27 (through AND gate U62)

Figure 1-7 shows the USB 2.0 ULPI Transceiver circuitry. Note that the shield for the USB Mini-B connector (J1) can be tied to GND by a jumper on header J36 pins 1–2 (default). The USB shield can optionally be connected through a capacitor to GND by installing a capacitor (body size 0402) at location C202 and jumping pins 2-3 on header J36.

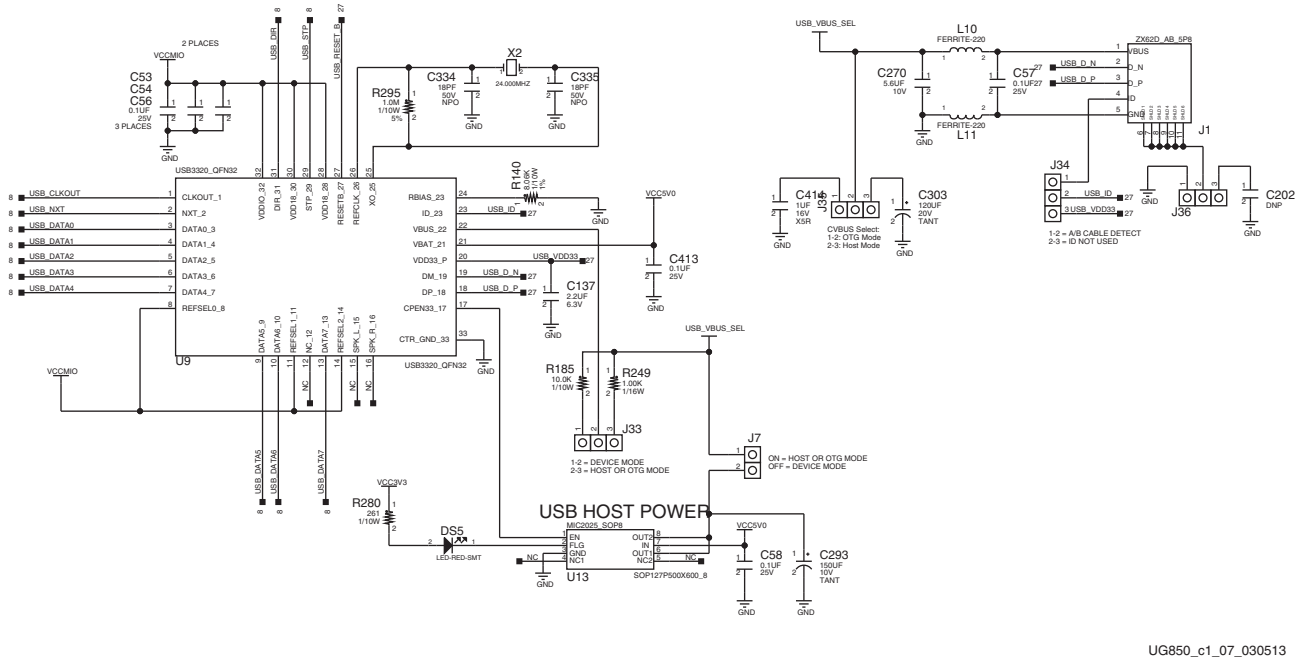


Figure 1-7: **USB 2.0 ULPI Transceiver**

SD Card Interface

[Figure 1-2, callout 5]

The ZC702 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found at the SanDisk Corporation [Ref 17] or SD Association [Ref 18] websites.

The SDIO signals are connected to XC7Z020 AP SoC PS bank 501 which has its VCCMIO set to 1.8V. A TXB02612 SDIO port expander with voltage-level translation (U61) is used between the XC7Z020 AP SoC and the SD card connector (J64).

Figure 1-8 shows the connections of the SD card interface on the ZC702 board.

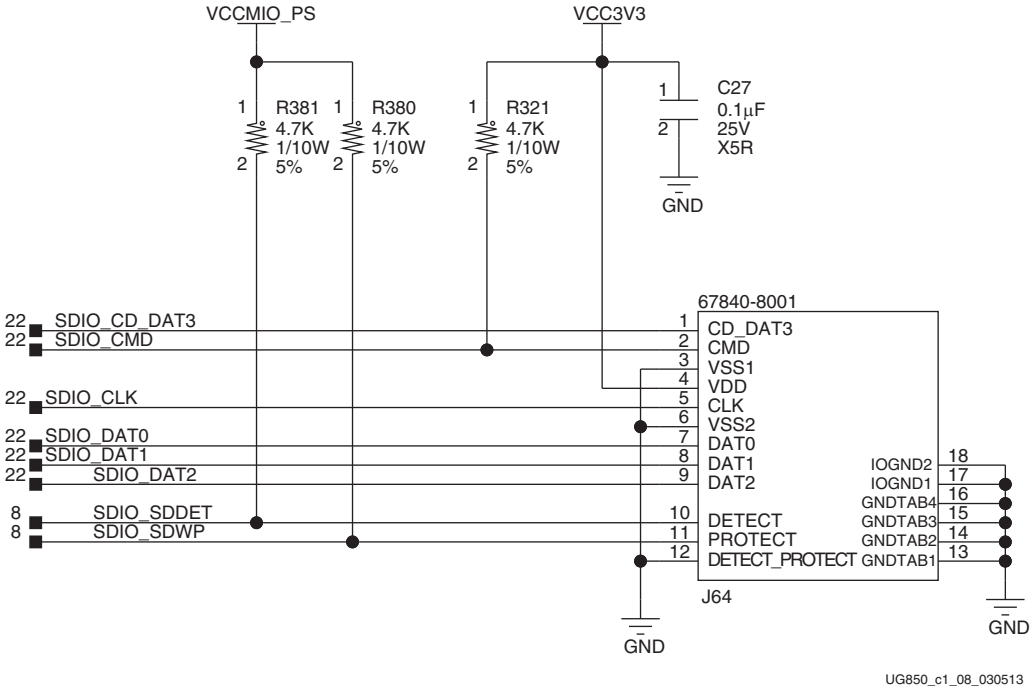


Figure 1-8: **SD Card Interface**

Table 1-9 lists the SD card interface connections to the XC7Z020 AP SoC.

Table 1-9: **SDIO Connections to the XC7Z020 AP SoC**

XC7Z020 (U1) Pin			Schematic Net Name	Level Shifter (U61)		SDIO Connector (J64)	
Pin Name	Bank	Pin Number		(A) Pin Number	(B) Pin Number	Pin Number	Pin Name
PS_MIO15	500	E6	SDIO_SDWP	N/A	N/A	11	PROTECT
PS_MIO0	500	G6	SDIO_SDDET	N/A	N/A	10	DETECT
PS_MIO41	501	C8	SDIO_CMD_LS	4	20	2	CMD
PS_MIO40	501	E14	SDIO_CLK_LS	9	19	5	CLK
PS_MIO42	501	D8	SDIO_DAT2_LS	1	23	9	DAT2
PS_MIO45	501	B9	SDIO_DAT1_LS	7	16	8	DAT1
PS_MIO44	501	E13	SDIO_DAT0_LS	6	18	7	DAT0
PS_MIO43	501	B11	SDIO_CD_DAT3_LS	3	22	1	CD_DAT3

Programmable Logic JTAG Programming Options

[Figure 1-2, callout 6]

The ZC702 board JTAG chain is shown in Figure 1-9.

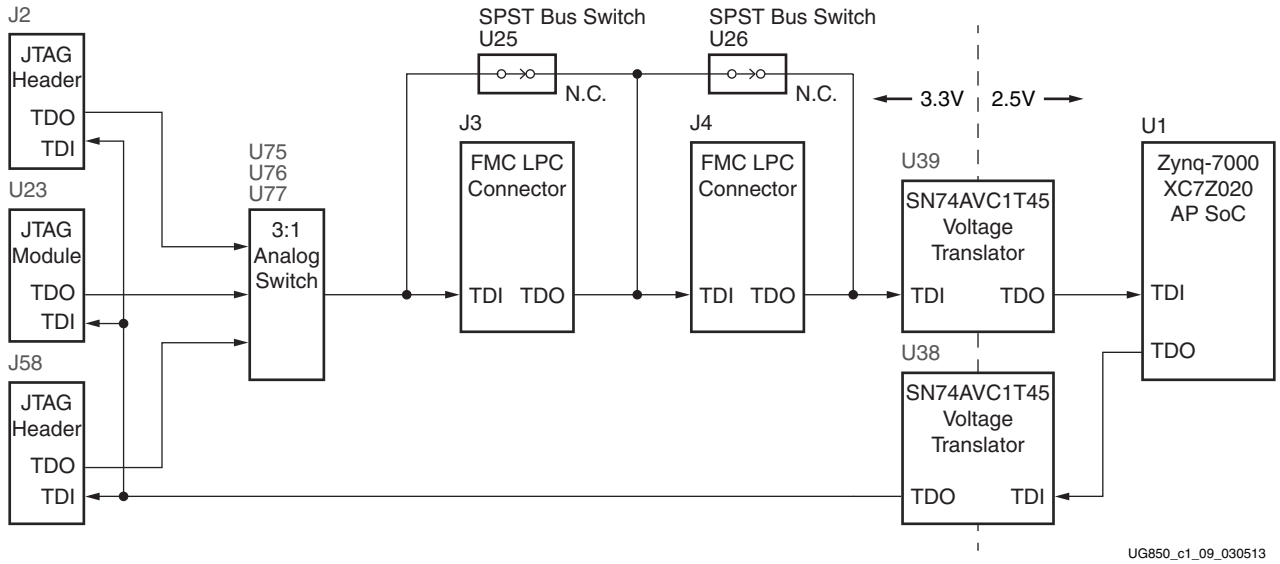


Figure 1-9: **JTAG Chain Block Diagram**

Programmable Logic JTAG Select Switch, JTAG Cable Connector

[Figure 1-2, callout 23]

The JTAG chain can be programmed by three different methods made available through a 3-to-1 analog switch (U75, U76, and U77) controlled by a 2-position DIP switch at SW10.

Figure 1-10 shows the JTAG analog switches and DIP switch SW10.

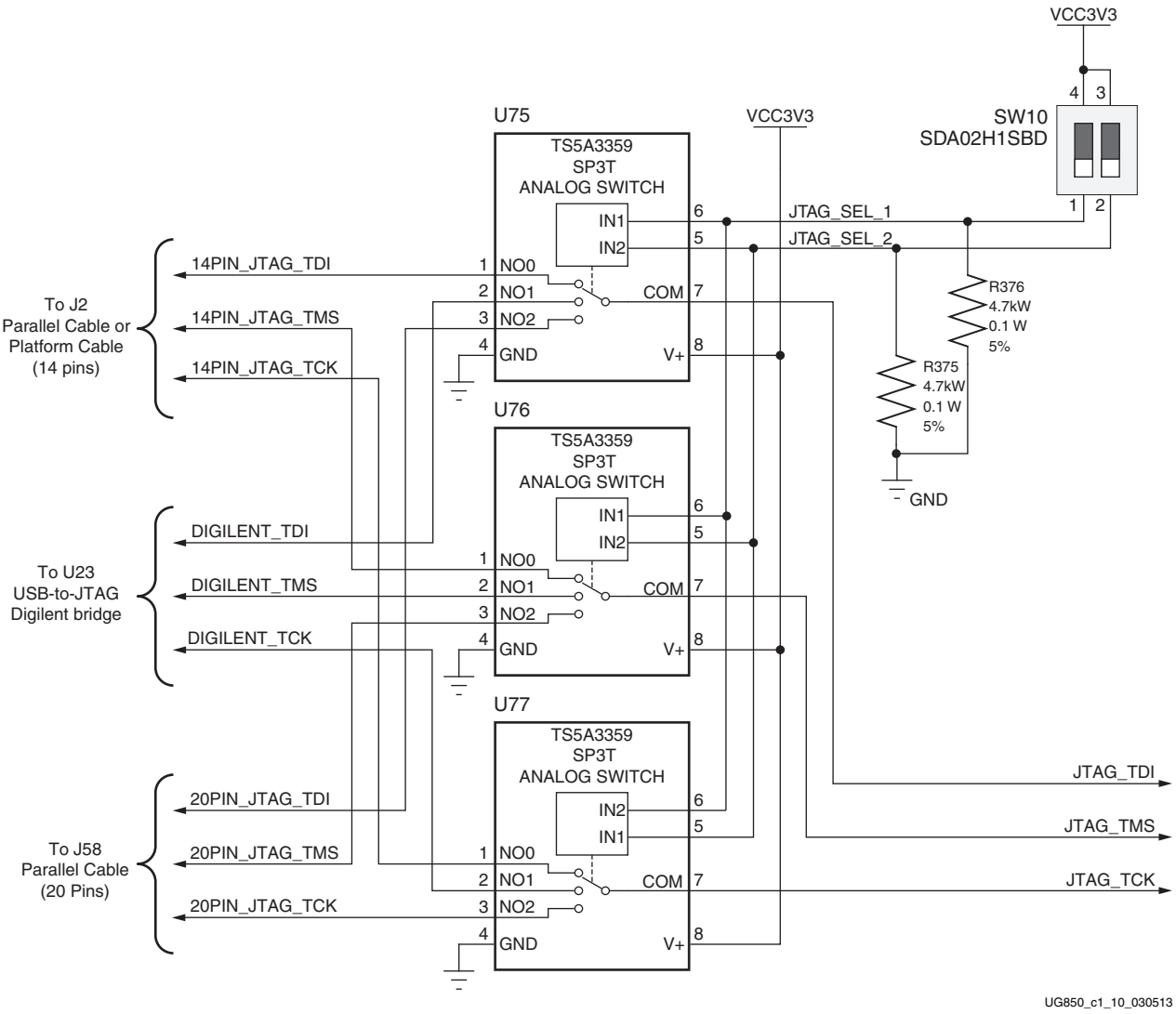


Figure 1-10: **PL JTAG Programming Source Analog Switch**

DIP switch SW10[1:2] setting `10` selects the 14-pin header J2 for configuration using either a Parallel Cable IV (PC4) or Platform Cable USB II. DIP switch SW10 setting `01` selects the USB-to-JTAG Digilent bridge U23 for configuration over a Standard-A to Micro-B USB cable. DIP switch SW10 setting `11` selects the JTAG 20-pin header at J58. The four JTAG signals TDI,

TDO, TCK, and TMS would be connected to J58 through flying leads from a JTAG cable. The 3-to-1 analog switch settings are shown in Table 1-10.

Table 1-10: **Switch SW10 JTAG Configuration Option Settings**

Configuration Source	DIP Switch SW10[1:2]	
	Switch 1[(1)] JTAG_SEL_1	Switch 2[(1)] JTAG_SEL_2
None	0	0
Digilent USB-to-JTAG interface U23	0	1
Cable connector J2[(2)]	1	0
JTAG header J58	1	1

Notes:
1. 0 = open, 1 = closed
2. Default switch setting

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to J3 or J4 it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U25 and U26. The SPST switches are normally closed and transition to an open state when an FMC is attached. Switch U25 adds an attached FMC to the JTAG chain as determined by the FMC1_HPC_PRSNT_M2C_B signal. Switch U26 adds an attached FMC to the JTAG chain as determined by the FMC2_LPC_PRSNT_M2C_B signal The attached FMC card must implement a TDI-to-TDO connection using a device or bypass jumper to ensure that the JTAG chain connects to the XC7Z020 AP SoC.

Clock Generation

The ZC702 board provides three clock sources for the XC7Z020 AP SoC. Table 1-11 lists the source devices for each clock.

Table 1-11: **ZC702 Board Clock Sources**

Clock Name	Clock Source	Description
System Clock	U43	SiT9102 2.5V LVDS 200 MHz fixed-frequency oscillator (SiTime). See System Clock.
User Clock	U28	Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default (Silicon Labs). See Programmable User Clock.
PS Clock	U65	SIT8103 1.8V single-ended CMOS 33.3333 MHz fixed frequency oscillator (SiTime). See Processing System Clock Source.

Table 1-12 lists the pin-to-pin connections from each clock source to the XC7Z020 AP SoC.

Table 1-12: **Clock Connections, Source to XC7Z020 AP SoC**

Clock Reference	Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
U43	5	SYSCLK_N	LVDS_25	C19
	4	SYSCLK_P	LVDS_25	D18
U28	5	USRCLK_N	LVDS_25	Y8
	4	USRCLK_P	LVDS_25	Y9
U65	3	PS_CLK	NA	F7 (Bank 500)

System Clock

[Figure 1-2, callout 7]

The system clock source is an LVDS 200 MHz oscillator at U43. It is wired to a multi-region clock capable (MRCC) input on programmable logic (PL) bank 35. The signal pair is named SYSCLK_P and SYSCLK_N and each signal is connected to U1 pins D18 and C19 respectively on the XC7Z020 AP SoC.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- Frequency Tolerance: 50 ppm
- Differential Output

For more details, see the SiTime SiT9102 data sheet [Ref 19]. The system clock circuit is shown in Figure 1-11.

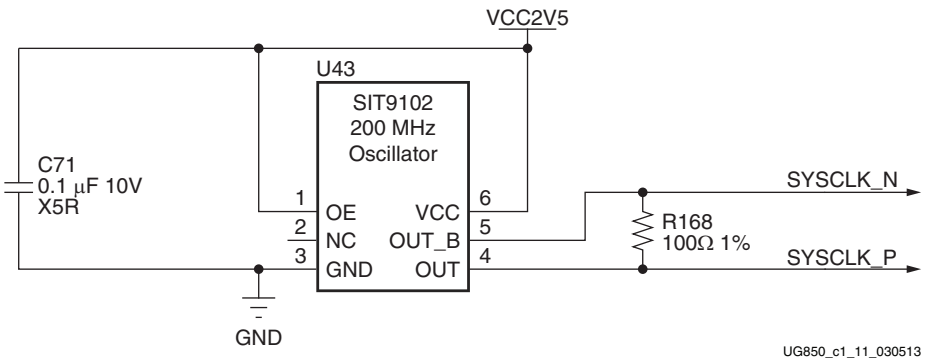


Figure 1-11: **System Clock Source**

Programmable User Clock

[Figure 1-2, callout 8]

The ZC702 board has a programmable low-jitter 3.3V LVDS differential oscillator (U28) connected to the MRCC inputs of bank 13. This USRCLK_P and USRCLK_N clock signal pair is connected to XC7Z020 AP SoC U1 pins Y9 and Y8 respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the ZC702 board reverts the user clock to the default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz–810 MHz)
- LVDS Differential Output

The user clock circuit is shown in Figure 1-12.

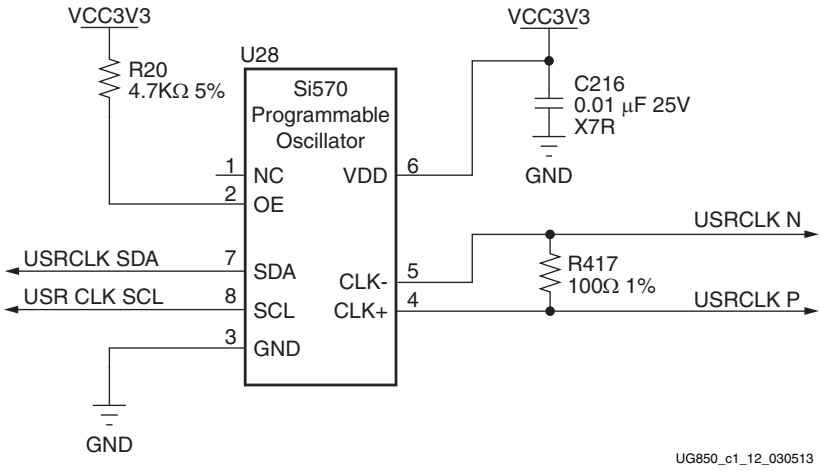


Figure 1-12: **User Clock Source**

The Silicon Labs Si570 data sheet is available on the Silicon Labs website [Ref 20].

Processing System Clock Source

[Figure 1-2, callout 8]

The Processing System (PS) clock source is a 1.8V LVCMOS single-ended fixed 33.33333 MHz oscillator at U65. It is wired to PS bank 500, pin F7 (PS_CLK), on the XC7Z020 AP SoC.

- Oscillator: SiTime SiT8103AC-23-18E-33.33333 (33.3 MHz)
- Frequency Tolerance: 50 ppm
- Single-ended output

For more details, see the SiTime SiT8103 data sheet [Ref 19].

The system clock circuit is shown in Figure 1-13.

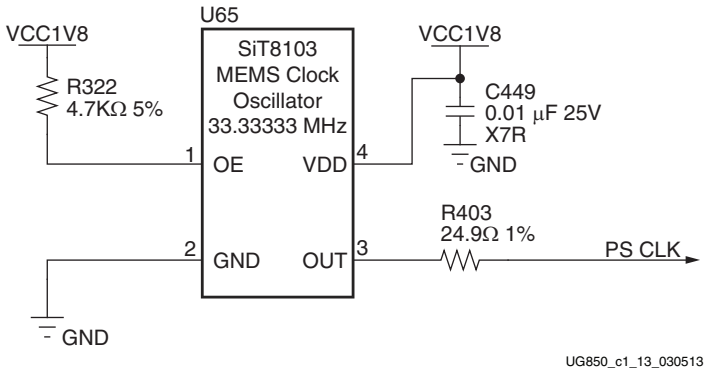


Figure 1-13: **Processing System Clock Source**

10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 1-2, callout 9]

The ZC702 board uses the Marvell Alaska PHY device (88E1116R) at U35 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Halo HFJ11-1G01E RJ-45 connector (P2) with built-in magnetics.

On power-up, or on reset, the PHY is configured to operate in RGMII mode with PHY address `0b00111` using the settings shown in Table 1-13. These settings can be overwritten using software commands passed over the MDIO interface.

Table 1-13: **Board Connections for PHY Configuration Pins**

U35 Pin	Setting	Configuration	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

The Ethernet connections from the XC7Z020 AP SoC at U1 to the 88E1116R PHY device at U35 are listed in Table 1-14.

Table 1-14: **Ethernet Connections, XC7Z020 AP SoC to the PHY Device**

XC7Z020 (U1) Pin			Schematic Net Name	M88E1116R PHY U35	
Pin Name	Bank	Pin Number		Pin	Name
PS_MIO53	501	C12	PHY_MDIO	45	MDIO
PS_MIO52	501	D10	PHY_MDC	48	MDC
PS_MIO16	501	D6	PHY_TX_CLK	60	TX_CLK
PS_MIO21	501	F11	PHY_TX_CTRL	63	TX_CTRL
PS_MIO20	501	A8	PHY_TXD3	62	TXD3
PS_MIO19	501	E10	PHY_TXD2	61	TXD2
PS_MIO18	501	A7	PHY_TXD1	59	TXD1
PS_MIO17	501	E9	PHY_TXD0	58	TXD0
PS_MIO22	501	A14	PHY_RX_CLK	53	RX_CLK
PS_MIO27	501	D7	PHY_RX_CTRL	49	RX_CTRL
PS_MIO26	501	A13	PHY_RXD3	55	RXD3
PS_MIO25	501	F12	PHY_RXD2	54	RXD2
PS_MIO24	501	B7	PHY_RXD1	51	RXD1
PS_MIO23	501	E11	PHY_RXD0	50	RXD0

Ethernet PHY Clock Source

[Figure 1-2, callout 10]

A 25.00 MHz 50 ppm crystal at X1 is the clock source for the 88E1116R PHY at U35. Figure 1-14 shows the clock source.

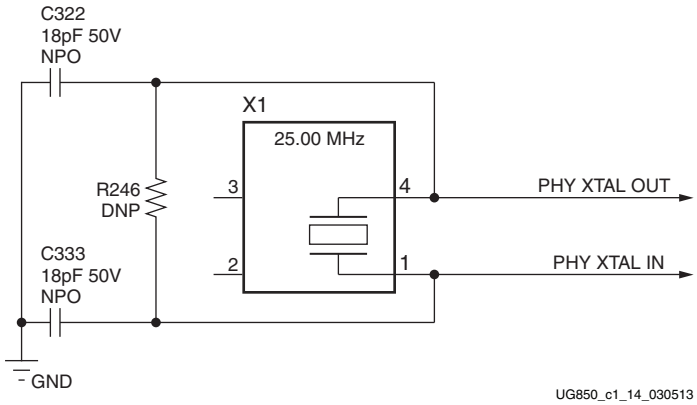


Figure 1-14: **Ethernet PHY Clock Source**

The data sheet can be obtained under NDA with Marvell. The Marvell site includes contact information [Ref 21],

USB-to-UART Bridge

[Figure 1-2, callout 12]

The ZC702 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U36) which allows a connection to a host computer with a USB port. The USB cable is supplied in the ZC702 Evaluation Kit (Standard-A end to host computer, Type Mini-B end to ZC702 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the ZC702 board.

The CP2013GM TX and RX pins are wired to the UART_1 IP block within the XC7Z020 AP SoC PS I/O Peripherals set. The XC7Z020 AP SoC supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer.

IMPORTANT: *The VCP device drivers must be installed on the host PC prior to establishing communications with the ZC702 board.*

The USB Connector pin assignments and signal definitions between J17 and U36 are listed in Table 1-15.

Table 1-15: **USB Connector J17 Pin Assignments and Signal Definitions**

USB Connector (J17)		Net Name	Description	CP2103GM (U36)	
Pin	Name			Pin	Name
1	VBUS	USB_UART_VBUS	+5V VBUS Powered	7	REGIN
				8	VBUS
2	D_N	USB_UART_D_N	Bidirectional differential serial data (N-side)	4	D –
3	D_P	USB_UART_D_P	Bidirectional differential serial data (P-side)	3	D +
5	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 1-16 lists the USB connections between the XC7Z020 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 1-16: **XC7Z020 AP SoC to CP2103 Connections**

XC7Z020 AP SoC (U1) Bank 500				Net Name	CP2103GM Device (U36)		
Pin Name	Pin Number	Function	Direction		Pin	Function	Direction
PS_MIO48	D11	TX	Data Out	USB_UART_RX	24	RXD	Data In
PS_MIO49	C14	RX	Data In	USB_UART_TX	25	TXD	Data Out

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers [Ref 20].

HDMI Video Output

[Figure 1-2, callout 13]

The ZC702 board provides a high-definition multimedia interface (HDMI®) video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U40. The HDMI output is provided on a Molex 500254-1927 HDMI type-A receptacle at P1. The ADV7511 supports 1080P 60Hz, YCbCr 4:2:2 encoding via 16-bit input data mapping.

The ZC702 board supports the following HDMI device interfaces:

- 16 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out pin to XC7Z020 AP SoC
- I2C
- SPDIF

Figure 1-15 shows the HDMI codec circuit.

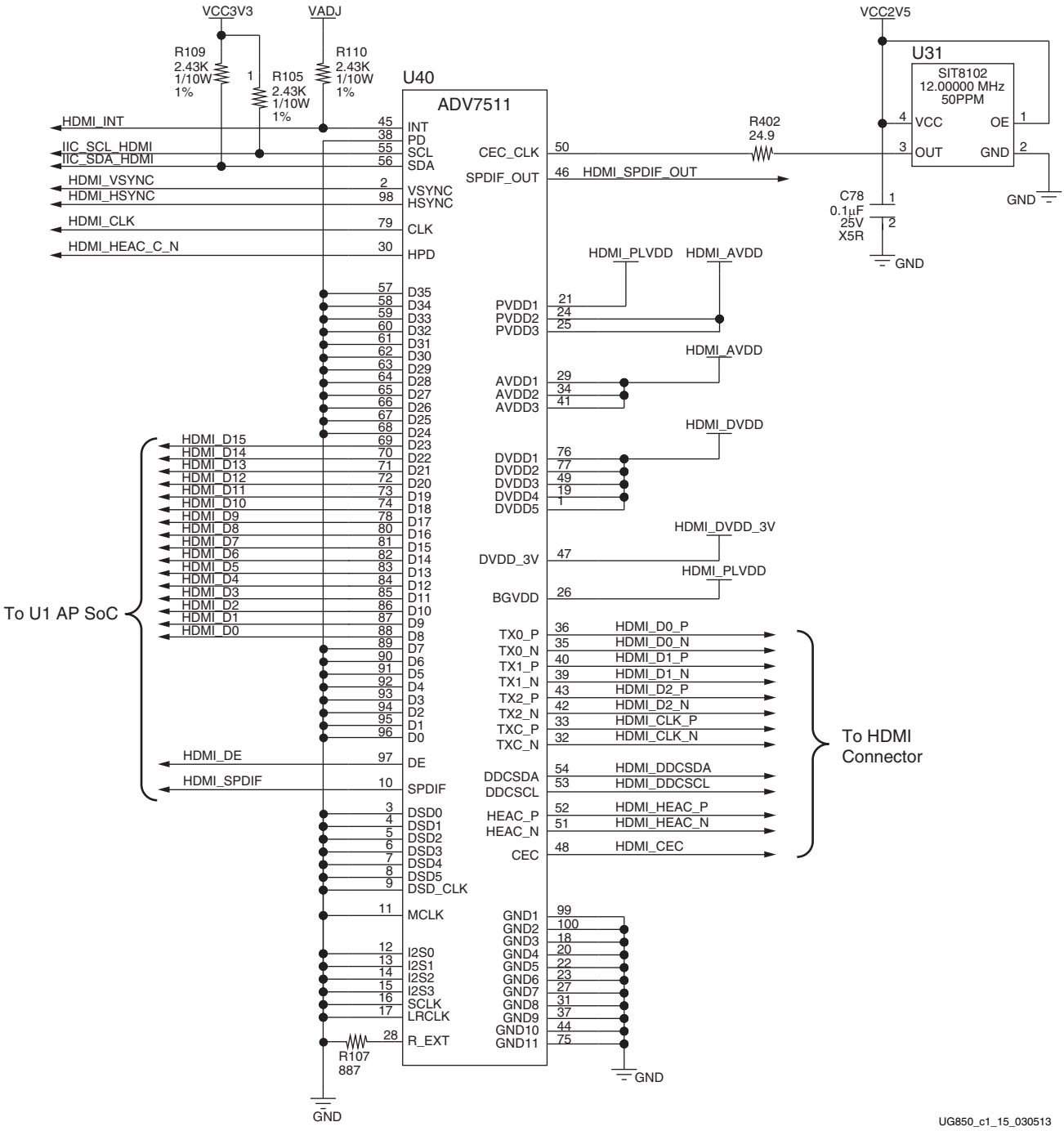


Figure 1-15: **HDMI Codec Circuit**

Table 1-17 lists the connections between the codec and the XC7Z020 AP SoC.

Table 1-17: **XC7Z020 AP SoC to HDMI Codec Connections (ADV7511)**

XC7Z020 (U1) Pin	Net Name	I/O Standard	ADV7511 (U40)	
			Pin	Name
AB21	HDMI_D0	LVCMOS25	88	D8
AA21	HDMI_D1	LVCMOS25	87	D9
AB22	HDMI_D2	LVCMOS25	86	D10
AA22	HDMI_D3	LVCMOS25	85	D11
V19	HDMI_D4	LVCMOS25	84	D12
V18	HDMI_D5	LVCMOS25	83	D13
V20	HDMI_D6	LVCMOS25	82	D14
U20	HDMI_D7	LVCMOS25	81	D15
W21	HDMI_D8	LVCMOS25	80	D16
W20	HDMI_D9	LVCMOS25	78	D17
W18	HDMI_D10	LVCMOS25	74	D18
T19	HDMI_D11	LVCMOS25	73	D19
U19	HDMI_D12	LVCMOS25	72	D20
R19	HDMI_D13	LVCMOS25	71	D21
T17	HDMI_D14	LVCMOS25	70	D22
T16	HDMI_D15	LVCMOS25	69	D23
T18	HDMI_DE	LVCMOS25	97	DE
R15	HDMI_SPDIF	LVCMOS25	10	SPDIF
L16	HDMI_CLK	LVCMOS25	79	CLK
H15	HDMI_VSYNC	LVCMOS25	2	VSYNC
R18	HDMI_HSYNC	LVCMOS25	98	HSYNC
U14	HDMI_INT	LVCMOS25	45	INT
H20	HDMI_SPDIF_OUT	LVCMOS25	46	SPDIF_OUT

Table 1-18 lists the connections between the codec and the HDMI receptacle P1.

Table 1-18: **ADV7511 to HDMI Receptacle Connections**

ADV7511 (U40)	Net Name	HDMI Receptacle P1 Pin
36	HDMI_D0_P	7
35	HDMI_D0_N	9
40	HDMI_D1_P	4
39	HDMI_D1_N	6
43	HDMI_D2_P	1

Table 1-18: **ADV7511 to HDMI Receptacle Connections *(Cont'd)***

ADV7511 (U40)	Net Name	HDMI Receptacle P1 Pin
42	HDMI_D2_N	3
33	HDMI_CLK_P	10
32	HDMI_CLK_N	12
54	HDMI_DDCSDA	16
53	HDMI_DDCSCL	15
52	HDMI_HEAC_P	14
51	HDMI_HEAC_N	19
48	HDMI_CEC	13

Information about the ADV7511KSTZ-P is available on the Analog Devices website [Ref 22].

I2C Bus

[Figure 1-2, callout 14]

The ZC702 board implements a single I2C port on the XC7Z020 AP SoC (IIC_SDA_MAIN, IIC_SDA_SCL), which is routed through an TI Semiconductor PCA9548 1-to-8 channel I2C bus switch (U44). The bus switch can operate at speeds up to 400 kHz.

The bus switch I2C address is `0x74` (`0b1110100`) and must be addressed and configured to select the desired downstream device.

The ZC702 board I2C bus topology is shown in Figure 1-16.

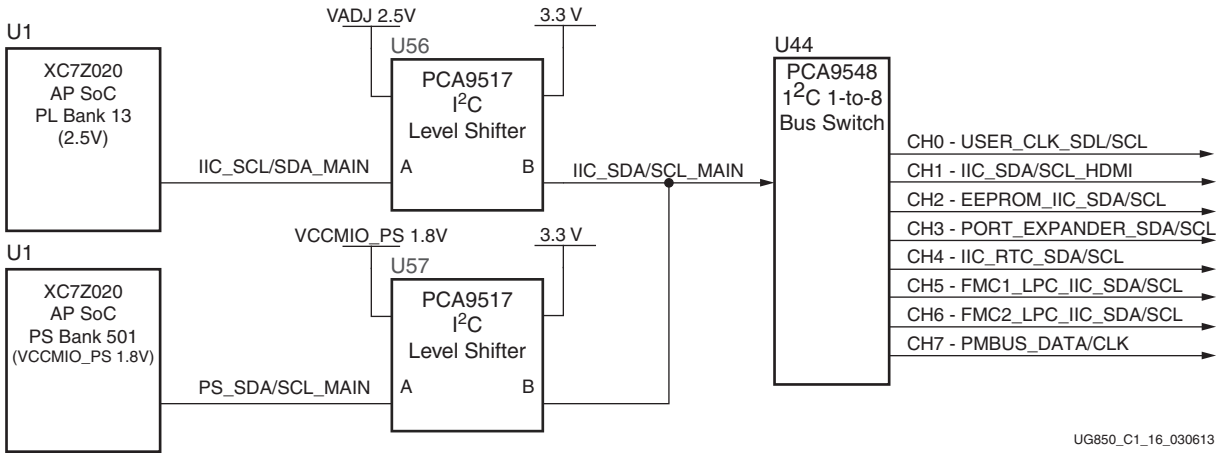


Figure 1-16: **I2C Bus Topology**

User applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired bus through the U44 bus switch at I2C address 0x74 (0b1110100). Table 1-19 lists the address for each bus.

Table 1-19: **I2C Bus Addresses**

I2C Device	I2C Switch Position	I2C Address
PCA9548 8-channel bus switch	NA	0b1110100
Si570 clock	0	0b1011101
ADV7511 HDMI	1	0b0111001
I2C EEPROM	2	0b1010100
I2C port expander	3	0b0100001
I2C real time clock	4	0b1010001
FMC LPC J3	5	0bxxxxx00
FMC LPC J4	6	0bxxxxx00
UCD9248 controller PMBUS	7	0b01101[ADDR] (1)

Notes:
1. This I2C address is the binary equivalent of the TI Power Controller PMBus decimal address 52, 53, or 54 which corresponds to b00, b01 and b10 in the lower 2 bits.

IMPORTANT: *The PCA9548 I2C bus switch U44 pin 24 net IIC_MUX_RESET_B is level-shifted by U81 and is connected to the XCZ020 AP SoC U1 bank 500 pin A6. This is an active-Low signal and must be driven High to enable I2C bus transactions between the U1 and the other components on the I2C bus.*

Information about the PCA9548 is available on the TI Semiconductor website at [Ref 26].

Real-Time Clock

[Figure 1-2, callout 15]

The Epson RTC-8564JE is an 1^2C bus interface real-time clock that has a built-in 32.768 KHz oscillator with these features

- Frequency output options: 32.768 KHz, 1024 Hz, 32 Hz or 1 Hz
- Calendar output functions: Year, month, day, weekday, hour, minute and second
- Clock counter, alarm and fixed-cycle timer interrupt functions

Programming information for the RTC-8564JE is available in the RTC-8564JE/NB Application Manual at the Epson Electronics America website [Ref 23].

Figure 1-17 shows the real-time clock circuit.

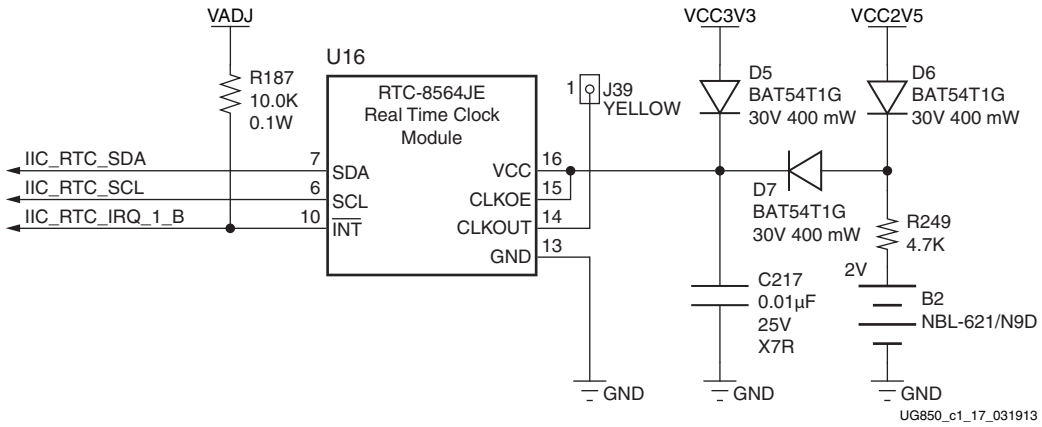


Figure 1-17: **Real Time Clock Circuit**

Real-time clock connections to the XC7Z020 AP SoC and the PCA9548 8-Channel bus switch are listed in Table 1-20.

Table 1-20: **Real Time Clock Connections**

RTC-8564JE (U16) Pin	Net Name	Connects To
6	IIC_RTC_SCL	U44.11 (PCA9548 SC4)
7	IIC_RTC_SDA	U44.10 (PCA9548 SD4)
10	IIC_RTC_IRQ_1_B(1)	U1.U7 (XC7Z020 AP SoC PL BANK 13)

Notes:

1. I/O standard = LVCMOS_25.

Information about the RTC-8564JE is available at the Epson Electronics America website [Ref 23].

I/O Expansion Header

[Figure 1-2, callout 16]

The 2 x 6 I/O expansion header J54 supports Digilent Pmod Peripheral Modules. 8 pins (IIC_PMOD[0:7]) are connected to the TI TCA6416APWR I2C expansion port device U80. See the Digilent website for information on Digilent Pmod Peripheral Modules [Ref 24].

The expansion header circuit is shown in Figure 1-18.

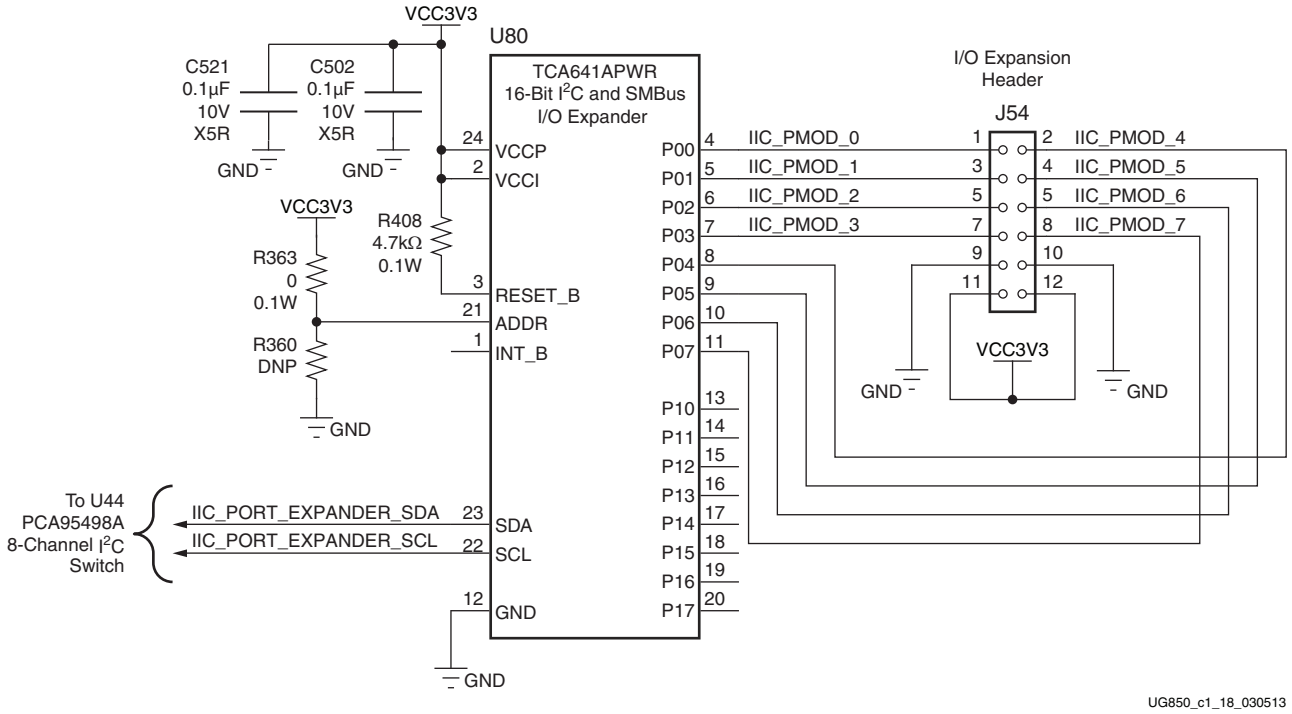


Figure 1-18: **I/O Expansion Header Circuit**

Information about the TCA641APWR is available at the Texas Instruments website [Ref 26].

High Speed CAN Transceiver

[Figure 1-2, callout 21]

The TJA1040 (U14) is an advanced high speed Controller Area Network (CAN) transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation described in the international standard for in-vehicle high speed CAN applications (ISO 11898).

Figure 1-19 shows the controller area network (CAN) bus interface.

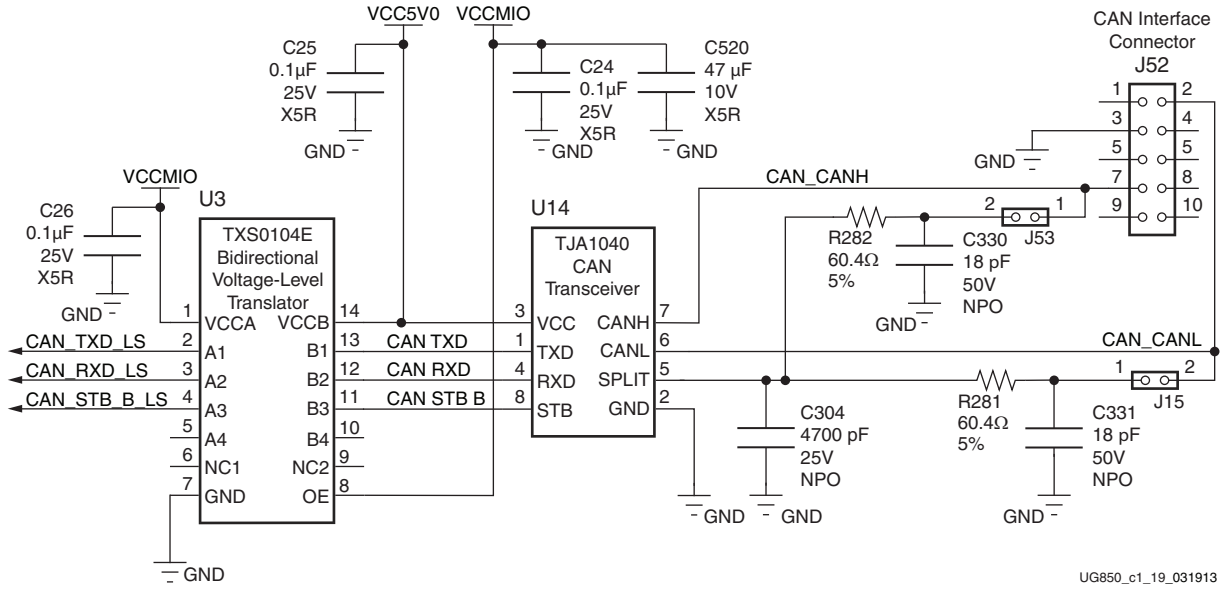


Figure 1-19: **CAN Bus Interface**

Information about the TXS0104E is available at the Texas Instruments website [Ref 26]. Data sheets and application notes for the TJA01040 CAN transceiver are available at the NXP Semiconductors website [Ref 25]. Table 1-21 shows the U14 CAN transceiver to U1 XC7Z020 interface connections through level shifter U3.

Table 1-21: **CAN Transceiver AP SoC Connections**

TJA1040 (U14)		TXS0104E Level Shifter (U3)	XC7Z020 AP SoC (U1)		
Pin	Net Name	Net Name	Low Side Net	Bank	Pin
1	CAN_TXD	CAN_TXD_LS	PS_MIO47	501	B10
4	CAN_RXD	CAN_RXD_LS	PS_MIO46	501	D12
8	CAN_STB_B	CAN_STB_B_LS	PS_MIO9	500	C4

Status LEDs

[Figure 1-2, callout 21]

Table 1-22 defines the status LEDs. For user controlled LEDs see User I/O, page 43.

Table 1-22: **Status LEDs**

Reference Designator	Net Name	LED Color	Description
DS1	POR	Red	Power on reset is active
DS2	FPGA_INIT_B	Green/Red	Green: FPGA initialization was successful
			Red: FPGA initialization is in progress
DS3	DONE	Green	FPGA bit file download is complete
DS4	PWRCTL_VCC1B_FLKT_LINEAR_PG	Green	DDR3 V_{TT} OK
DS5	U13_FLG	Red	USB Power Error
DS6	PHY_LED2	Green	Ethernet PHY (U35) User LED2
DS7	PHY_LED1	Green	Ethernet PHY (U35) User LED1
DS8	PHY_LED0	Green	Ethernet PHY (U35) User LED0
DS14	VCC12_P_IN	Green	$12V_{DC}$ Power ON
DS13	PWRCTL_PWRGOOD	Green	UCD9248 Power Controllers U32, U33, U34 Power Good (board supply voltages $\geq$ minimum operating voltage)
DS24	PWRCTL1_VCC4A_PG	Green	FMC1, FMC2 Power Good

Ethernet PHY User LEDs

[Figure 1-2, callout 11]

The three Ethernet PHY user LEDs shown in Figure 1-20 are located near the RJ45 Ethernet jack P2. The on/off state for each LED is software dependent and has no specific meaning at Ethernet PHY power on.

Refer to the Marvell 88E1116R Alaska Gigabit Ethernet transceiver data sheet for details concerning the use of the Ethernet PHY user LEDs. They are referred in the data sheet as LED0, LED1, and LED2. The data sheet and other product information for the Marvell 88E1116R Alaska Gigabit Ethernet Transceiver is available at the Marvell website [Ref 21].

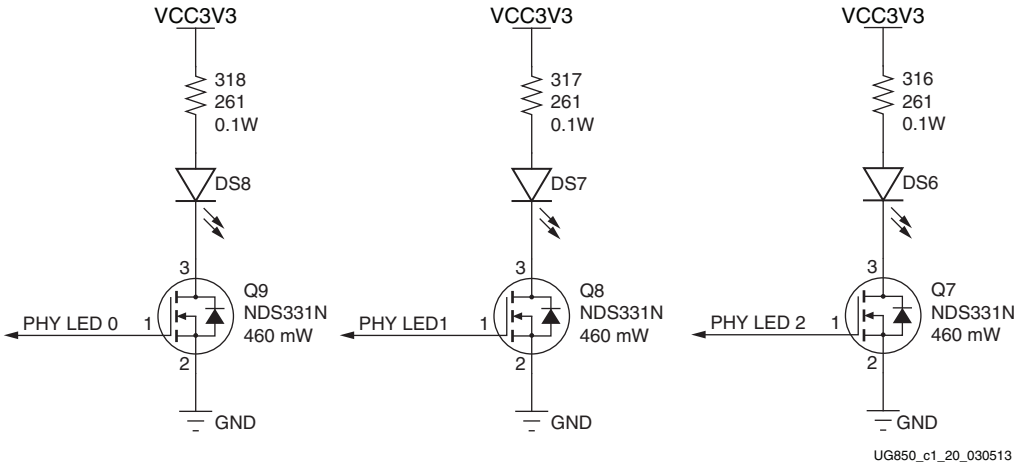


Figure 1-20: **Ethernet PHY User LEDs**

User I/O

[Figure 1-2, callout 17–28]

The ZC702 board provides the following user and general purpose I/O capabilities:

- Ten user LEDs (callout 17)
  - PMOD0 0–PMOD0 3 and PMOD1 0–PMOD1 3: DS15–DS22
  - PS_LED1: DS23 and PS_MIO8_LED0: DS12
- Two user pushbuttons and reset switch (callout 18)
  - GPIO_SW_N and GPIO_SW_S: SW5 and SW7
- 2-position user DIP switch (callout 24)
  - GPIO_DIP_SW1 and GPIO_DIP_SW0: SW12
- User PS switches (near callout 18)

  - Pushbutton SW13 wired in parallel to DIP switch SW15 switch 1
  - Pushbutton SW14 wired in parallel to DIP switch SW15 switch 2
- PS Power-On and System Reset pushbuttons (Switches, page 49)
  - SW1 (PS_POR_B)
  - SW2 (PS_SRST_B)
- Two user GPIO male pin headers (callout 28)
- 2 x 6 0.1 inch pitch PMOD1 J63
- 1 x 6 0.1 inch pitch PMOD2 J62

User LEDs

[Figure 1-2, callout 17]

The ZC702 board supports eight user LEDs connected to XC7Z020 AP SoC Banks 13, 33, 34, and 35 through level-shifters. Note that the LEDs are wired in parallel with headers J63 (PMOD1) and J62 (PMOD2). These headers are described in User PMOD GPIO Headers, page 48.

Figure 1-21 shows the user LED circuits.

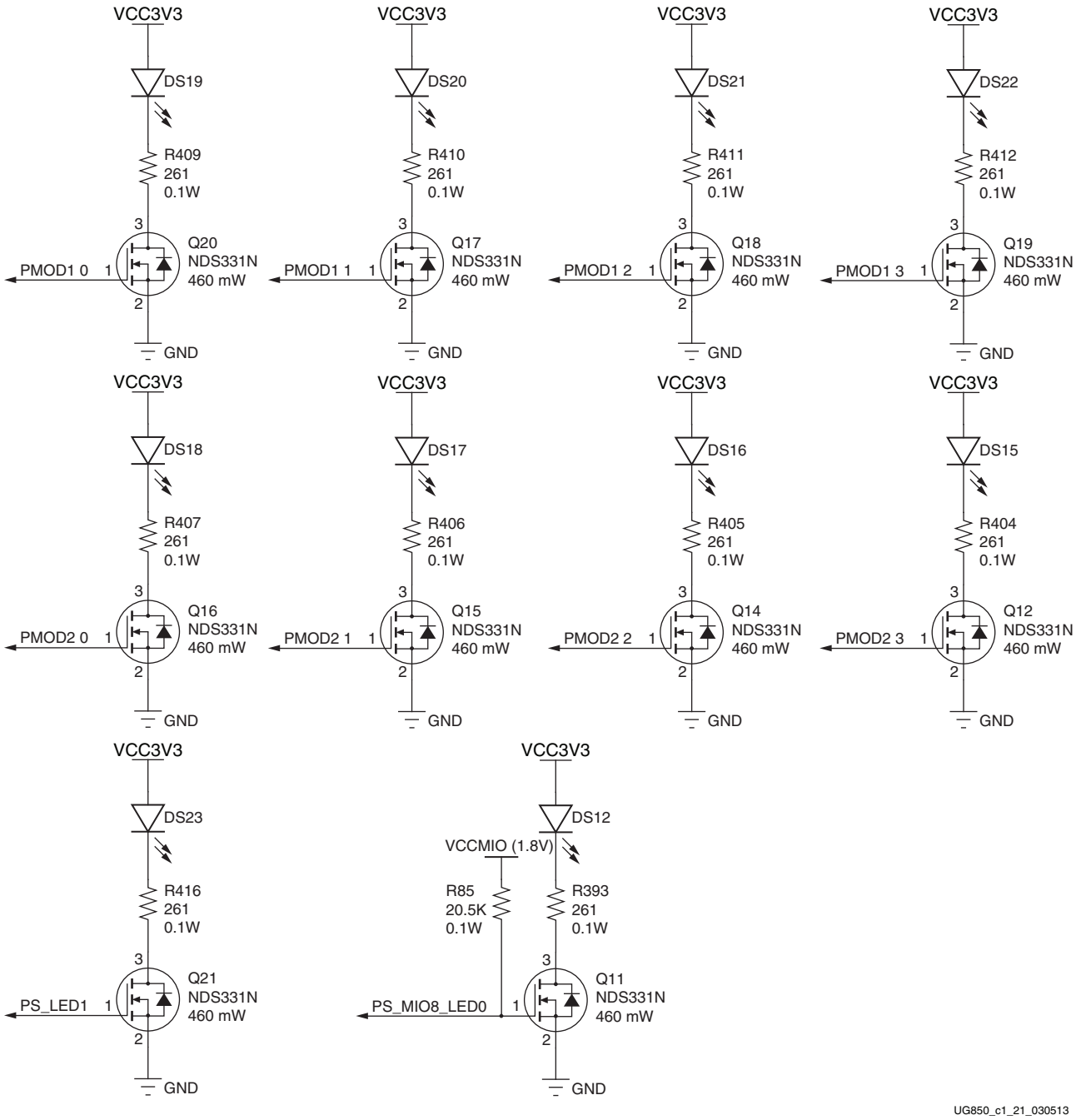


Figure 1-21: **User LEDs**

Table 1-23 lists the user LED connections to XC7Z020 AP SoC U1.

Table 1-23: **User LED Connections to XC7Z020 AP SoC U1**

XC7Z020 (U1) Pin	Net Name	I/O Standard	LED Reference Designator
E15	PMOD1_0	LVCMOS25	DS19
D15	PMOD1_1	LVCMOS25	DS20
W17	PMOD1_2	LVCMOS25	DS21
W5	PMOD1_3	LVCMOS25	DS22
V7	PMOD2_0	LVCMOS25	DS18
W10	PMOD2_1	LVCMOS25	DS17
P18	PMOD2_2	LVCMOS25	DS16
P17	PMOD2_3	LVCMOS25	DS15
Bank 501 G7	PS_LED1	N/A	DS23
Bank 500 E5	PS_MIO8_LED0	N/A	DS12

User Pushbuttons

[Figure 1-2, callout 18]

Figure 1-22 shows the user pushbutton circuits.

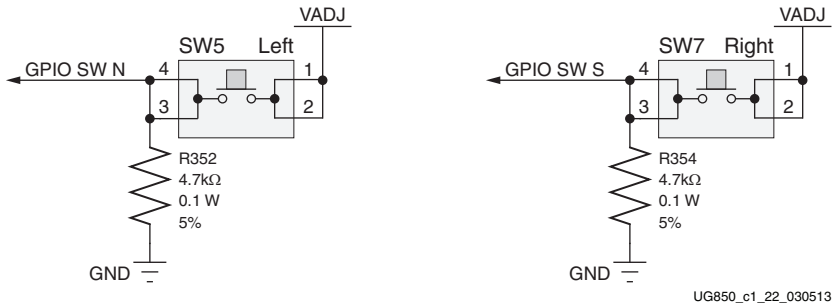


Figure 1-22: **User Pushbuttons**

Table 1-24 lists the user pushbutton connections to XC7Z020 AP SoC U1.

Table 1-24: **User Pushbutton Connections to XC7Z020 AP SoC U1**

XC7Z020 AP SoC (U1) Pin	Net Name	I/O Standard	Pushbutton and Pin Reference
G19	GPIO_SW_N	LVCMOS25	SW5.3 (Left switch)
F19	GPIO_SW_S	LVCMOS25	SW7.3 (Right switch)

GPIO DIP Switch

[Figure 1-2, callout 19]

Figure 1-23 shows the GPIO DIP switch circuit.

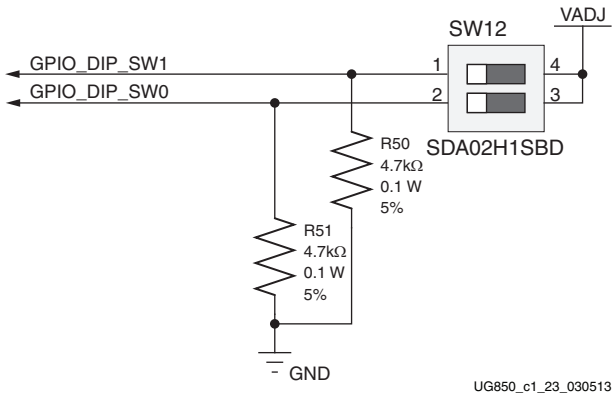


Figure 1-23: **GPIO DIP Switch**

Table 1-25 lists the GPIO DIP switch connections to XC7Z020 AP SoC U1.

Table 1-25: **GPIO DIP Switch Connections to XC7Z020 AP SoC at U1**

XC7Z020 (U1) Pin	Net Name	I/O Standard	DIP Switch SW12 Pin
W6	GPIO_DIP_SW0	LVCMOS25	2
W7	GPIO_DIP_SW1	LVCMOS25	1

User PS Switches

[Figure 1-2, near callout 18]

Figure 1-25 shows the user PS pushbutton and DIP switch circuit.

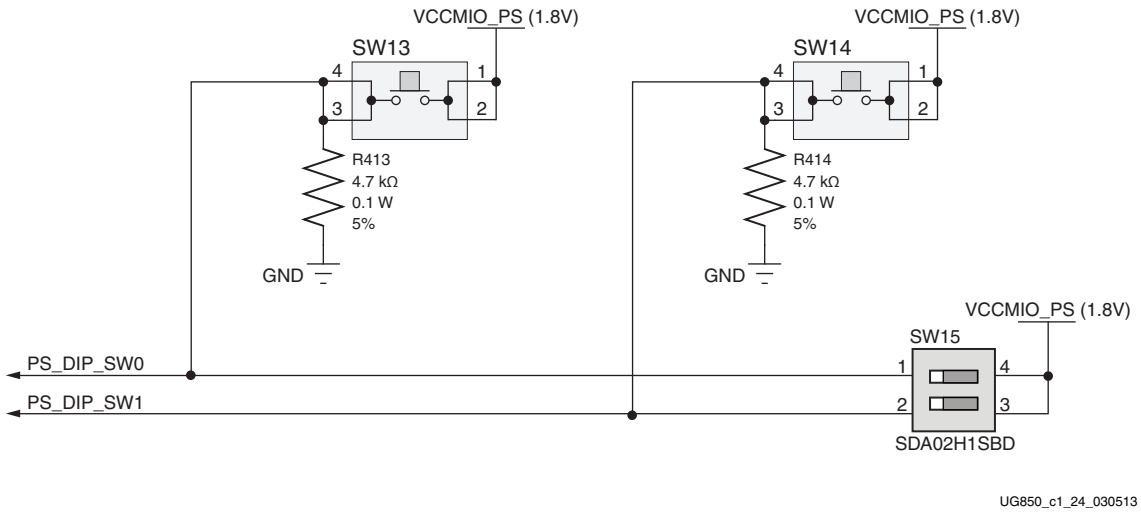


Figure 1-24: **User PS Pushbutton and DIP Switch Circuit**

Table 1-26 lists the user PS-side pushbutton and DIP switch connections to XC7Z020 AP SoC U1 Bank 500.

Table 1-26: **User PS Switch Connections to XC7Z020 AP SoC U1**

XC7Z020 AP SoC (U1) Pin	Net Name	Switch and Pin Reference
B6	PS_DIP_SW0	SW13.4 and SW15.1
C5	PS_DIP_SW1	SW14.4 and SW15.2

User PMOD GPIO Headers

[Figure 1-2, callout 28]

The ZC702 board supports two GPIO headers J62 and J63. The PMOD nets connected to these headers are dual-purpose, with the User LEDs, page 44 wired in parallel to the header pins.

J63 has a second dual-purpose function. The even numbered pins are wired in parallel to the ARM PJTAG header J41 pins TDI, TIMS, TCK, and TDO. The J41 PJTAG signals are connected to AP SoC Bank 13 GPIO pins which simultaneously drive J41 and J63. When J41 is used for ARM PJTAG functionality, the J63 even numbered pin should not be used. When J63 even numbered pins are used as GPIO, connector J41 should not be used.

Figure 1-25 shows the user GPIO male pin header circuits.

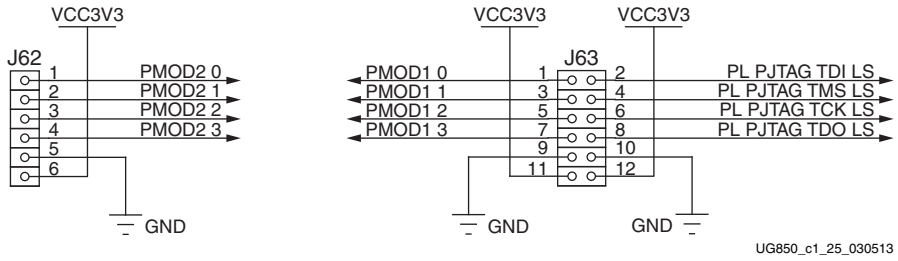


Figure 1-25: **User GPIO Headers**

Table 1-27 lists the GPIO Header connections to XC7Z020 AP SoC U1.

Table 1-27: **GPIO Header Connections to XC7Z020 AP SoC at U1**

XC7Z020 (U1) Pin	Net Name	I/O Standard	GPIO Header and Pin
E15	PMOD1_0	LVCMOS25	J63.1
D15	PMOD1_1	LVCMOS25	J63.3
W17	PMOD1_2	LVCMOS25	J63.5
W5	PMOD1_3	LVCMOS25	J63.7
V7	PMOD2_0	LVCMOS25	J62.1
W10	PMOD2_1	LVCMOS25	J62.2
P18	PMOD2_2	LVCMOS25	J62.3
P17	PMOD2_3	LVCMOS25	J62.4

Refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 9] for information about the PS PJTAG functionality.

Switches

[Figure 1-2, callout 22–26]

The ZC702 board includes a power and a configuration switch:

- Power On/Off slide switch SW11 (callout 26)
- SW4 (FPGA_PROG_B), active-Low pushbutton (callout 22)

Power On/Off Slide Switch

[Figure 1-2, callout 20]

The ZC702 board power switch is SW11. Sliding the switch actuator from the Off to On position applies 12V power from J60, a 6-pin mini-fit connector. Green LED DS14 illuminates when the ZC702 board power is on. See Power Management for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J60 on the ZC702 board. The ATX 6-pin connector has a different pinout than J60. Connecting an ATX 6-pin connector into J60 damages the ZC702 board and voids the board warranty.*

Figure 1-26 shows the power connector J60, power switch SW11 and indicator LED DS14.

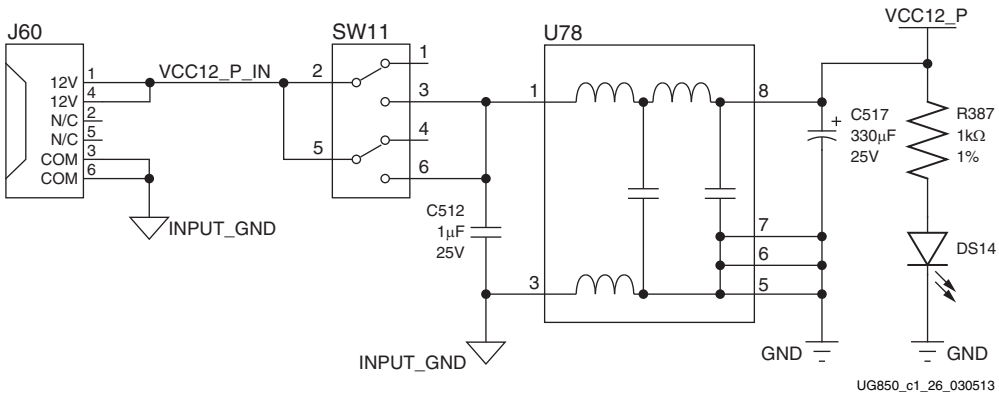


Figure 1-26: **Power On/Off Switch SW11**

Program_B Pushbutton

[Figure 1-2, callout 22]

Switch SW4 grounds the XC7Z020 AP SoC PROG_B pin when pressed. This action clears programmable logic configuration, which the PS software can then act on. The FPGA_PROG_B signal is connected to XC7Z020 AP SoC U1 pin T11.

See the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 4] for further details on configuring the 7 series FPGAs.

Figure 1-27 shows SW4.

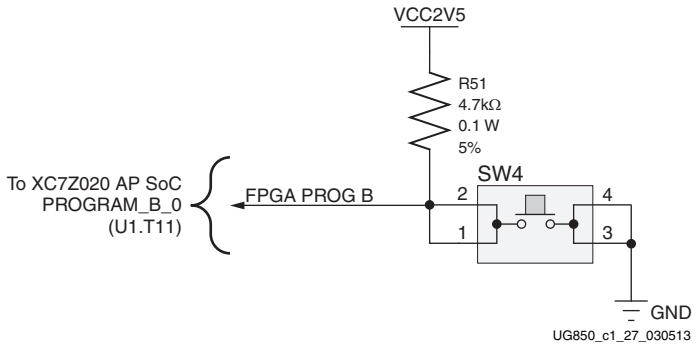


Figure 1-27: **PROG_B Pushbutton SW4**

PS Power-On and System Reset Pushbuttons

[Figure 1-2, callout 27]

Figure 1-28 shows the reset circuitry for the processing system.

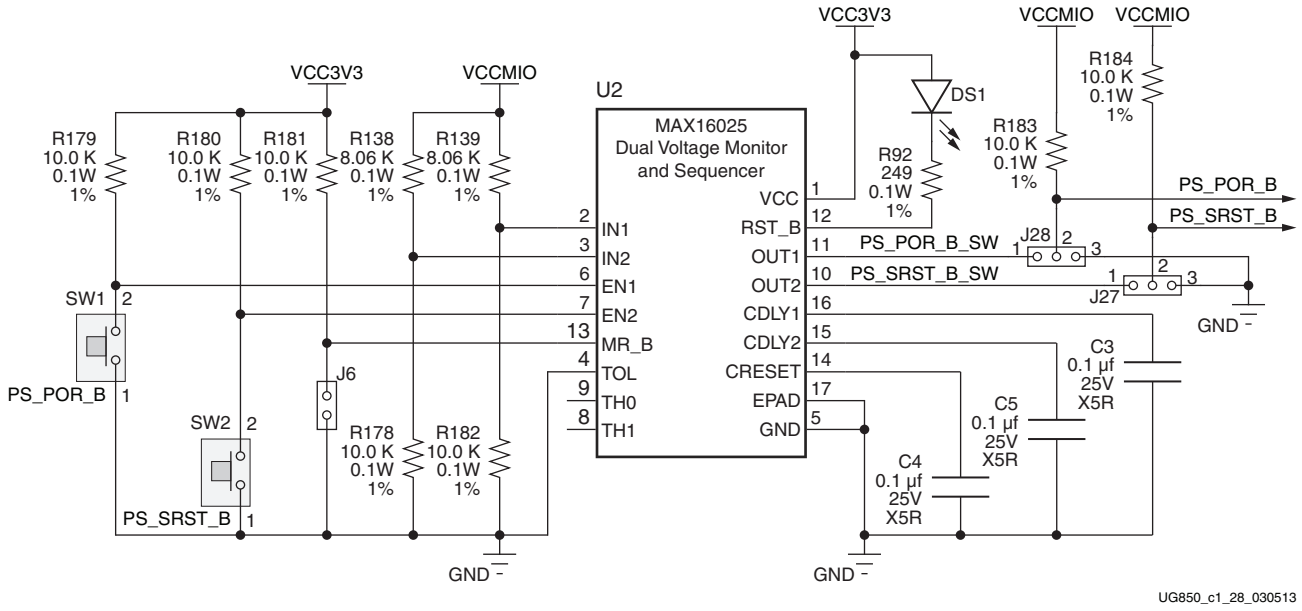


Figure 1-28: **PS Power On and System Reset Circuitry**

Depressing and then releasing pushbutton SW1 causes PS_POR_B_SW to strobe Low.

PS_POR_B: This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply *power-good* signal.

Depressing and then releasing pushbutton SW2 causes PS_SRST_B_SW to strobe Low.

PS_SRST_B: This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps.

Refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual (UG585)* [Ref 9] for information concerning the resets.

FPGA Mezzanine (FMC) Card Interface

[Figure 1-2, callout 24]

The ZC702 board supports the VITA 57.1 FPGA Mezzanine Card (FMC) specification by providing subset implementations of low pin count (LPC) connectors at J3 and J4. Both connectors use a 10 x 40 form factor that is partially populated with 160 pins. The connectors are keyed so that a the mezzanine card faces away from the ZC702 board when connected.

Connector Type:

- Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector.

For more information about SEAF series connectors, go to the Samtec website [Ref 29].

LPC Connectors J3 and J4

[Figure 1-2, callout 24]

The 160-pin LPC connector defined by the FMC specification (Figure B-1, page 67) provides connectivity for up to:

- 68 single-ended or 34 differential user-defined signals (34 LA pairs, LA00–LA33)
- 1 GTX transceiver
- 1 GTX clock
- 2 differential clocks
- 61 ground and 10 power connections

The LPC connections between FMC1 (J3) and XC7Z020 AP SoC U1 (Table 1-28) and between FMC2 (J4) and XC7Z020 AP SoC U1 (Table 1-29) both implement a subset of this connectivity:

- 68 single-ended or 34 differential user-defined signals (34 LA pairs, LA00–LA33)
- 0 GTX transceivers
- 0 GTX clocks
- 2 differential clocks
- 61 ground and 9 power connections

Note: FMC1 (J3) and FMC2 (J4) GA0 = GA1 = 0 (GND).

Table 1-28 shows the LPC connections between J3 and XC7Z020 AP SoC U1.

Table 1-28: **LPC Connections, FMC1 (J3) to XC7Z020 AP SoC U1**

FMC1 J3 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin	FMC1 J3 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
C2	NC			D1	PWRCTL2_VCC4A_PG		
C3	NC			D4	NC		
C6	NC			D5	NC		
C7	NC			D8	FMC1_LPC_LA01_CC_P	LVCMOS25	N19
C10	FMC1_LPC_LA06_P	LVCMOS25	J18	D9	FMC1_LPC_LA01_CC_N	LVCMOS25	N20
C11	FMC1_LPC_LA06_N	LVCMOS25	K18	D11	FMC1_LPC_LA05_P	LVCMOS25	N17
C14	FMC1_LPC_LA10_P	LVCMOS25	L17	D12	FMC1_LPC_LA05_N	LVCMOS25	N18
C15	FMC1_LPC_LA10_N	LVCMOS25	M17	D14	FMC1_LPC_LA09_P	LVCMOS25	M15
C18	FMC1_LPC_LA14_P	LVCMOS25	J16	D15	FMC1_LPC_LA09_N	LVCMOS25	M16
C19	FMC1_LPC_LA14_N	LVCMOS25	J17	D17	FMC1_LPC_LA13_P	LVCMOS25	P16
C22	FMC1_LPC_LA18_CC_P	LVCMOS25	D20	D18	FMC1_LPC_LA13_N	LVCMOS25	R16
C23	FMC1_LPC_LA18_CC_N	LVCMOS25	C20	D20	FMC1_LPC_LA17_CC_P	LVCMOS25	B19
C26	FMC1_LPC_LA27_P	LVCMOS25	C17	D21	FMC1_LPC_LA17_CC_N	LVCMOS25	B20
C27	FMC1_LPC_LA27_N	LVCMOS25	C18	D23	FMC1_LPC_LA23_P	LVCMOS25	G15
C30	FMC1_LPC_IIC_SCL			D24	FMC1_LPC_LA23_N	LVCMOS25	G16
C31	FMC1_LPC_IIC_SDA			D26	FMC1_LPC_LA26_P	LVCMOS25	F18
C34	GA0 = 0 = GND			D27	FMC1_LPC_LA26_N	LVCMOS25	E18
C35	VCC12_P			D29	FMC1_LPC_TCK_BUF		
C37	VCC12_P			D30	FMC_TDI_BUF		
C39	VCC3V3			D31	FMC1_LPC_TDO_FMC2_LPC_TDI		
				D32	VCC3V3		
				D33	FMC1_LPC_TMS_BUF		
				D34	NC		
				D35	GA0 = 0 = GND		
				D36	VCC3V3		
				D38	VCC3V3		
				D40	VCC3V3		
G2	FMC1_LPC_CLK1_M2C_P	LVCMOS25	M19	H1	NC		
G3	FMC1_LPC_CLK1_M2C_N	LVCMOS25	M20	H2	FMC1_LPC_PRSNT_M2C_B		

Table 1-28: **LPC Connections, FMC1 (J3) to XC7Z020 AP SoC U1 *(Cont'd)***

FMC1 J3 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin	FMC1 J3 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
G6	FMC1_LPC_LA00_CC_P	LVCMOS25	K19	H4	FMC1_LPC_CLK0_M2C_P	LVCMOS25	L18
G7	FMC1_LPC_LA00_CC_N	LVCMOS25	K20	H5	FMC1_LPC_CLK0_M2C_N	LVCMOS25	L19
G9	FMC1_LPC_LA03_P	LVCMOS25	J20	H7	FMC1_LPC_LA02_P	LVCMOS25	L21
G10	FMC1_LPC_LA03_N	LVCMOS25	K21	H8	FMC1_LPC_LA02_N	LVCMOS25	L22
G12	FMC1_LPC_LA08_P	LVCMOS25	J21	H10	FMC1_LPC_LA04_P	LVCMOS25	M21
G13	FMC1_LPC_LA08_N	LVCMOS25	J22	H11	FMC1_LPC_LA04_N	LVCMOS25	M22
G15	FMC1_LPC_LA12_P	LVCMOS25	N22	H13	FMC1_LPC_LA07_P	LVCMOS25	J15
G16	FMC1_LPC_LA12_N	LVCMOS25	P22	H14	FMC1_LPC_LA07_N	LVCMOS25	K15
G18	FMC1_LPC_LA16_P	LVCMOS25	N15	H16	FMC1_LPC_LA11_P	LVCMOS25	R20
G19	FMC1_LPC_LA16_N	LVCMOS25	P15	H17	FMC1_LPC_LA11_N	LVCMOS25	R21
G21	FMC1_LPC_LA20_P	LVCMOS25	G20	H19	FMC1_LPC_LA15_P	LVCMOS25	P20
G22	FMC1_LPC_LA20_N	LVCMOS25	G21	H20	FMC1_LPC_LA15_N	LVCMOS25	P21
G24	FMC1_LPC_LA22_P	LVCMOS25	G17	H22	FMC1_LPC_LA19_P	LVCMOS25	E19
G25	FMC1_LPC_LA22_N	LVCMOS25	F17	H23	FMC1_LPC_LA19_N	LVCMOS25	E20
G27	FMC1_LPC_LA25_P	LVCMOS25	C15	H25	FMC1_LPC_LA21_P	LVCMOS25	F21
G28	FMC1_LPC_LA25_N	LVCMOS25	B15	H26	FMC1_LPC_LA21_N	LVCMOS25	F22
G30	FMC1_LPC_LA29_P	LVCMOS25	B16	H28	FMC1_LPC_LA24_P	LVCMOS25	A21
G31	FMC1_LPC_LA29_N	LVCMOS25	B17	H29	FMC1_LPC_LA24_N	LVCMOS25	A22
G33	FMC1_LPC_LA31_P	LVCMOS25	A16	H31	FMC1_LPC_LA28_P	LVCMOS25	D22
G34	FMC1_LPC_LA31_N	LVCMOS25	A17	H32	FMC1_LPC_LA28_N	LVCMOS25	C22
G36	FMC1_LPC_LA33_P	LVCMOS25	A18	H34	FMC1_LPC_LA30_P	LVCMOS25	E21
G37	FMC1_LPC_LA33_N	LVCMOS25	A19	H35	FMC1_LPC_LA30_N	LVCMOS25	D21
G39	VADJ			H37	FMC1_LPC_LA32_P	LVCMOS25	B21
				H38	FMC1_LPC_LA32_N	LVCMOS25	B22
				H40	VADJ		

Table 1-29 shows the LPC connections between FMC2 (J4) and AP SoC U1.

Table 1-29: **LPC Connections, FMC2 (J4) to AP SoC U1**

FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin	FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
C2	NC			D1	PWRCTL2_VCC4A_PG		
C3	NC			D4	NC		
C6	NC			D5	NC		
C7	NC			D8	FMC2_LPC_LA01_CC_P	LVCMOS25	W16

Table 1-29: **LPC Connections, FMC2 (J4) to AP SoC U1 *(Cont'd)***

FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin	FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
C10	FMC2_LPC_LA06_P	LVCMOS25	U17	D9	FMC2_LPC_LA01_CC_N	LVCMOS25	Y16
C11	FMC2_LPC_LA06_N	LVCMOS25	V17	D11	FMC2_LPC_LA05_P	LVCMOS25	AB19
C14	FMC2_LPC_LA10_P	LVCMOS25	Y20	D12	FMC2_LPC_LA05_N	LVCMOS25	AB20
C15	FMC2_LPC_LA10_N	LVCMOS25	Y21	D14	FMC2_LPC_LA09_P	LVCMOS25	U15
C18	FMC2_LPC_LA14_P	LVCMOS25	T22	D15	FMC2_LPC_LA09_N	LVCMOS25	U16
C19	FMC2_LPC_LA14_N	LVCMOS25	U22	D17	FMC2_LPC_LA13_P	LVCMOS25	V22
C22	FMC2_LPC_LA18_CC_P	LVCMOS25	AA9	D18	FMC2_LPC_LA13_N	LVCMOS25	W22
C23	FMC2_LPC_LA18_CC_N	LVCMOS25	AA8	D20	FMC2_LPC_LA17_CC_P	LVCMOS25	AA7
C26	FMC2_LPC_LA27_P	LVCMOS25	AB2	D21	FMC2_LPC_LA17_CC_N	LVCMOS25	AA6
C27	FMC2_LPC_LA27_N	LVCMOS25	AB1	D23	FMC2_LPC_LA23_P	LVCMOS25	V12
C30	FMC2_LPC_IIC_SCL			D24	FMC2_LPC_LA23_N	LVCMOS25	W12
C31	FMC2_LPC_IIC_SDA			D26	FMC2_LPC_LA26_P	LVCMOS25	U12
C34	GA0 = 0 = GND			D27	FMC2_LPC_LA26_N	LVCMOS25	U11
C35	VCC12_P			D29	FMC2_LPC_TCK_BUF		
C37	VCC12_P			D30	FMC1_LPC_TDO_FMC2_LPC_TDI		
C39	VCC3V3			D31	FMC2_LPC_TDO_FPGA_TDI		
				D32	VCC3V3		
				D33	FMC2_LPC_TMS_BUF		
				D34	NC		
				D35	GA0 = 0 = GND		
				D36	VCC3V3		
				D38	VCC3V3		
				D40	VCC3V3		
G2	FMC2_LPC_CLK1_M2C_P	LVCMOS25	Y6	H1	NC		
G3	FMC2_LPC_CLK1_M2C_N	LVCMOS25	Y5	H2	FMC2_LPC_PRSNT_M2C_B		
G6	FMC2_LPC_LA00_CC_P	LVCMOS25	Y19	H4	FMC2_LPC_CLK0_M2C_P	LVCMOS25	Y18
G7	FMC2_LPC_LA00_CC_N	LVCMOS25	AA19	H5	FMC2_LPC_CLK0_M2C_N	LVCMOS25	AA18
G9	FMC2_LPC_LA03_P	LVCMOS25	AA16	H7	FMC2_LPC_LA02_P	LVCMOS25	V14
G10	FMC2_LPC_LA03_N	LVCMOS25	AB16	H8	FMC2_LPC_LA02_N	LVCMOS25	V15

Table 1-29: **LPC Connections, FMC2 (J4) to AP SoC U1 *(Cont'd)***

FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin	FMC2 J4 Pin	Net Name	I/O Standard	XC7Z020 (U1) Pin
G12	FMC2_LPC_LA08_P	LVCMOS25	AA17	H10	FMC2_LPC_LA04_P	LVCMOS25	V13
G13	FMC2_LPC_LA08_N	LVCMOS25	AB17	H11	FMC2_LPC_LA04_N	LVCMOS25	W13
G15	FMC2_LPC_LA12_P	LVCMOS25	W15	H13	FMC2_LPC_LA07_P	LVCMOS25	T21
G16	FMC2_LPC_LA12_N	LVCMOS25	Y15	H14	FMC2_LPC_LA07_N	LVCMOS25	U21
G18	FMC2_LPC_LA16_P	LVCMOS25	AB14	H16	FMC2_LPC_LA11_P	LVCMOS25	Y14
G19	FMC2_LPC_LA16_N	LVCMOS25	AB15	H17	FMC2_LPC_LA11_N	LVCMOS25	AA14
G21	FMC2_LPC_LA20_P	LVCMOS25	T4	H19	FMC2_LPC_LA15_P	LVCMOS25	Y13
G22	FMC2_LPC_LA20_N	LVCMOS25	U4	H20	FMC2_LPC_LA15_N	LVCMOS25	AA13
G24	FMC2_LPC_LA22_P	LVCMOS25	U10	H22	FMC2_LPC_LA19_P	LVCMOS25	R6
G25	FMC2_LPC_LA22_N	LVCMOS25	U9	H23	FMC2_LPC_LA19_N	LVCMOS25	T6
G27	FMC2_LPC_LA25_P	LVCMOS25	AA12	H25	FMC2_LPC_LA21_P	LVCMOS25	V5
G28	FMC2_LPC_LA25_N	LVCMOS25	AB12	H26	FMC2_LPC_LA21_N	LVCMOS25	V4
G30	FMC2_LPC_LA29_P	LVCMOS25	AA11	H28	FMC2_LPC_LA24_P	LVCMOS25	U6
G31	FMC2_LPC_LA29_N	LVCMOS25	AB11	H29	FMC2_LPC_LA24_N	LVCMOS25	U5
G33	FMC2_LPC_LA31_P	LVCMOS25	AB10	H31	FMC2_LPC_LA28_P	LVCMOS25	AB5
G34	FMC2_LPC_LA31_N	LVCMOS25	AB9	H32	FMC2_LPC_LA28_N	LVCMOS25	AB4
G36	FMC2_LPC_LA33_P	LVCMOS25	Y11	H34	FMC2_LPC_LA30_P	LVCMOS25	AB7
G37	FMC2_LPC_LA33_N	LVCMOS25	Y10	H35	FMC2_LPC_LA30_N	LVCMOS25	AB6
G39	VADJ			H37	FMC2_LPC_LA32_P	LVCMOS25	Y4
				H38	FMC2_LPC_LA32_N	LVCMOS25	AA4
				H40	VADJ		

Power Management

[Figure 1-2, callout 25]

TheZC702 PCB layout and power system design meets the recommended criteria described in the *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933) [Ref 14].

The ZC702 board power distribution diagram is shown in Figure 1-29.

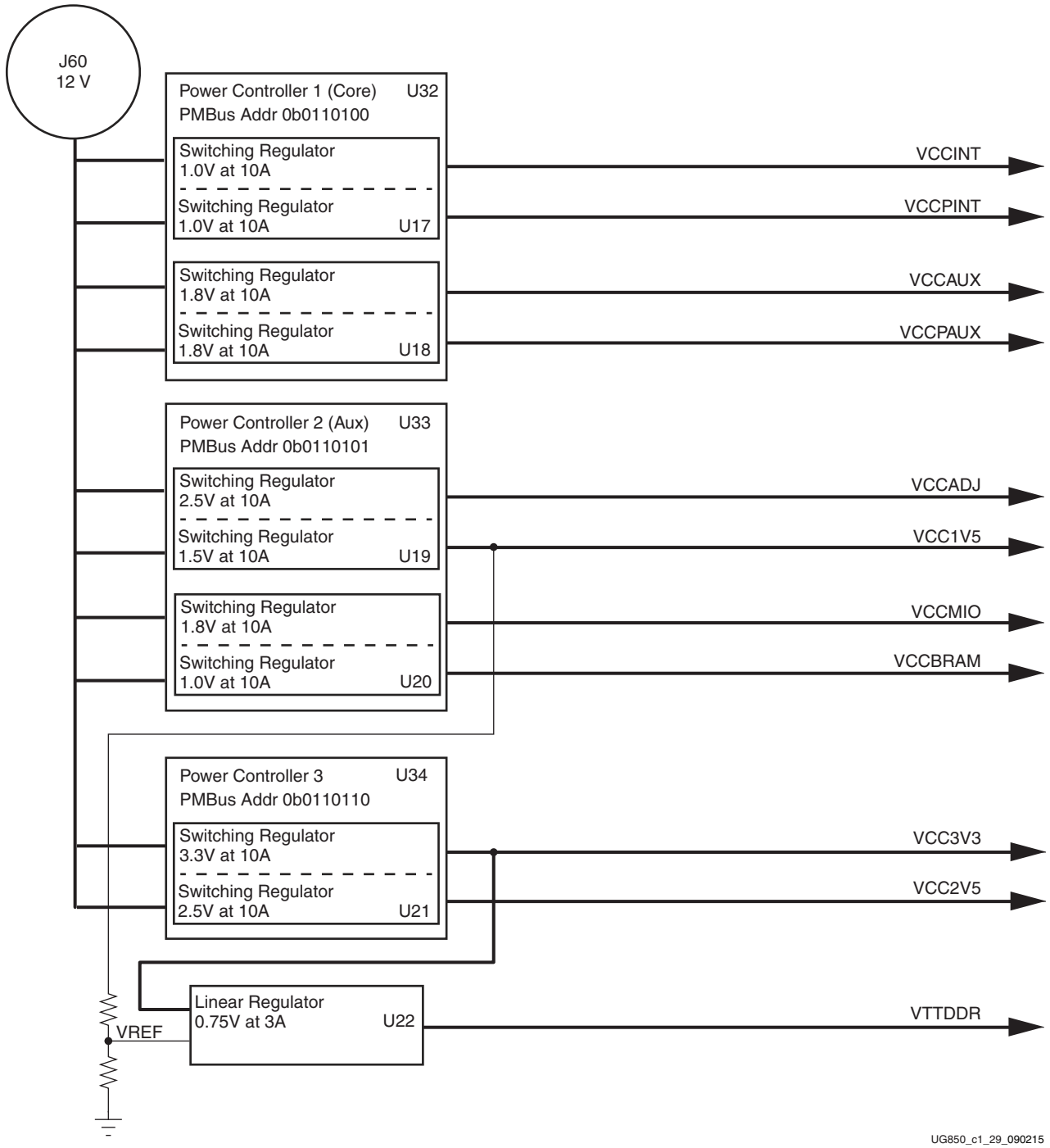


Figure 1-29: **Onboard Power Regulators**

The ZC702 board uses power regulators and a PMBus compliant system controller from Texas Instruments to supply core and auxiliary voltages as listed in Table 1-30. The Texas Instruments Fusion Digital Power graphical user interface is used to monitor the voltage and current levels of the board power modules.

Table 1-30: **Onboard Power System Devices**

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
Core voltage controller and regulators					
UCD9248PFC	U32	PMBus Controller–Core Addr = 52 dec., 0b0110100)			39
PTD08D210W—VoutA	U17	Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCINT	1.00V	40
PTD08D210W—VoutB		Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCPINT	1.00V	40
PTD08D210W—VoutA	U18	Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCAUX	1.80V	41
PTD08D210W—VoutB		Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCPAUX	1.80V	41
Auxiliary voltage controller and regulators					
UCD9248PFC	U33	PMBus Controller–Aux Addr = 53 dec., 0b0110101)			42
PTD08D210W—VoutA	U19	Dual 10A 0.6V–3.6V Adj. Switching Regulator (set to 1.8V, 2.5V or 3.3V)	VADJ	2.50V	43
PTD08D210W—VoutB		Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCC1V5	1.50V	43
PTD08D210W—VoutA	U20	Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCMIO_PS	1.80V	44
PTD08D210W—VoutB		Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCCBRAM	1.00V	44
UCD9248PFC	U34	PMBus Controller–Aux Addr = 54 dec., 0b0110110)			45
PTD08D210W—VoutA	U21	Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCC3V3	3.30V	46
PTD08D210W—VoutB		Dual 10A 0.6V–3.6V Adj. Switching Regulator	VCC2V5/ VCC2V5_PL	2.50V	46
Linear regulator					
TPS51200DR	U22	3A Tracking Regulator	VTTDDR_PS	0.75V	37

VADJ Voltage Control

The VADJ rail is set to 2.5V. When the ZC702 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J12 is sampled by the TI UCD9248 controller U33.

If a jumper is installed on J12 signal FMC_VADJ_ON_B is held Low, and the TI controller U33 energizes the VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J12 jumper, removing the jumper at J12 after the board is powered up does not affect the 2.5V power delivered to the VADJ rail and it remains on.

A jumper installed at J12 is the default setting.

If a jumper is not installed on J12, signal FMC_VADJ_ON_B is High, and the ZC702 board does not energize the VADJ 2.5V at power on. In this mode you can control when to turn on VADJ and to what voltage level (1.8V, 2.5V or 3.3V only). With VADJ off, the XC7Z020 AP SoC still configures and has access to the TI controller PMBUS along with the FMC_VADJ_ON_B signal. The combination of these allows the user to develop code to command the VADJ rail to be set to something other than the default setting of 2.5V. After the new VADJ voltage level has been programmed into TI controller U33, the FMC_VADJ_ON_B signal can be driven Low by the user logic and the VADJ rail comes up at the new VADJ voltage level. Installing a jumper at J12 after a ZC702 board powers up in this mode turns on the VADJ rail.

The FMC_VADJ_ON_B signal is sourced by the TCA6416APWR I2C port expander U80 pin 13 (see Figure 1-18, page 40).

The I2C port expander IIC_PORT_EXPANDER SDA/SCL bus is wired to the PCA9548ARGER I2C bus switch (see I2C Bus, page 37).

Documentation describing PMBUS programming for the UCD9248 digital power controller is available at TI [Ref 26].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U32 at address 52 decimal, U33 at address 53 decimal, and U34 at address 54 decimal) are wired to the same PMBus. The PMBus connector, J59, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO, which can be ordered from the Texas Instruments website [Ref 27] and associated TI Fusion Digital Power Designer GUI [Ref 28]. This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-31, Table 1-32, and Table 1-33.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the setpoint at or above which the particular rail is deemed “good”. The PG Off Threshold is the setpoint at or below which the particular rail is no longer deemed “good”. The controller internally OR's these PG conditions together and drives an output PG pin High only if all active rail PG states are “good”. The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

Table 1-31 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 52 decimal (U32).

Table 1-31: **Power Rail Specifications for UCD9248 PMBus Controller at Address 52 Decimal**

Rail Number	Rail Name	Rail Name	Nominal VOUT (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold(1)		
										VOUT Over Fault (V)	IOUT Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCCINT	1	0.9	0.85	0	5	10	1	1.15	20	90
2	Rail #2	VCCPINT	1	0.9	0.85	0	5	10	1	1.15	20	90
3	Rail #3	VCCAUX	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90
4	Rail #4	VCCPAUX	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-32 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 53 decimal (U33).

Table 1-32: **Power Rail Specifications for UCD9248 PMBus Controller at Address 53 Decimal**

Rail Number	Rail Name	Schematic Rail Name	Nominal VOUT (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold(1)		
										VOUT Over Fault (V)	IOUT Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VADJ	2.5	2.25	2.125	0	5	1	1	2.875	10.41	90
2	Rail #2	VCC1V5	1.5	1.35	1.275	0	5	0	1	1.725	10.41	90
3	Rail #3	VCCMIO_PS	1.8	1.62	1.53	0	5	5	1	2.07	10.41	90
4	Rail #4	VCCBRAM	1	0.9	0.85	0	5	10	1	1.15	20	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-33 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 54 decimal (U34).

Table 1-33: **Power Rail Specifications for UCD9248 PMBus Controller at Address 54 Decimal**

Rail Number	Rail Name	Schematic Rail Name	Nominal VOUT (V)	PG On Threshold (V)	PG Off Threshold (V)	On Delay (ms)	Rise Time (ms)	Off Delay (ms)	Fall Time (ms)	Shutdown Threshold(1)		
										VOUT Over Fault (V)	IOUT Over Fault (A)	Temp Over Fault (°C)
1	Rail #1	VCC3V3	3.3	2.97	2.805	0	5	4	1	3.795	10.41	90
2	Rail #2	VCC2V5	2.5	2.25	2.125	0	5	1	1	2.875	10.41	90

Notes:

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Cooling Fan

The XC7Z020 AP SoC cooling fan connector J61 is wired directly to $12V_{DC}$ as shown in Figure 1-30.

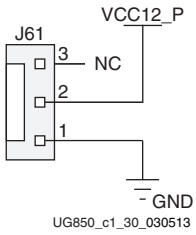


Figure 1-30: **Cooling Fan Circuit**

More information about the power system components used by the ZC702 board are available from the Texas Instruments digital power website [Ref 26].

XADC Analog-to-Digital Converter

[Figure 1-2, callout 26]

The XC7Z020 AP SoC provides an Analog Front End XADC block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See the *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 8] for details on the capabilities of the analog front end. Figure 1-31 shows the XADC block diagram.

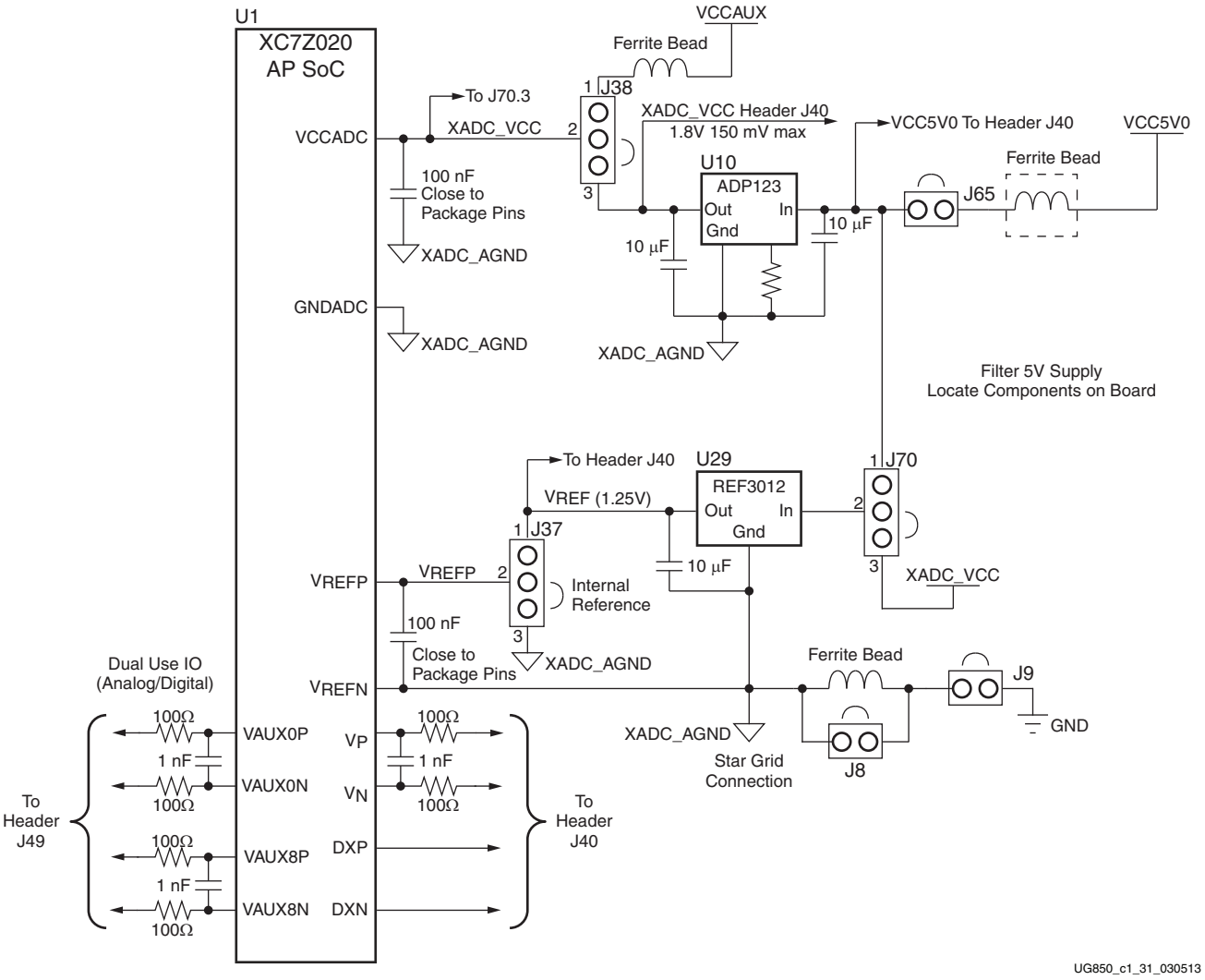


Figure 1-31: **XADC Block Diagram**

The ZC702 board supports both the internal XC7Z020 AP SoC sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available.

Jumper J37 can be used to select either an external voltage reference (VREF) or on-chip voltage reference for the analog-to-digital converter.

For external measurements an XADC header (J19) is provided. This header can be used to provide analog inputs to the XC7Z020 AP SoC dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the 4 GPIO pins available on the XADC header as multiplexer address lines. Figure 1-32 shows the XADC header connections.

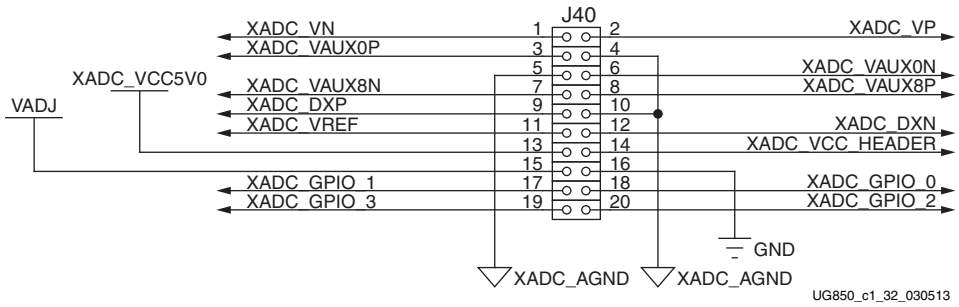


Figure 1-32: **XADC Header (J40)**

Table 1-34 describes the XADC header J40 pin functions.

Table 1-34: **XADC Header J40 Pinout**

Net Name	J19 Pin Number	Description
VN, VP	1, 2	Dedicated analog input channel for the XADC.
XADC_VAUX0P, N	3, 6	Auxiliary analog input channel 0. Also supports use as I/O inputs when anti alias capacitor is not present.
XADC_VAUX8N, P	7, 8	Auxiliary analog input channel 8. Also supports use as I/O inputs when anti alias capacitor is not present.
DXP, DXN	9, 12	Access to thermal diode.
XADC_AGND	4, 5, 10	Analog ground reference.
XADC_VREF	11	1.25V reference from the board.
XADC_VCC5V0	13	Filtered 5V supply from board.
XADC_VCC_HEADER	14	Analog 1.8V supply for XADC.
VADJ	15	VCCO supply for bank which is the source of DIO pins.
GND	16	Digital Ground (board) Reference
XADC_GPIO_3, 2, 1, 0	19, 20, 17, 18	Digital I/O. These pins should come from the same bank. These I/Os should not be shared with other functions because they are required to support 3-state operation.

Default Switch and Jumper Settings

Switches

[Figure 1-2, callout 24]

Default switch settings are listed in Table A-1.

Table A-1: **Default Switch Settings**

Switch	Position	Setting	Figure 1-2 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	23
	2	On	
SW12 (two-position DIP switch)	1	Off	19
	2	Off	
SW15 (two-position DIP switch)	1	Off	19
	2	Off	
SW16 (five-position DIP switch)	1	Right	29
	2	Right	
	3	Right	
	4	Right	
	5	Right	

Jumpers

[Figure 1-2, callout 24]

Default jumper positions are listed in Table A-2. Jumper locations are shown in Figure A-1.

Table A-2: **Default Jumper Settings**

Callout	Jumper	Function	Default Position
	HDR_1 X 2		
1	J5	CFGBVS short to GND	OFF

Table A-2: **Default Jumper Settings *(Cont'd)***

Callout	Jumper	Function	Default Position
2	J6	POR Master Reset	OFF
3	J7	USB 2.0 USB_VBUS_SEL	1-2
4	J8	XADC GND L3 BYPASS	OFF
5	J9	XADC GND	ON
6	J10	ARM HDR J41 PIN 2 TO VADJ	OFF
7	J11	UCD9248 U32 ADDR52 RESET_B	OFF
8	J12	FMC VADJ OFF	ON
9	J13	UCD9248 U33 ADDR53 RESET_B	OFF
10	J14	UCD9248 U34 ADDR54 RESET_B	OFF
11	J15	CAN BUS COMMON-MODE CANH HDR	1-2
12	J43	ETHERNET PHY HDR	1-2
13	J44	USB 2.0 USB_RESET_B	OFF
14	J53	CAN BUS COMMON-MODE CANL HDR	1-2
15	J56	JTAG HDR J58 PIN 2 3.3V SEL	OFF
16	J65	XADC_VCC5V0 = VCC5V0	ON
HDR_1 X 3			
17	J20	MIO3/QSPI_IO1	OFF
18	J21	MIO2/QSPI_IO0	OFF
19	J22	MIO4/QSPI_IO2	OFF
20	J25	MIO5/QSPI_IO3	OFF
21	J26	MIO6/QSPI_CLK	OFF
22	J27	PS_SRST_B	1-2
23	J28	PS_POR_B	1-2
24	J30	ETHERNET PHY HDR	1-2
25	J31	ETHERNET PHY HDR	NONE
26	J32	ETHERNET PHY HDR	NONE
27	J33	USB 2.0 MODE	2-3
28	J34	USB 2.0 J1 ID SEL	1-2
29	J35	USB 2.0 J1 VBUS CAP SEL	1-2
30	J36	USB 2.0 J1 GND SEL	1-2
31	J37	XADC_VREP SEL	1-2
32	J38	XADC_VCC SEL	2-3
33	J70	XADC_VREF SOURCE SEL	2-3

Figure A-1 shows jumper locations described in this table.

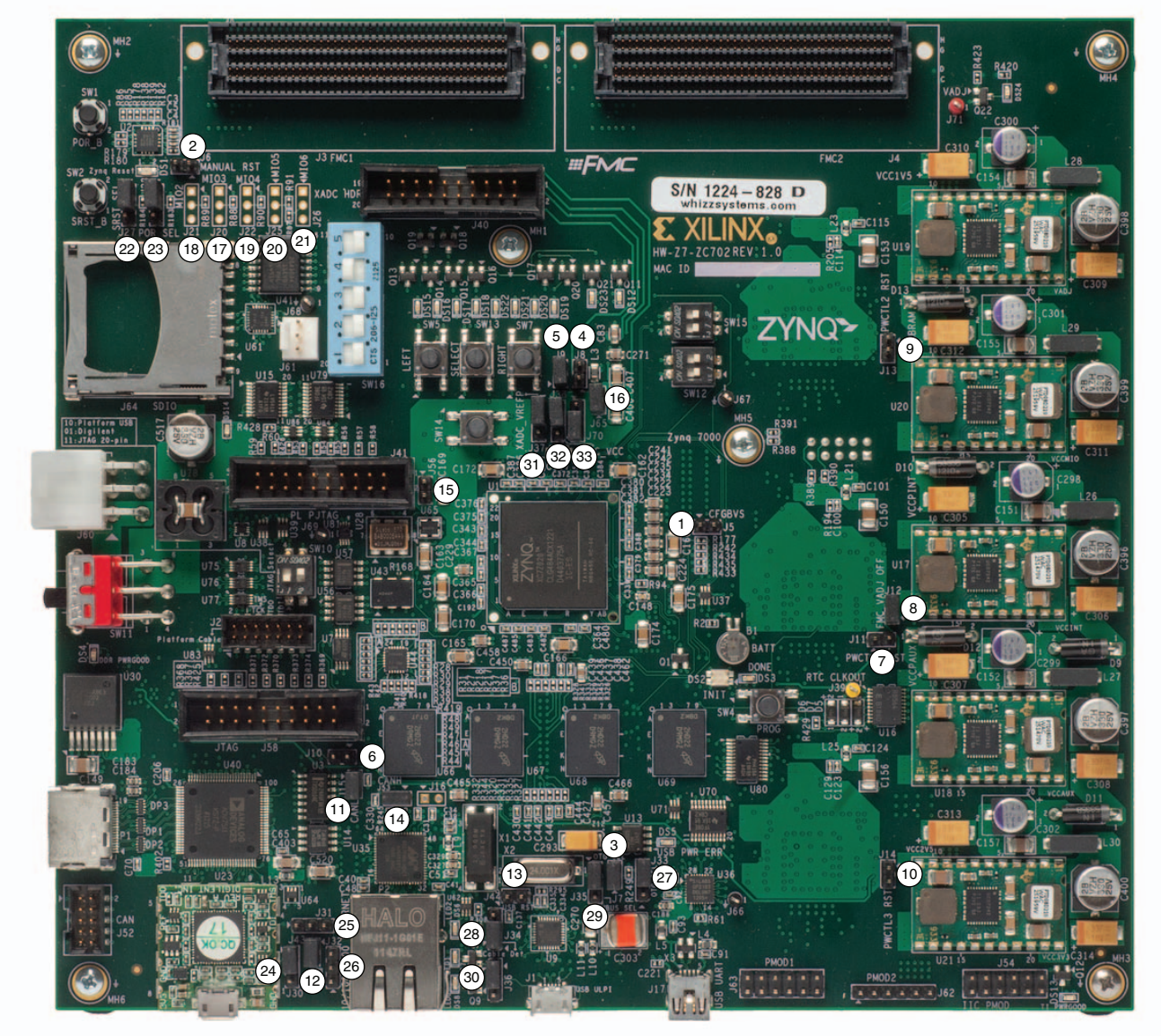


Figure A-1: **Jumper Locations**

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZC702 board implements the FMC specification, see FPGA Mezzanine (FMC) Card Interface, page 52 and LPC Connectors J3 and J4, page 52.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

UG850_aB_01_081612

Figure B-1: **FMC LPC Connector Pinout**

Master Constraints File Listing

Overview

The ZC702 Xilinx Design Constraints (XDC) template provides for designs targeting the ZC702 board. Net names in the constraints listed in the file correlate with net names on the latest ZC702 board schematic. You must identify the appropriate pins and replace the net names below with net names in your RTL.

See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 13] for more information.

For detailed I/O standards information required for a particular interface, refer to the constraint files generated by tools like the Memory Interface Generator (MIG) and Base System Builder (BSB).

The FMC LPC connectors J3 and J4 are connected to 2.5V VADJ banks. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Note: The ZC702 XDC file can be found on the Zynq-7000 All Programmable SoC ZC702 Evaluation Kit product page.

ZC702 Board Constraints File Listing

```
#FMC1 LPC
set_property PACKAGE_PIN H19 [get_ports FMC_C2M_PG_LS]
set_property IOSTANDARD LVCMOS25 [get_ports FMC_C2M_PG_LS]
set_property PACKAGE_PIN L19 [get_ports FMC1_LPC_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_CLK0_M2C_N]
set_property PACKAGE_PIN L18 [get_ports FMC1_LPC_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_CLK0_M2C_P]
set_property PACKAGE_PIN M20 [get_ports FMC1_LPC_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_CLK1_M2C_N]
set_property PACKAGE_PIN M19 [get_ports FMC1_LPC_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_CLK1_M2C_P]

#LA
set_property PACKAGE_PIN K20 [get_ports FMC1_LPC_LA00_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA00_CC_N]
```

```
set_property PACKAGE_PIN K19 [get_ports FMC1_LPC_LA00_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA00_CC_P]
set_property PACKAGE_PIN N20 [get_ports FMC1_LPC_LA01_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA01_CC_N]
set_property PACKAGE_PIN N19 [get_ports FMC1_LPC_LA01_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA01_CC_P]
set_property PACKAGE_PIN L22 [get_ports FMC1_LPC_LA02_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA02_N]
set_property PACKAGE_PIN L21 [get_ports FMC1_LPC_LA02_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA02_P]
set_property PACKAGE_PIN K21 [get_ports FMC1_LPC_LA03_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA03_N]
set_property PACKAGE_PIN J20 [get_ports FMC1_LPC_LA03_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA03_P]
set_property PACKAGE_PIN M22 [get_ports FMC1_LPC_LA04_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA04_N]
set_property PACKAGE_PIN M21 [get_ports FMC1_LPC_LA04_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA04_P]
set_property PACKAGE_PIN N18 [get_ports FMC1_LPC_LA05_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA05_N]
set_property PACKAGE_PIN N17 [get_ports FMC1_LPC_LA05_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA05_P]
set_property PACKAGE_PIN K18 [get_ports FMC1_LPC_LA06_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA06_N]
set_property PACKAGE_PIN J18 [get_ports FMC1_LPC_LA06_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA06_P]
set_property PACKAGE_PIN K15 [get_ports FMC1_LPC_LA07_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA07_N]
set_property PACKAGE_PIN J15 [get_ports FMC1_LPC_LA07_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA07_P]
set_property PACKAGE_PIN J22 [get_ports FMC1_LPC_LA08_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA08_N]
set_property PACKAGE_PIN J21 [get_ports FMC1_LPC_LA08_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA08_P]
set_property PACKAGE_PIN M16 [get_ports FMC1_LPC_LA09_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA09_N]
set_property PACKAGE_PIN M15 [get_ports FMC1_LPC_LA09_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA09_P]
set_property PACKAGE_PIN M17 [get_ports FMC1_LPC_LA10_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA10_N]
set_property PACKAGE_PIN L17 [get_ports FMC1_LPC_LA10_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA10_P]
set_property PACKAGE_PIN R21 [get_ports FMC1_LPC_LA11_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA11_N]
set_property PACKAGE_PIN R20 [get_ports FMC1_LPC_LA11_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA11_P]
set_property PACKAGE_PIN P22 [get_ports FMC1_LPC_LA12_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA12_N]
set_property PACKAGE_PIN N22 [get_ports FMC1_LPC_LA12_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA12_P]
set_property PACKAGE_PIN R16 [get_ports FMC1_LPC_LA13_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA13_N]
set_property PACKAGE_PIN P16 [get_ports FMC1_LPC_LA13_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA13_P]
set_property PACKAGE_PIN J17 [get_ports FMC1_LPC_LA14_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA14_N]
set_property PACKAGE_PIN J16 [get_ports FMC1_LPC_LA14_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA14_P]
set_property PACKAGE_PIN P21 [get_ports FMC1_LPC_LA15_N]
```

```
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA15_N]
set_property PACKAGE_PIN P20 [get_ports FMC1_LPC_LA15_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA15_P]
set_property PACKAGE_PIN P15 [get_ports FMC1_LPC_LA16_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA16_N]
set_property PACKAGE_PIN N15 [get_ports FMC1_LPC_LA16_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA16_P]
set_property PACKAGE_PIN B20 [get_ports FMC1_LPC_LA17_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA17_CC_N]
set_property PACKAGE_PIN B19 [get_ports FMC1_LPC_LA17_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA17_CC_P]
set_property PACKAGE_PIN C20 [get_ports FMC1_LPC_LA18_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA18_CC_N]
set_property PACKAGE_PIN D20 [get_ports FMC1_LPC_LA18_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA18_CC_P]
set_property PACKAGE_PIN E20 [get_ports FMC1_LPC_LA19_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA19_N]
set_property PACKAGE_PIN E19 [get_ports FMC1_LPC_LA19_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA19_P]
set_property PACKAGE_PIN G21 [get_ports FMC1_LPC_LA20_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA20_N]
set_property PACKAGE_PIN G20 [get_ports FMC1_LPC_LA20_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA20_P]
set_property PACKAGE_PIN F22 [get_ports FMC1_LPC_LA21_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA21_N]
set_property PACKAGE_PIN F21 [get_ports FMC1_LPC_LA21_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA21_P]
set_property PACKAGE_PIN F17 [get_ports FMC1_LPC_LA22_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA22_N]
set_property PACKAGE_PIN G17 [get_ports FMC1_LPC_LA22_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA22_P]
set_property PACKAGE_PIN G16 [get_ports FMC1_LPC_LA23_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA23_N]
set_property PACKAGE_PIN G15 [get_ports FMC1_LPC_LA23_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA23_P]
set_property PACKAGE_PIN A22 [get_ports FMC1_LPC_LA24_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA24_N]
set_property PACKAGE_PIN A21 [get_ports FMC1_LPC_LA24_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA24_P]
set_property PACKAGE_PIN B15 [get_ports FMC1_LPC_LA25_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA25_N]
set_property PACKAGE_PIN C15 [get_ports FMC1_LPC_LA25_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA25_P]
set_property PACKAGE_PIN E18 [get_ports FMC1_LPC_LA26_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA26_N]
set_property PACKAGE_PIN F18 [get_ports FMC1_LPC_LA26_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA26_P]
set_property PACKAGE_PIN C18 [get_ports FMC1_LPC_LA27_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA27_N]
set_property PACKAGE_PIN C17 [get_ports FMC1_LPC_LA27_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA27_P]
set_property PACKAGE_PIN C22 [get_ports FMC1_LPC_LA28_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA28_N]
set_property PACKAGE_PIN D22 [get_ports FMC1_LPC_LA28_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA28_P]
set_property PACKAGE_PIN B17 [get_ports FMC1_LPC_LA29_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA29_N]
set_property PACKAGE_PIN B16 [get_ports FMC1_LPC_LA29_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA29_P]
```

```
set_property PACKAGE_PIN D21 [get_ports FMC1_LPC_LA30_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA30_N]
set_property PACKAGE_PIN E21 [get_ports FMC1_LPC_LA30_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA30_P]
set_property PACKAGE_PIN A17 [get_ports FMC1_LPC_LA31_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA31_N]
set_property PACKAGE_PIN A16 [get_ports FMC1_LPC_LA31_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA31_P]
set_property PACKAGE_PIN B22 [get_ports FMC1_LPC_LA32_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA32_N]
set_property PACKAGE_PIN B21 [get_ports FMC1_LPC_LA32_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA32_P]
set_property PACKAGE_PIN A19 [get_ports FMC1_LPC_LA33_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA33_N]
set_property PACKAGE_PIN A18 [get_ports FMC1_LPC_LA33_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC1_LPC_LA33_P]

#FMC2 LPC
set_property PACKAGE_PIN AA18 [get_ports FMC2_LPC_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_CLK0_M2C_N]
set_property PACKAGE_PIN Y18 [get_ports FMC2_LPC_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_CLK0_M2C_P]
set_property PACKAGE_PIN Y5 [get_ports FMC2_LPC_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_CLK1_M2C_N]
set_property PACKAGE_PIN Y6 [get_ports FMC2_LPC_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_CLK1_M2C_P]

#LA
set_property PACKAGE_PIN AA19 [get_ports FMC2_LPC_LA00_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA00_CC_N]
set_property PACKAGE_PIN Y19 [get_ports FMC2_LPC_LA00_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA00_CC_P]
set_property PACKAGE_PIN Y16 [get_ports FMC2_LPC_LA01_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA01_CC_N]
set_property PACKAGE_PIN W16 [get_ports FMC2_LPC_LA01_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA01_CC_P]
set_property PACKAGE_PIN V15 [get_ports FMC2_LPC_LA02_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA02_N]
set_property PACKAGE_PIN V14 [get_ports FMC2_LPC_LA02_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA02_P]
set_property PACKAGE_PIN AB16 [get_ports FMC2_LPC_LA03_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA03_N]
set_property PACKAGE_PIN AA16 [get_ports FMC2_LPC_LA03_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA03_P]
set_property PACKAGE_PIN W13 [get_ports FMC2_LPC_LA04_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA04_N]
set_property PACKAGE_PIN V13 [get_ports FMC2_LPC_LA04_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA04_P]
set_property PACKAGE_PIN AB20 [get_ports FMC2_LPC_LA05_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA05_N]
set_property PACKAGE_PIN AB19 [get_ports FMC2_LPC_LA05_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA05_P]
set_property PACKAGE_PIN V17 [get_ports FMC2_LPC_LA06_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA06_N]
set_property PACKAGE_PIN U17 [get_ports FMC2_LPC_LA06_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA06_P]
set_property PACKAGE_PIN U21 [get_ports FMC2_LPC_LA07_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA07_N]
set_property PACKAGE_PIN T21 [get_ports FMC2_LPC_LA07_P]
```

```
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA07_P]
set_property PACKAGE_PIN AB17 [get_ports FMC2_LPC_LA08_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA08_N]
set_property PACKAGE_PIN AA17 [get_ports FMC2_LPC_LA08_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA08_P]
set_property PACKAGE_PIN U16 [get_ports FMC2_LPC_LA09_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA09_N]
set_property PACKAGE_PIN U15 [get_ports FMC2_LPC_LA09_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA09_P]
set_property PACKAGE_PIN Y21 [get_ports FMC2_LPC_LA10_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA10_N]
set_property PACKAGE_PIN Y20 [get_ports FMC2_LPC_LA10_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA10_P]
set_property PACKAGE_PIN AA14 [get_ports FMC2_LPC_LA11_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA11_N]
set_property PACKAGE_PIN Y14 [get_ports FMC2_LPC_LA11_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA11_P]
set_property PACKAGE_PIN Y15 [get_ports FMC2_LPC_LA12_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA12_N]
set_property PACKAGE_PIN W15 [get_ports FMC2_LPC_LA12_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA12_P]
set_property PACKAGE_PIN W22 [get_ports FMC2_LPC_LA13_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA13_N]
set_property PACKAGE_PIN V22 [get_ports FMC2_LPC_LA13_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA13_P]
set_property PACKAGE_PIN U22 [get_ports FMC2_LPC_LA14_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA14_N]
set_property PACKAGE_PIN T22 [get_ports FMC2_LPC_LA14_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA14_P]
set_property PACKAGE_PIN AA13 [get_ports FMC2_LPC_LA15_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA15_N]
set_property PACKAGE_PIN Y13 [get_ports FMC2_LPC_LA15_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA15_P]
set_property PACKAGE_PIN AB15 [get_ports FMC2_LPC_LA16_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA16_N]
set_property PACKAGE_PIN AB14 [get_ports FMC2_LPC_LA16_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA16_P]
set_property PACKAGE_PIN AA6 [get_ports FMC2_LPC_LA17_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA17_CC_N]
set_property PACKAGE_PIN AA7 [get_ports FMC2_LPC_LA17_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA17_CC_P]
set_property PACKAGE_PIN AA8 [get_ports FMC2_LPC_LA18_CC_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA18_CC_N]
set_property PACKAGE_PIN AA9 [get_ports FMC2_LPC_LA18_CC_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA18_CC_P]
set_property PACKAGE_PIN T6 [get_ports FMC2_LPC_LA19_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA19_N]
set_property PACKAGE_PIN R6 [get_ports FMC2_LPC_LA19_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA19_P]
set_property PACKAGE_PIN U4 [get_ports FMC2_LPC_LA20_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA20_N]
set_property PACKAGE_PIN T4 [get_ports FMC2_LPC_LA20_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA20_P]
set_property PACKAGE_PIN V4 [get_ports FMC2_LPC_LA21_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA21_N]
set_property PACKAGE_PIN V5 [get_ports FMC2_LPC_LA21_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA21_P]
set_property PACKAGE_PIN U9 [get_ports FMC2_LPC_LA22_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA22_N]
```

```
set_property PACKAGE_PIN U10 [get_ports FMC2_LPC_LA22_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA22_P]
set_property PACKAGE_PIN W12 [get_ports FMC2_LPC_LA23_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA23_N]
set_property PACKAGE_PIN V12 [get_ports FMC2_LPC_LA23_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA23_P]
set_property PACKAGE_PIN U5 [get_ports FMC2_LPC_LA24_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA24_N]
set_property PACKAGE_PIN U6 [get_ports FMC2_LPC_LA24_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA24_P]
set_property PACKAGE_PIN AB12 [get_ports FMC2_LPC_LA25_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA25_N]
set_property PACKAGE_PIN AA12 [get_ports FMC2_LPC_LA25_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA25_P]
set_property PACKAGE_PIN U11 [get_ports FMC2_LPC_LA26_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA26_N]
set_property PACKAGE_PIN U12 [get_ports FMC2_LPC_LA26_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA26_P]
set_property PACKAGE_PIN AB1 [get_ports FMC2_LPC_LA27_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA27_N]
set_property PACKAGE_PIN AB2 [get_ports FMC2_LPC_LA27_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA27_P]
set_property PACKAGE_PIN AB4 [get_ports FMC2_LPC_LA28_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA28_N]
set_property PACKAGE_PIN AB5 [get_ports FMC2_LPC_LA28_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA28_P]
set_property PACKAGE_PIN AB11 [get_ports FMC2_LPC_LA29_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA29_N]
set_property PACKAGE_PIN AA11 [get_ports FMC2_LPC_LA29_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA29_P]
set_property PACKAGE_PIN AB6 [get_ports FMC2_LPC_LA30_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA30_N]
set_property PACKAGE_PIN AB7 [get_ports FMC2_LPC_LA30_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA30_P]
set_property PACKAGE_PIN AB9 [get_ports FMC2_LPC_LA31_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA31_N]
set_property PACKAGE_PIN AB10 [get_ports FMC2_LPC_LA31_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA31_P]
set_property PACKAGE_PIN AA4 [get_ports FMC2_LPC_LA32_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA32_N]
set_property PACKAGE_PIN Y4 [get_ports FMC2_LPC_LA32_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA32_P]
set_property PACKAGE_PIN Y10 [get_ports FMC2_LPC_LA33_N]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA33_N]
set_property PACKAGE_PIN Y11 [get_ports FMC2_LPC_LA33_P]
set_property IOSTANDARD LVCMOS25 [get_ports FMC2_LPC_LA33_P]

#GPIO DIP SW
set_property PACKAGE_PIN W6 [get_ports GPIO_DIP_SW0]
set_property IOSTANDARD LVCMOS25 [get_ports GPIO_DIP_SW0]
set_property PACKAGE_PIN W7 [get_ports GPIO_DIP_SW1]
set_property IOSTANDARD LVCMOS25 [get_ports GPIO_DIP_SW1]

GPIO P.B. SW
set_property PACKAGE_PIN G19 [get_ports GPIO_SW_N]
set_property IOSTANDARD LVCMOS25 [get_ports GPIO_SW_N]
set_property PACKAGE_PIN F19 [get_ports GPIO_SW_S]
set_property IOSTANDARD LVCMOS25 [get_ports GPIO_SW_S]
```

```
#HDMI
set_property PACKAGE_PIN U14 [get_ports HDMI_INT]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_INT]
set_property PACKAGE_PIN K16 [get_ports 6N1412]
set_property IOSTANDARD LVCMOS25 [get_ports 6N1412]
set_property PACKAGE_PIN L16 [get_ports HDMI_R_CLK]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_CLK]
set_property PACKAGE_PIN AB21 [get_ports HDMI_R_D0]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D0]
set_property PACKAGE_PIN AA21 [get_ports HDMI_R_D1]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D1]
set_property PACKAGE_PIN AB22 [get_ports HDMI_R_D2]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D2]
set_property PACKAGE_PIN AA22 [get_ports HDMI_R_D3]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D3]
set_property PACKAGE_PIN V19 [get_ports HDMI_R_D4]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D4]
set_property PACKAGE_PIN V18 [get_ports HDMI_R_D5]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D5]
set_property PACKAGE_PIN V20 [get_ports HDMI_R_D6]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D6]
set_property PACKAGE_PIN U20 [get_ports HDMI_R_D7]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D7]
set_property PACKAGE_PIN W21 [get_ports HDMI_R_D8]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D8]
set_property PACKAGE_PIN W20 [get_ports HDMI_R_D9]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D9]
set_property PACKAGE_PIN W18 [get_ports HDMI_R_D10]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D10]
set_property PACKAGE_PIN T19 [get_ports HDMI_R_D11]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D11]
set_property PACKAGE_PIN U19 [get_ports HDMI_R_D12]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D12]
set_property PACKAGE_PIN R19 [get_ports HDMI_R_D13]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D13]
set_property PACKAGE_PIN T17 [get_ports HDMI_R_D14]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D14]
set_property PACKAGE_PIN T16 [get_ports HDMI_R_D15]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_D15]
set_property PACKAGE_PIN T18 [get_ports HDMI_R_DE]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_DE]
set_property PACKAGE_PIN R18 [get_ports HDMI_R_HSYNC]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_HSYNC]
set_property PACKAGE_PIN R15 [get_ports HDMI_R_SPDIF]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_SPDIF]
set_property PACKAGE_PIN H15 [get_ports HDMI_R_VSYNC]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_R_VSYNC]
set_property PACKAGE_PIN H20 [get_ports HDMI_SPDIF_OUT_LS]
set_property IOSTANDARD LVCMOS25 [get_ports HDMI_SPDIF_OUT_LS]

#RTC
set_property PACKAGE_PIN U7 [get_ports IIC_RTC_IRQ_1_B]
set_property IOSTANDARD LVCMOS25 [get_ports IIC_RTC_IRQ_1_B]

#IIC
set_property PACKAGE_PIN W11 [get_ports IIC_SCL_MAIN_LS]
set_property IOSTANDARD LVCMOS25 [get_ports IIC_SCL_MAIN_LS]
set_property PACKAGE_PIN W8 [get_ports IIC_SDA_MAIN_LS]
set_property IOSTANDARD LVCMOS25 [get_ports IIC_SDA_MAIN_LS]
```

```
#PL_PJTAG
set_property PACKAGE_PIN V10 [get_ports PL_PJTAG_TCK]
set_property IOSTANDARD LVCMOS25 [get_ports PL_PJTAG_TCK]
set_property PACKAGE_PIN V8 [get_ports PL_PJTAG_TDI]
set_property IOSTANDARD LVCMOS25 [get_ports PL_PJTAG_TDI]
set_property PACKAGE_PIN R7 [get_ports PL_PJTAG_TDO_R]
set_property IOSTANDARD LVCMOS25 [get_ports PL_PJTAG_TDO_R]
set_property PACKAGE_PIN V9 [get_ports PL_PJTAG_TMS]
set_property IOSTANDARD LVCMOS25 [get_ports PL_PJTAG_TMS]

#GPIO PMOD1
set_property PACKAGE_PIN E15 [get_ports PMOD1_0_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD1_0_LS]
set_property PACKAGE_PIN D15 [get_ports PMOD1_1_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD1_1_LS]
set_property PACKAGE_PIN W17 [get_ports PMOD1_2_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD1_2_LS]
set_property PACKAGE_PIN W5 [get_ports PMOD1_3_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD1_3_LS]

#GPIO PMOD2
set_property PACKAGE_PIN V7 [get_ports PMOD2_0_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD2_0_LS]
set_property PACKAGE_PIN W10 [get_ports PMOD2_1_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD2_1_LS]
set_property PACKAGE_PIN P18 [get_ports PMOD2_2_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD2_2_LS]
set_property PACKAGE_PIN P17 [get_ports PMOD2_3_LS]
set_property IOSTANDARD LVCMOS25 [get_ports PMOD2_3_LS]

#CLOCKS
set_property PACKAGE_PIN C19 [get_ports SYSCLK_N]
set_property IOSTANDARD LVDS_25 [get_ports SYSCLK_N]
set_property PACKAGE_PIN D18 [get_ports SYSCLK_P]
set_property IOSTANDARD LVDS_25 [get_ports SYSCLK_P]
set_property PACKAGE_PIN Y8 [get_ports USRCLK_N]
set_property IOSTANDARD LVDS_25 [get_ports USRCLK_N]
set_property PACKAGE_PIN Y9 [get_ports USRCLK_P]
set_property IOSTANDARD LVDS_25 [get_ports USRCLK_P]

#ADC GPIO
set_property PACKAGE_PIN H17 [get_ports XADC_GPIO_0]
set_property IOSTANDARD LVCMOS25 [get_ports XADC_GPIO_0]
set_property PACKAGE_PIN H22 [get_portsports XADC_GPIO_1]
set_property IOSTANDARD LVCMOS25 [get_ports XADC_GPIO_1]
set_property PACKAGE_PIN G22 [get_ports XADC_GPIO_2]
set_property IOSTANDARD LVCMOS25 [get_ports XADC_GPIO_2]
set_property PACKAGE_PIN H18 [get_ports XADC_GPIO_3]
set_property IOSTANDARD LVCMOS25 [get_ports XADC_GPIO_3]
```

Board Specifications

Dimensions

Width: 7.750 in. (19.685 cm)

Length: 7.150 in. (18.161 cm)

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

For definitions and terms, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the ZC702 board and its documentation is available on the following websites.

ZC702 Evaluation Kit

ZC702 Evaluation Kit – Master Answer Record (AR 47864)

These Xilinx documents provide supplemental material useful with this guide:

1. *Zynq-7000 All Programmable SoC Overview* (DS190)
2. *Zynq-7000 All Programmable SoC (XC7Z010 and XC7Z020): DC and AC Switching Characteristics* (DS187)
3. *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138)
4. *7 Series FPGAs Configuration User Guide* (UG470)

5. *7 Series FPGAs Memory Resources User Guide* (UG473)
6. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
7. *7 Series FPGAs Integrated Block for PCI Express User Guide* (UG477)
8. *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480)
9. *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)
10. *7 Series FPGAs Memory Interface Solutions v1.8 User Guide* (UG586)
11. *Zynq-7000 All Programmable SoC Packaging and Pinout User Guide* (UG865)
12. *AMS101 Evaluation Card User Guide* (UG886)
13. *Vivado Design Suite User Guide: Using Constraints* (UG903)
14. *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933)

The following websites provide supplemental material useful with this guide:

15. Micron Technology: www.micron.com
    (N25Q128A11ESF40G, MT41J256M8HX-15E)
16. Standard Microsystems Corporation: www.smsc.com/
    (USB3320)
17. SanDisk Corporation: www.sandisk.com
18. SD Association: www.sdcard.org
19. SiTime: www.sitime.com
    (SiT8103, SiT9102)
20. Silicon Labs: www.silabs.com
    (Si570, Si5324C)
21. Marvell Semiconductor: www.marvell.com
    (88E1116R)
22. Analog Devices: www.analog.com/en/index.html
    (ADV7511KSTZ-P, ADP123)
23. Epson Electronics America: www.eea.epson.com and
    www.eea.epson.com/portal/pls/portal/docs/1/1413485.PDF
    (RTC-8564JE)
24. Digilent: www.digilentinc.com and
    www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9
    (Pmod Peripheral Modules)
25. NXP Semiconductors: ics.nxp.com
    (TJA01040)

26. Texas Instruments: www.ti.com, www.ti.com/fusiondocs, www.ti.com/ww/en/analog/digital-power/index.html and (UCD9248PFC, PTD08A010W, PTD08A020W, PTD08D210W, LMZ12002, TL1962ADC, TPS51200DR, PCA9548)
27. Texas Instruments EVM USB-TO-GPIO: www.ti.com/xilinx_usb.
28. Texas Instruments TI Fusion Digital Power Designer GUI, downloadable from: http://www.ti.com/fusion-gui
29. Samtec: www.samtec.com. (SEAF series connectors)
30. Integrated Device Technology: www.idt.com (ICS844021I)

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the ZC702 board master answer record concerning the CE requirements for the PC Test Environment:

www.xilinx.com/support/answers/47864.htm

Declaration of Conformity

The Zynq-7000 ZC702 Declaration of Conformity is online.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.